Contribution ID: **78** Type: **Oral**

Implementing the GBT data transmission protocol in FPGAs

Friday, 25 September 2009 10:10 (25 minutes)

The GBT chip is a radiation tolerant ASIC that can be used to implement bidirectional multipurpose 4.8 Gb/s optical links for high-energy physics experiments. It will be proposed to the LHC experiments for combined transmission of physics data, trigger, timing, fast and slow control and monitoring. Although radiation hardness is required on detectors, it is not necessary for the electronics located in the counting rooms. Therefore, a study is being made to implement these GBT links on FPGAs. This paper will describe the GBT protocol implementation, the configuration of the transceivers on Altera Stratix II GX and Xilinx Virtex 4, the optimization of resource for multi-transceivers, the first data transmission tests and the source code availability.

Summary

The GBT chip is a radiation tolerant ASIC that can be used to implement bidirectional multipurpose 4.8 Gb/s optical links for high-energy physics experiments. It will be proposed to the LHC experiments for combined transmission of physics data, trigger, timing, fast and slow control and monitoring. Although radiation hardness is required on detectors, it is not necessary for the electronics located in the counting rooms, where the GBT functionality can be realized using commercial off-the-shelf (COTS) components.
A physical implementation of the protocol has been achieved for FPGA devices in the most versatile way: on Altera and Xilinx devices, in Verilog and in VHDL. It is currently based on Altera Stratix II GX and Xilinx Virtex 4. Stratix IV GX and Virtex 5-6 versions are under study.
This paper will first describe the GBT protocol implementation: scrambling, Reed-Solomon encoding, interleaving for the transmission and de-interleaving, decoding and descrambling for the reception. It will then focus on practical solutions to make Stratix and Virtex transceivers match the custom encoding scheme chosen for the GBT (in particular, the word alignment in the receiver will be treated). Results will be presented on latency, single channel occupancy, resource optimization when using several channels in a chip and bit error rate measurements. Finally, information will be given on how to use the available source code and how to integrate GBT functionality into custom FPGA applications.

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Session Classification: Plenary Session 6 - Programmable Logic, Boards, Crates and Systems

Track Classification: Programmable Logic, design tools and methods