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Low power discriminator for ATLAS pixel chip

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The design of the front-end (FE) pixel electronics requires high speed, low power, low noise and low threshold dispersion. In this work, we propose a new architecture for the discriminator circuit. It is based on the principle of dynamic biasing and developed for the FE chip of the ATLAS pixel upgrade. This paper presents two discriminator structures where the bias current depends on the presence of a signal at the input of the discriminator. Since the activity in the FE chip is very low, the power consumption is greatly reduced.

Summary

A pixel FE pixel chip is developed in a 130nm CMOS technology for the B-layer replacement. The chip contains around ˜27,000 pixels of 50µm×250µm each. The pixel contains a fast charge preamplifier, a second stage amplifier, a discriminator and a logic bloc to transfer the hit information to the chip periphery.
The current pixel design uses a continuous biased discriminator where the bias current is defined in order to reach the required speed and to minimise the time walk. This allows assigning the hits to their corresponding bunch numbers with high probability. In the main analog pixel architecture flavour studied, the discriminator power consumption can reach 20% of the total pixel power budget.
Since the average counting rate for one pixel is low, it is possible to greatly reduce the power consumption of the pixel if the discriminator is biased only when a hit is present.
This paper proposes an efficient way to design very low power discriminators for pixel detectors. Two different architectures based on the dynamic biasing principle are proposed.
In the first one, an input differential stage controls the bias of the main comparator stage. The input voltage signal is converted to a current signal used to bias the second stage after applying a multiplicative factor.
The second architecture uses two stages. An auxiliary comparator with a low threshold value powers up selectively the main comparator stage.
A prototype test chip has been designed as an array of ˜300 pixels. Different discriminator architectures were implemented in this design. The chip is submitted for fabrication in 130 nm CMOS technology. We will be able to compare power consumption, noise and dispersion performances, as well as timing and crosstalk performances for the implemented architectures.

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