Status and plans for the pigtails

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INFN Milano LHCb UT Workshop

17-19 May 2016

Universität Zürich UZH

MAX-PLANCK-INSTITUT FÜR KERNPHYSIK HEIDELBERG

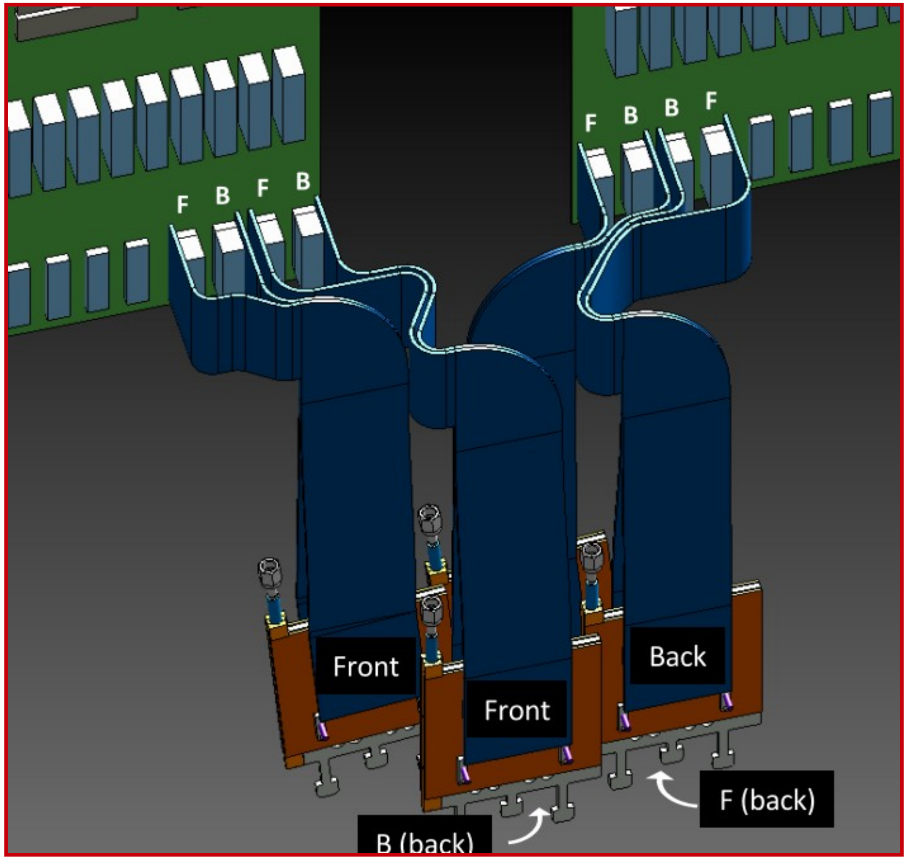
LHCb

Topics

- Brief introduction
- Pigtails limitations
- Study of the possibilities
- Mechanical mock-up
- Last pigtail version
- Future plans

Brief introduction

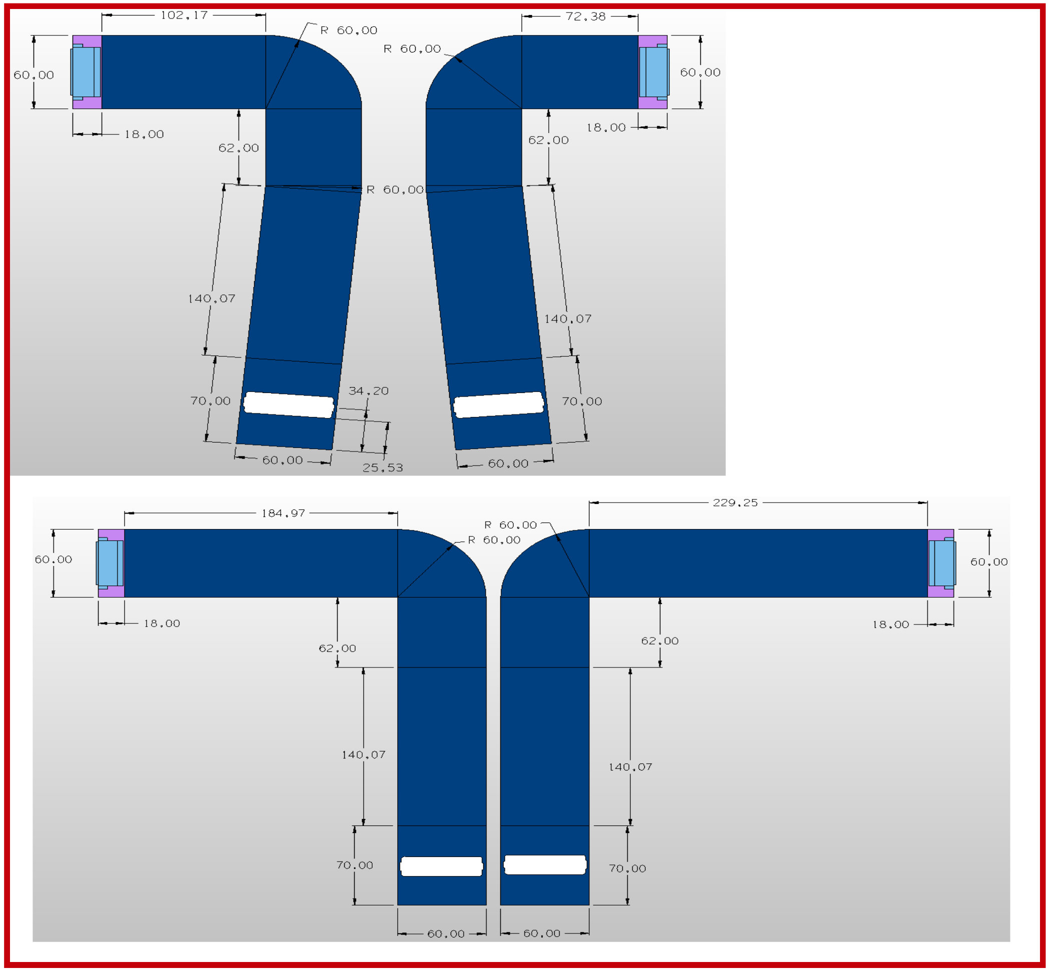
- Flex cable from the stave to the backplanes and need to perform several bends.
- Almost 400 pins to route.
- Two connectors: MEGARRAY and SEAF8-RA.



Pigtail limitations

- **Mechanical:**
  - **Max. Width**: 60mm
  - **Aprox. Shape and sizes:**
  - **Need to perform some bends**:

Degrees	Radius (mm)	Length (mm)
80	10	14
90	10	15.7
130	10	22.64



Min. Radius: 15xThickness

Max.Thickness: 370um

Pigtail limitations

- **Connectors:**

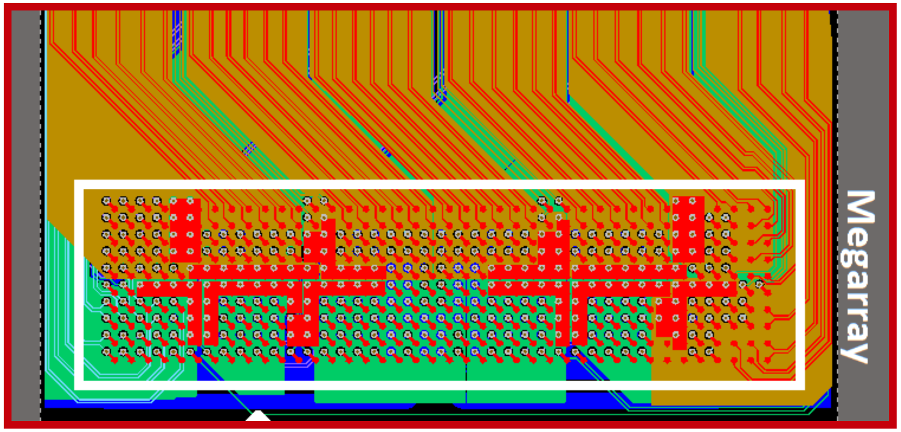
  MEGARRAY 400: Pad Pitch: 1.27mm

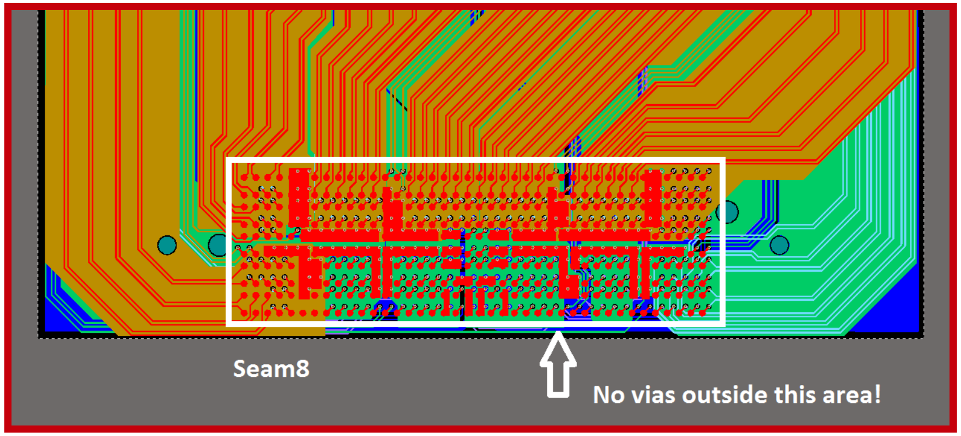
  As wide as the pigtail cable. No space at sides.

  SEAF8-RA: Pad Pitch: 0.8 mm

  Small connector. It limits the size of vias and tracks we can use.

  All these issues affect the fan-out design!





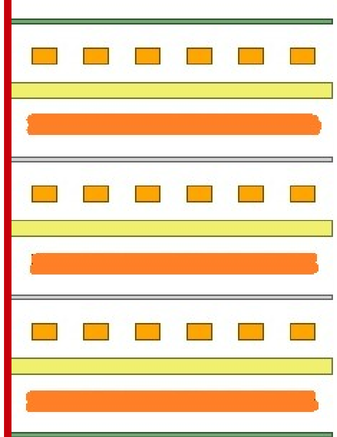
Pigtail limitations

- **Electrical:**
  - Z. diff for pairs: 100 ohms
  - Max. DC resistance for pairs (longest path 55cm): 5 ohms → Should not go under 100um trace width
  - DC resistance for PWR planes << 1 ohm

Study of possibilities

◆ **First pigtail prototype**

6-layer cable. Total thickness: 676um
Too high! Must be less than 370um approx.
Need to reduce this if we want it to be flex!



Layer Name	Type	Material	Thickness (mm)	Dielectric Material	Dielectric Constant	Pullback (mm)	Orientation
Top Overlay	Overlay						
Top Solder	Solder Mask/...	Surface Mat...	0.01	Solder Resist	3.5		
Top Layer	Signal	Copper	0.017				Top
Dielectric 1	Dielectric	Core	0.1	kapton	3.4		
Digital1	Signal	Copper	0.035				Not Allowed
Dielectric 2	Dielectric	Prepreg	0.1	kapton	3.4		
Signal Layer 2	Signal	Copper	0.017				Not Allowed
Dielectric 3	Dielectric	Core	0.1	kapton	3.4		
Digital2	Signal	Copper	0.035				Not Allowed
Dielectric 4	Dielectric	Prepreg	0.1	kapton	3.4		
Signal Layer 3	Signal	Copper	0.017				Not Allowed
Dielectric 5	Dielectric	Core	0.1	kapton	3.4		
Bottom Layer	Signal	Copper	0.035				Bottom
Bottom Solder	Solder Mask/...	Surface Mat...	0.01	Solder Resist	3.5		
Bottom Over...	Overlay						

Total Thickness: 0.676mm | Add Layer | Delete Layer | Move Up | Move Down | Drill Pairs... | Impedance Calculation...

Study of possibilities

- **Some proposals**

1) Try to design a 4 layer cable.

- **Reduce the substrate from 100um to 50um→ This implies going from a standard to a high-density routing (traces width << 100um).**
- **If we condense all pairs in two layers (standard or high density):**

There's space at the cable itself, but difficult to route the fan-out.

Each connector has a different limitation, so it's complicated to reconcile both fan-outs.

Problems

- High DC resistance at diff. pairs as traces get thinner. More than 5 ohms!
- Power planes width would be reduced to half & can't be routed in just one layer.
- For stripline traces in diff. pairs (high density) we need a HUGE separation.
- Not viable

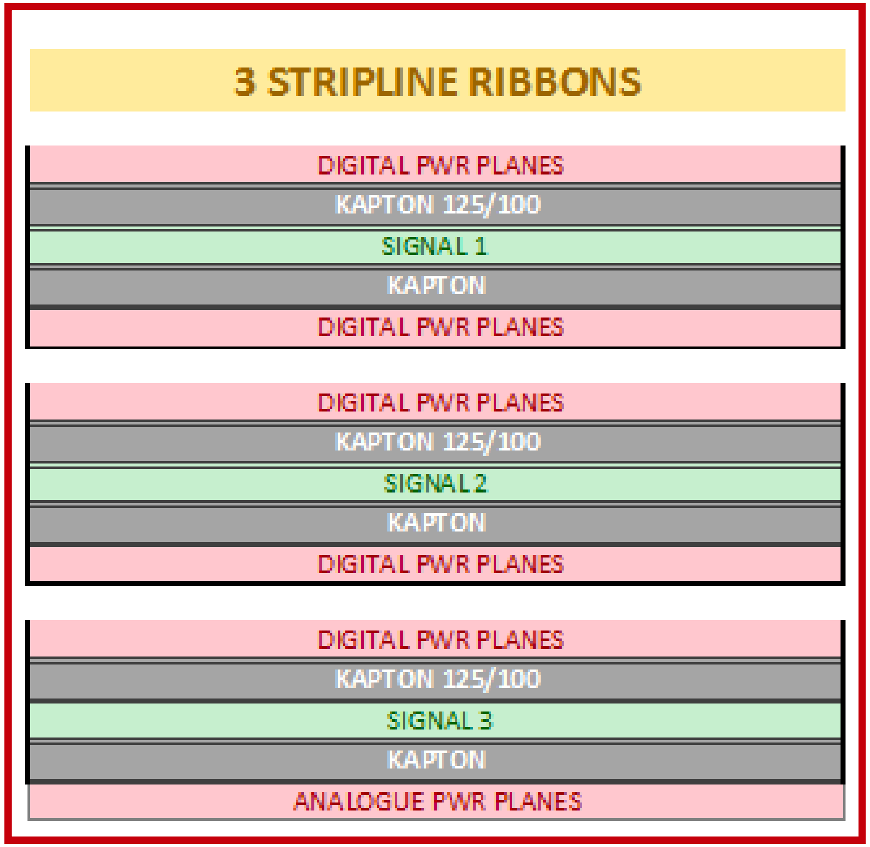
Study of possibilities

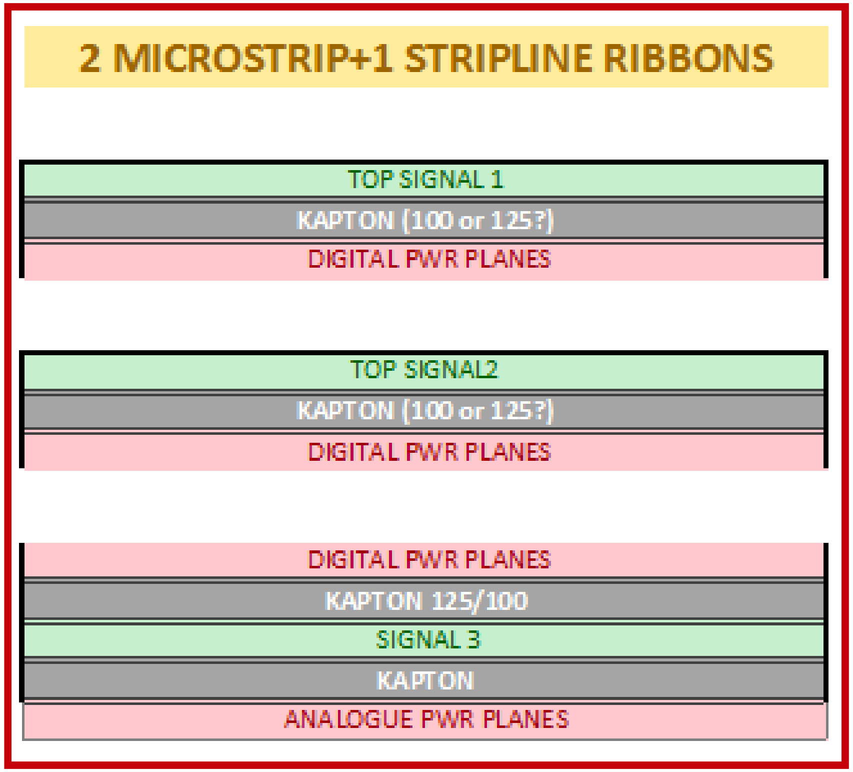
2) Split the cable in 3 ribbons

- We divide the total thickness, so the ribbons are more flexible.
- We can use wider pair traces if we increase a little bit the substrate (125um) → decreases DC resistance.
- Power lanes can remain as in the 3 layer cable design, which have a good DC resistance values.
- Much more freedom in the design.

Study of possibilities

- Possible configurations:





Best option in terms of SI and PI!

Study of possibilities

- Comparison

DESIGN	Mechanics	DC resistance	Routing
6 layer cable			
4 layer high density			
4 layer standard			
Splitted in 3ribbons			

For a 4 layer cable I need 2 layers for DIG powering. Do we really need analogue powering?

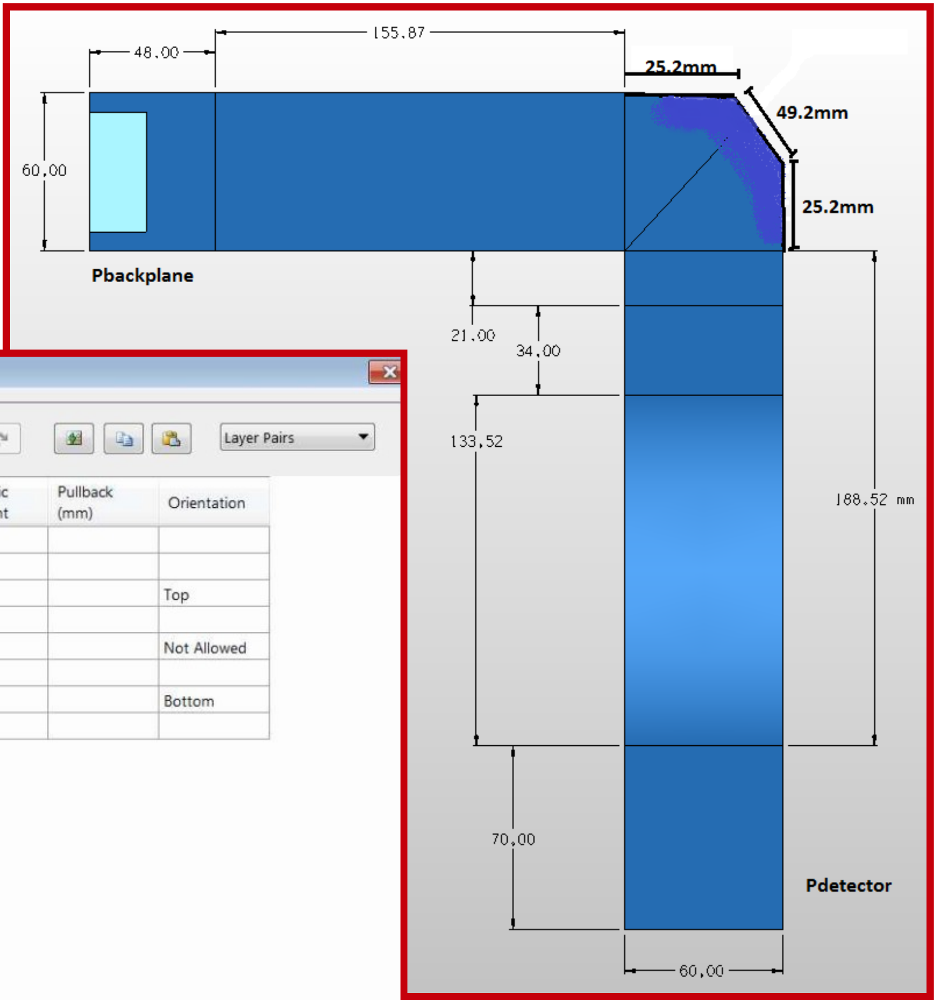
BAD
CAN LIVE WITH IT
GOOD

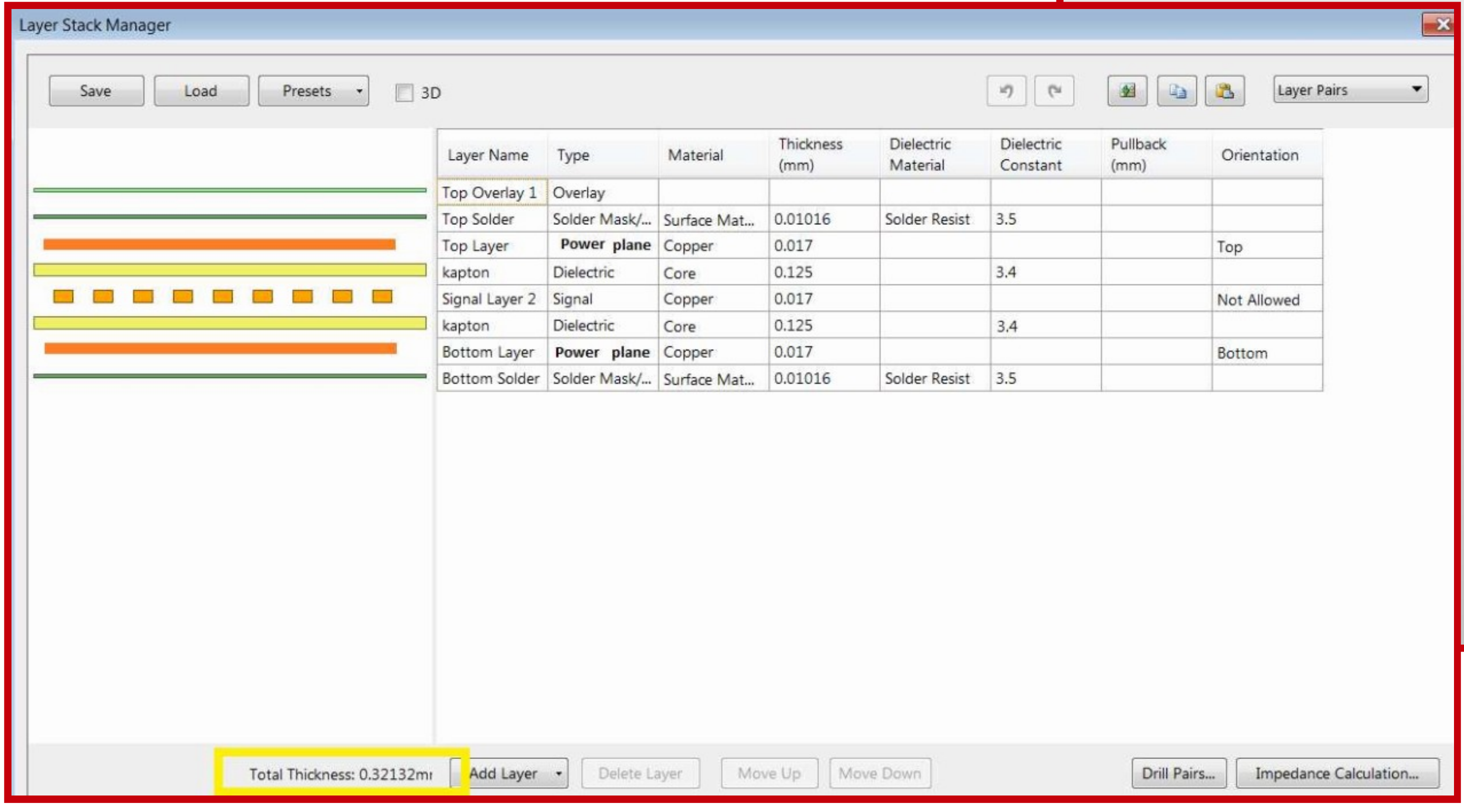
Mechanical Mock-up

- As we had a lot of doubts about the flexibility of the ribbons, we decided to produce a mechanical mock-up at CERN.
- 1 ribbon was designed. Next, we produced 3 of them.
- The ribbons are glued at one end and free at the other one, so we can study the movement.

Mechanical Mock-up

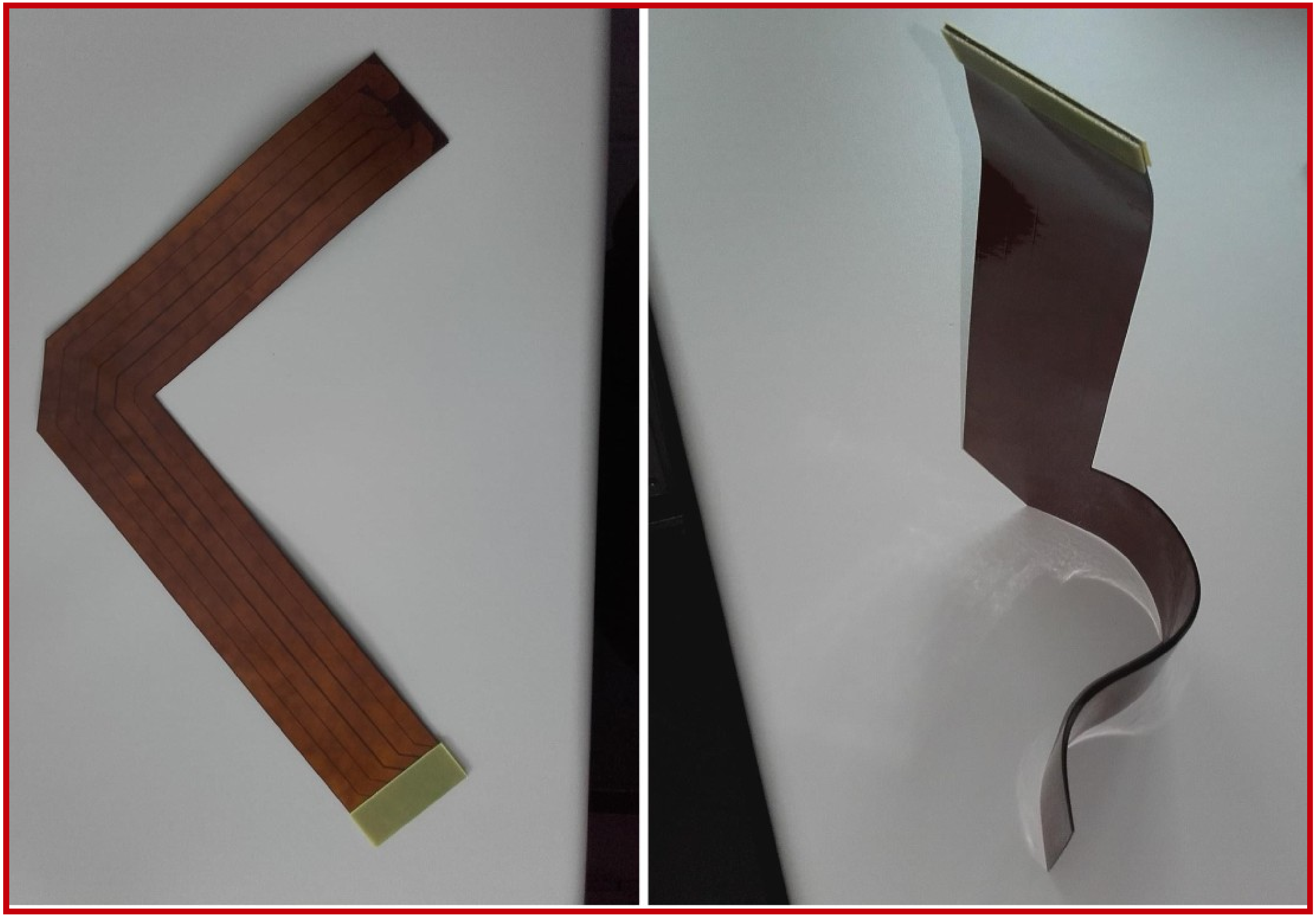
Copper thickness: 17um
Diff. Pairs: 109/235 um
Substrate: 125um
Total thickness: 320um





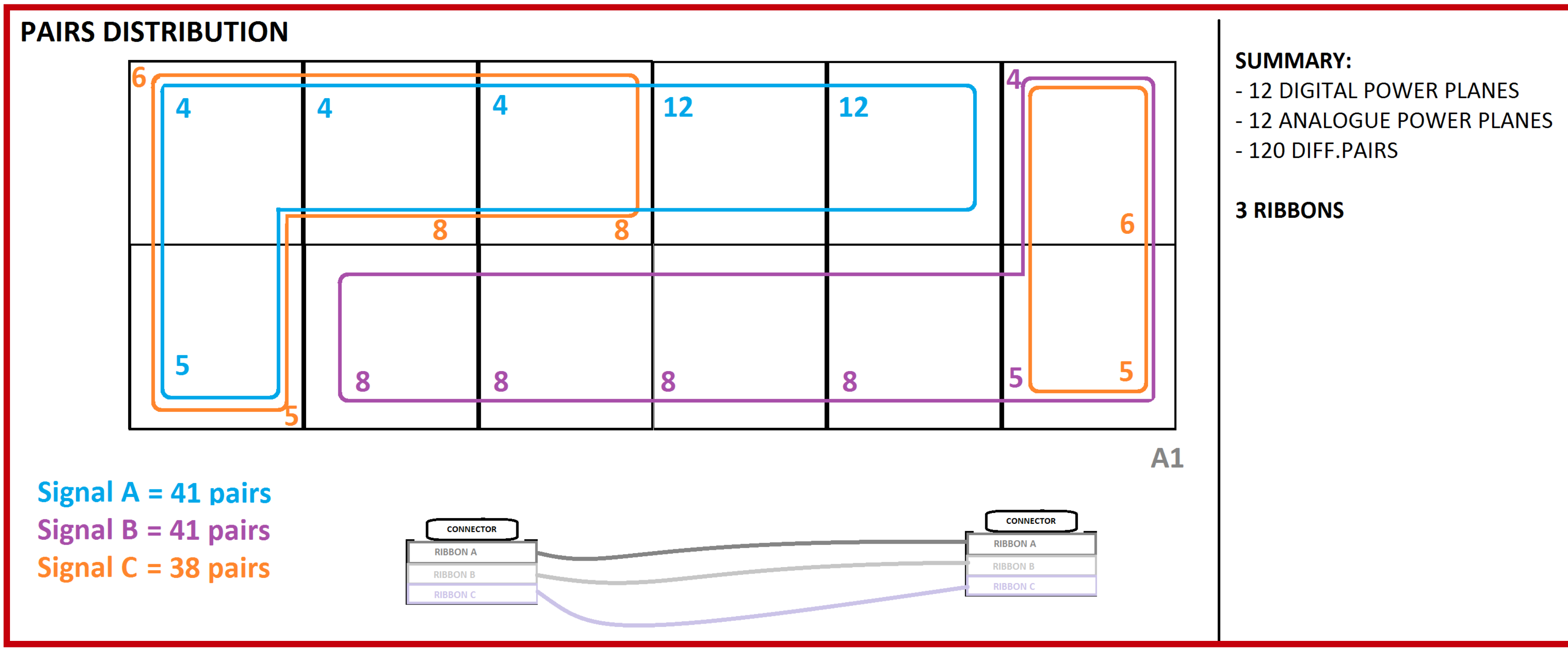
Layer Name	Type	Material	Thickness (mm)	Dielectric Material	Dielectric Constant	Pullback (mm)	Orientation
Top Overlay 1	Overlay						
Top Solder	Solder Mask/...	Surface Mat...	0.01016	Solder Resist	3.5		
Top Layer	**Power plane**	Copper	0.017				Top
kapton	Dielectric	Core	0.125		3.4		
Signal Layer 2	Signal	Copper	0.017				Not Allowed
kapton	Dielectric	Core	0.125		3.4		
Bottom Layer	**Power plane**	Copper	0.017				Bottom
Bottom Solder	Solder Mask/...	Surface Mat...	0.01016	Solder Resist	3.5		

Mechanical Mock-up

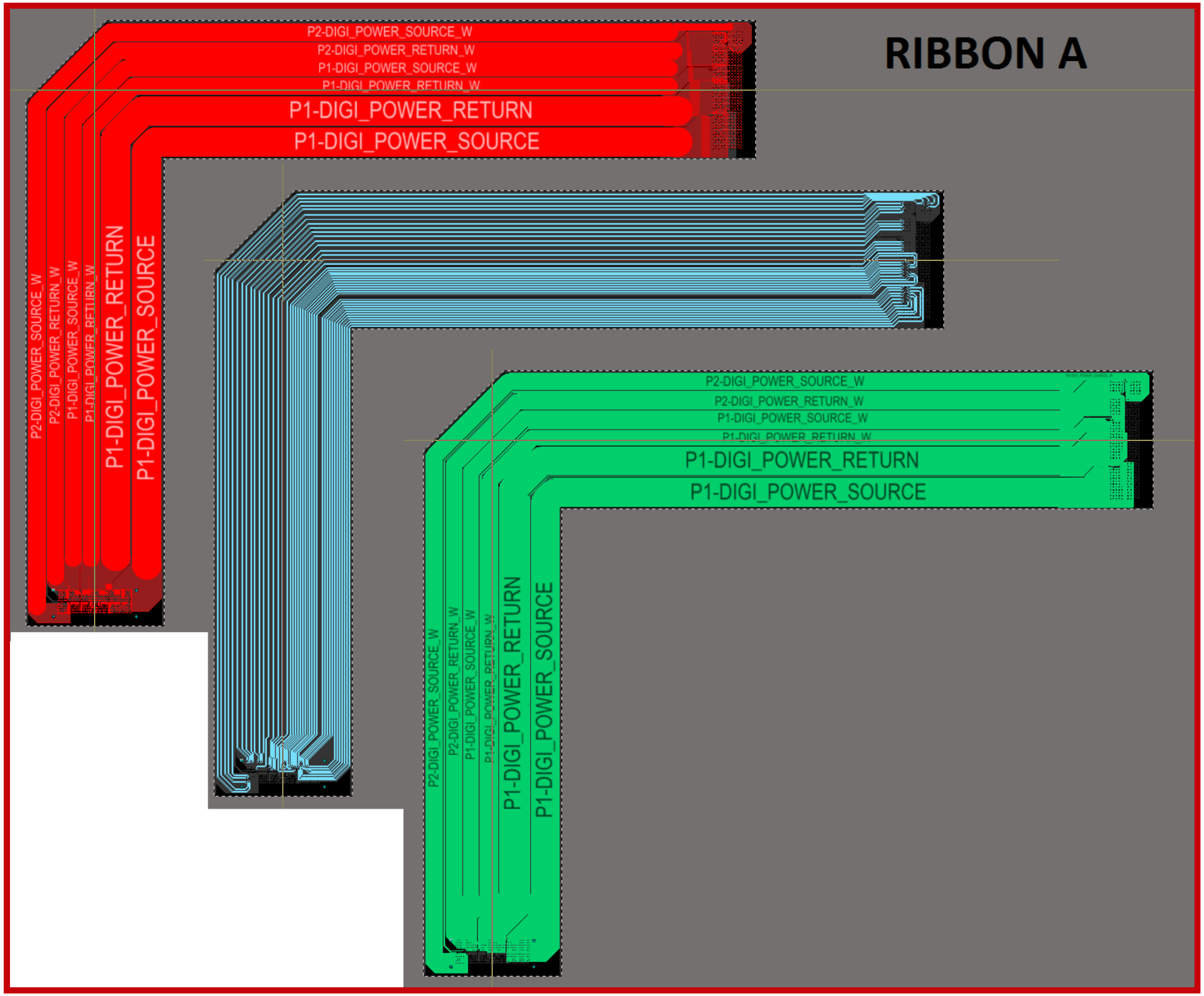


Last Pigtail Version

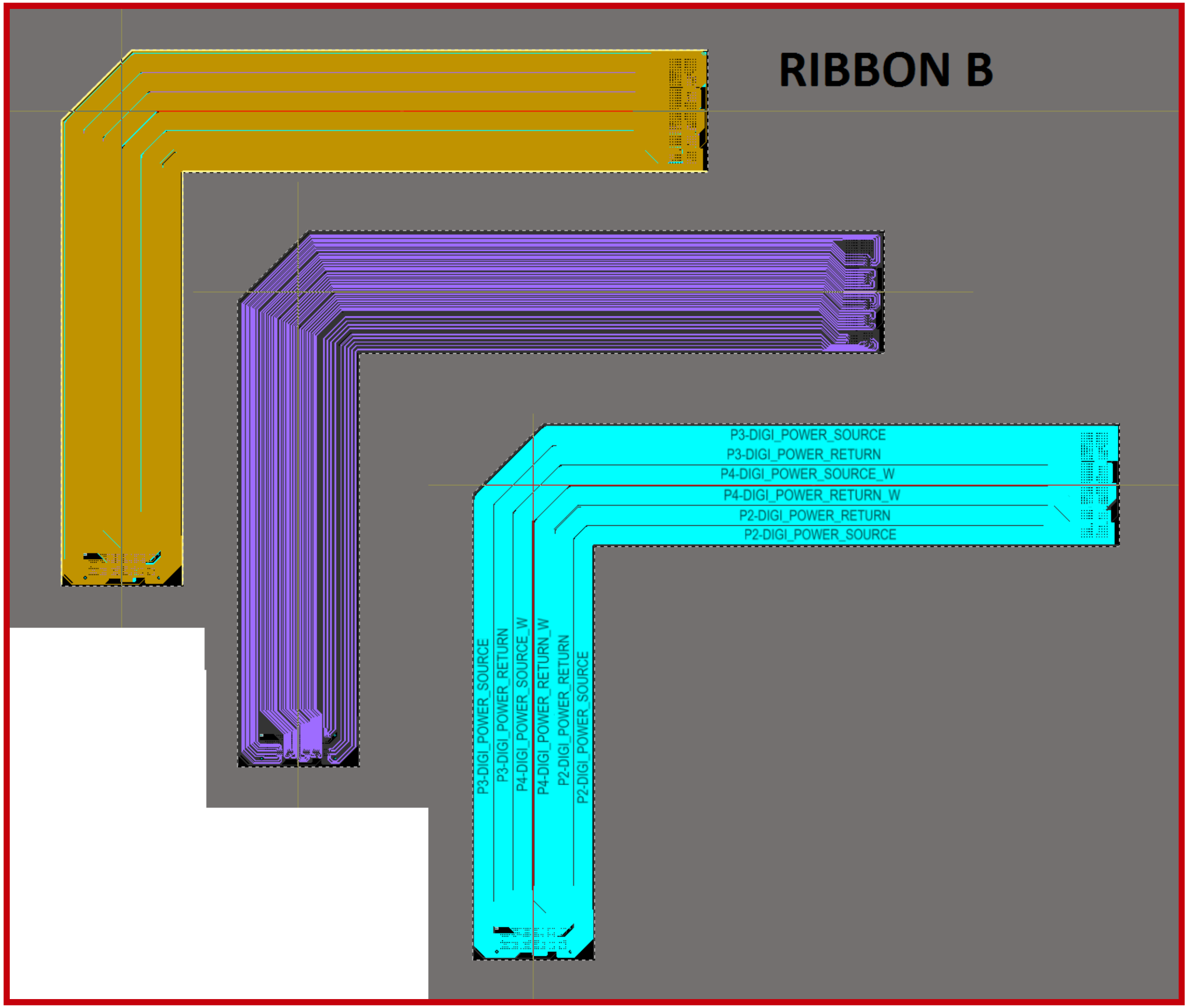
- Routing is finished.
- Distribution:



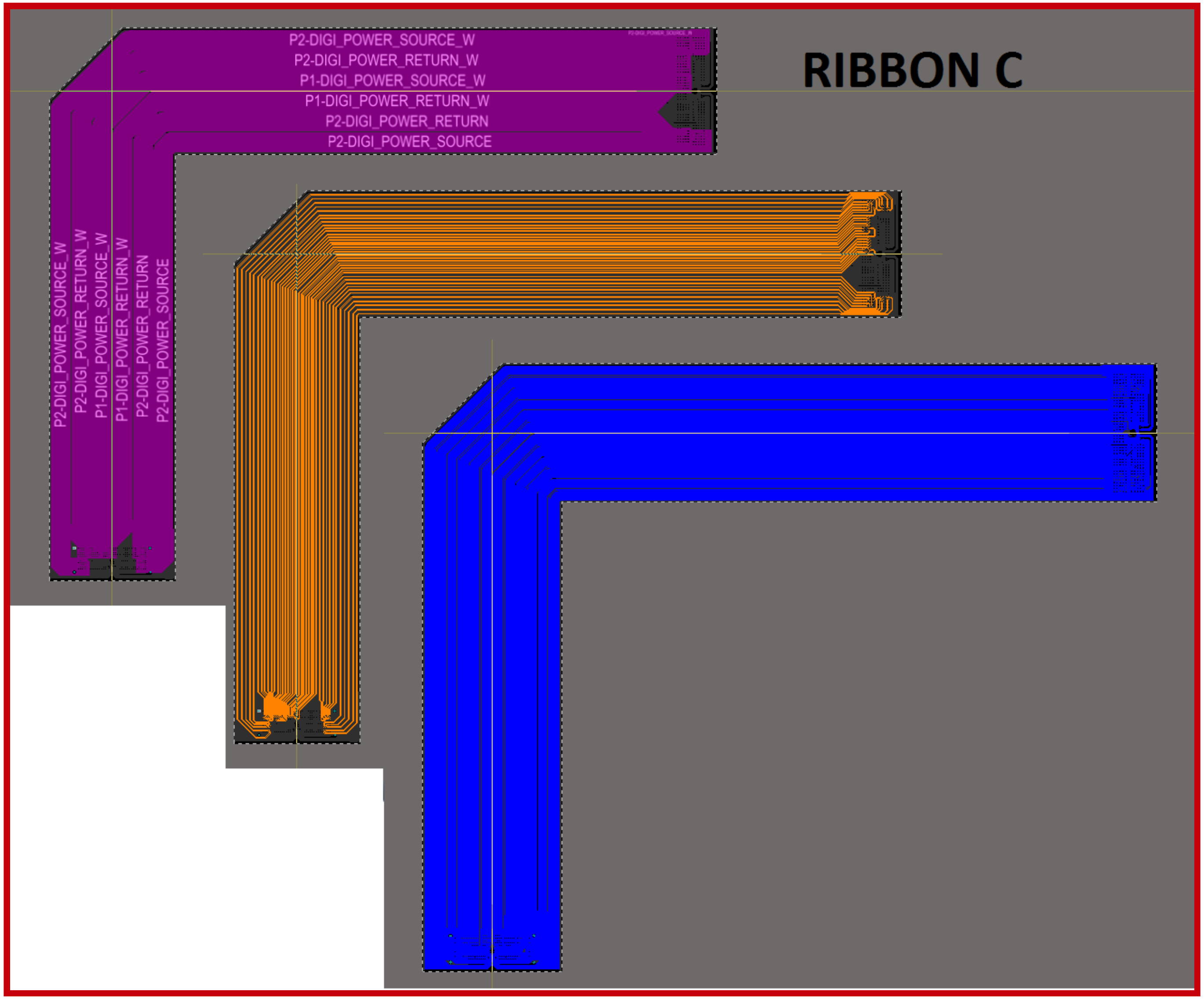
Last Pigtail Version



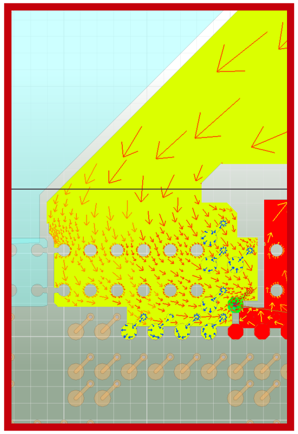
Last Pigtail Version



Last Pigtail Version



Last Pigtail Version



- Some simulations and results

RIBBON A	
	Ω (ohms)
DC RESISTANCE (roundtrip)	
P1 DIGI PWR	39.8m
P1 DIGI PWR_W	74.6m
P2 DIGI PWR_W	78.68m
Z.DIFF PAIRS	
W=109um	103.9
Sep= 235um	

RIBBON B	
DC RESISTANCE	
P2 DIGI PWR	57.28m
P3 DIGI PWR	61m
P4 DIGI PWR_W	58.28m
Z.DIFF PAIRS	
W=109um	103.9
Sep= 235um	

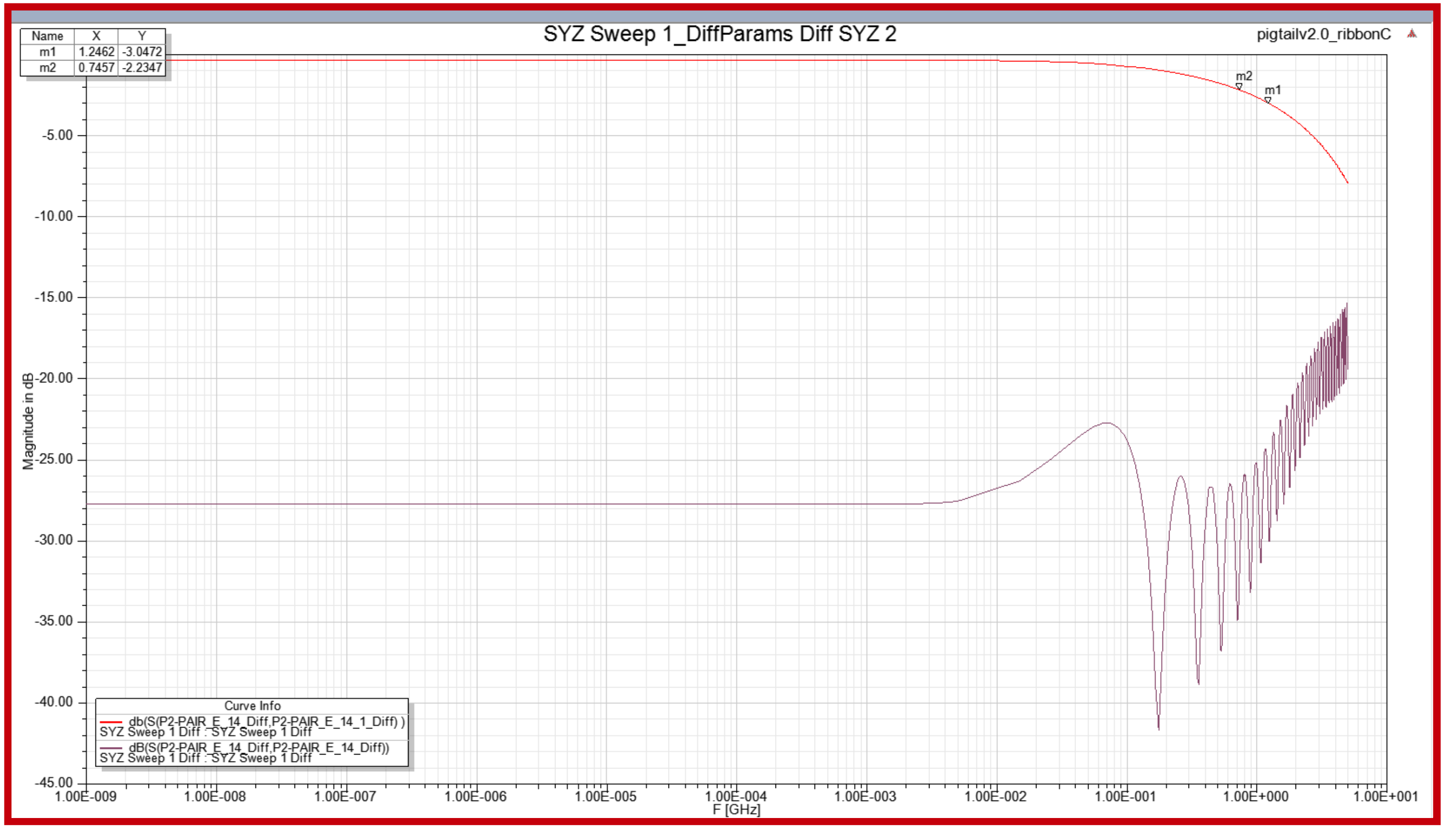
RIBBON C	
DC RESISTANCE	
P1 DIGI PWR_W	106.48m
P2 DIGI PWR	104.8m
P2 DIGI PWR_W	118.25m
P1 ANALOG PWR	245.88m
P1 ANALOG PWR_W	235.9m
P2 ANALOG PWR	299.4m
P2 ANALOG PWR_W	336.33m
P3 ANALOG PWR	316.22m
P4 ANALOG PWR_W	276.88m
Z.DIFF PAIRS	
W=109um	103.9
Sep= 235um	

Last Pigtail Version

- DC resistance for pairs: 5 ohms.
- Computed for the longest path 55cm, assuming rectangular section 17x109um (nominal values).

Last Pigtail Version

- **Simulated S parameters for one pair.**
- **-3dB → 1.24GHz**
- **-1.2dB → 300MHz**
- **Parameter S11 shows that most of the attenuation is not due to reflection.**



Future plans

- The routing is finished and the simulations give us reasonable results.
- Awaiting mechanical approval for submission.
- Cross-check between simulations and measures would be desirable.