Tests of SALT8b ASIC

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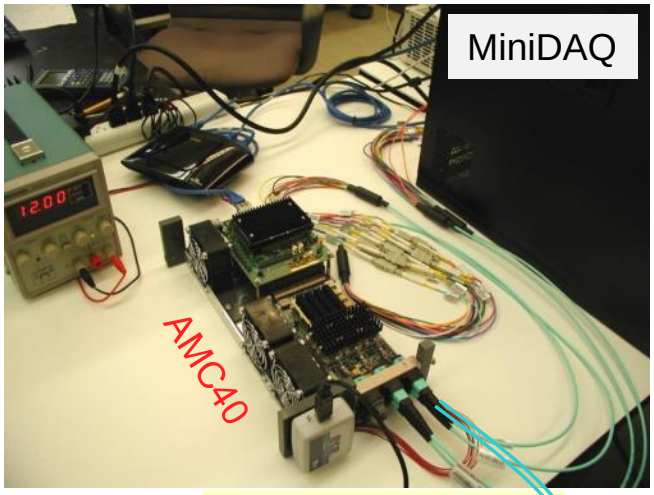
INFN Milano LHCb UT Workshop
May 17-19, 2016

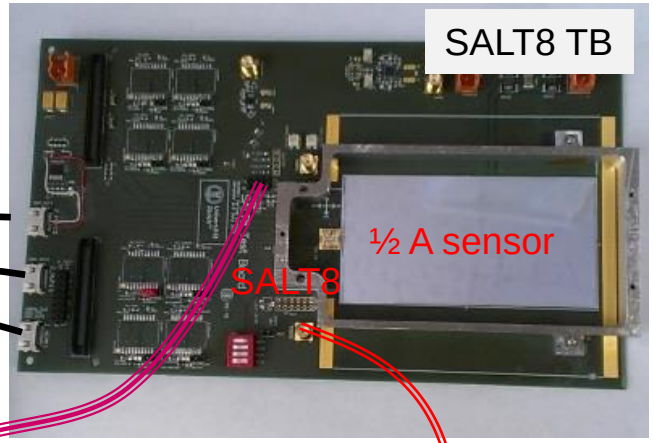
General Comments On SALT Tests

- Performance of SALT8a was already amazing, although a few issues were found.
- In SALT8b, most issues in SALT8a were fixed and verified in the tests.
- SALT128 has different event packet format and memory buffer design. Some issues in SALT8a/b related to these two become irrelevant in SALT128. But we study them very carefully anyway in case they lead to something critical.
- In SALT performance studies, besides of noise, gain, dynamic range, & uniformity etc, we pursue further in mainly two issues. One is the 2nd peak or shoulder in the pulse shape. The other is coupling between channels.

Test Setup & Information Flow

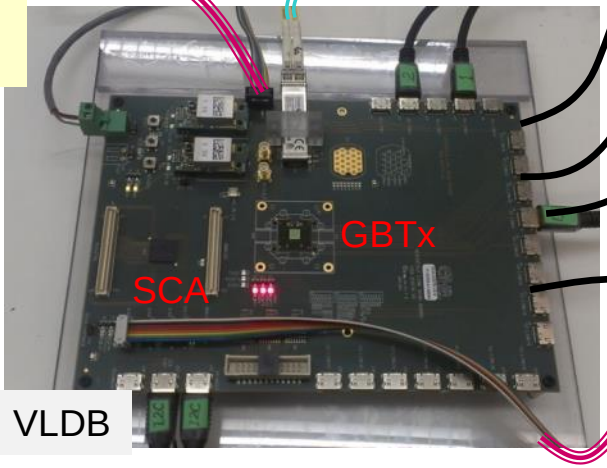


Mini-HDMI (320 Mbps)
1. Event data, CLK, TFC
2. Event data
3. Event data



GBT frame data
(TFC/ECS & event)

I²C signal to
config GBTx



VLDB

I²C signal to
config SALT8

Test pulse

12.5 ns NZS

LVDS-to-
LVCMOS

To synchronize
test pulse

Basic Communications

- The I^2C speed issue in SALT8a is fixed in SALT8b. The registers can be configured & read back using the USB-to-I2C adapter @100 kbps.
- All other tests are done with I^2C function in GBT-SCA.

- DLL adjustment agrees with expectation, same as in SALT8a.
- It is to adjust ADC phase so as to sample signal at the peak. As timing of test pulse & laser pulse are controlled through the waveform generator & FIFO delay, we use DLL to adjust the phase of output event data. In SALT128 there will be a designated register to take this duty.

- PLL works in both versions. TFC commands are decoded correctly, after phase & leading bit are properly adjusted.
- The TFC latencies are slightly modified in SALT8b, the measured delays agree with expectation from the designers.

Check Event Packet Formats

Packets	Format	BXID	Header Parity	Length	Length Parity	Data
Idle	✓	-	✓	-	-	-
HeaderOnly	✓	✓	✓	-	-	-
Truncation	✓	✓	✓	?	?(1)	-
Normal (2)	✓	✓	✓	✓	✓	✓
NZS	✓	✓	✓	✓	✓	✓(3)
Synch	✓	✓ (4)	✓			

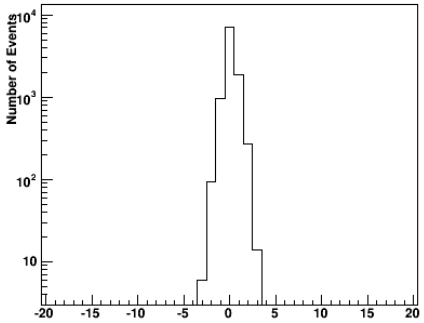
1) Length & parity bit in NZS truncation packet are wrong. They are generated from the ZS algorithm instead. There is also issues associated with the buffer after it is full once. BusyEvent ZS truncation does to present in SALT8.

2) Normal event packets are correct. It was not tested in SALT8a due to known issues.

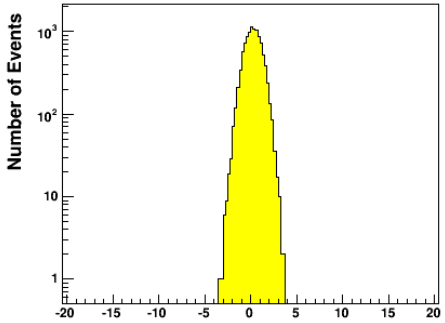
3) MCM & NumChan in CM calculation were not correct in SALT8a, & fixed in SALT8b.

4) BXID in Synch packet was off by 1 in SALT8a. It is corrected in SALT8b.

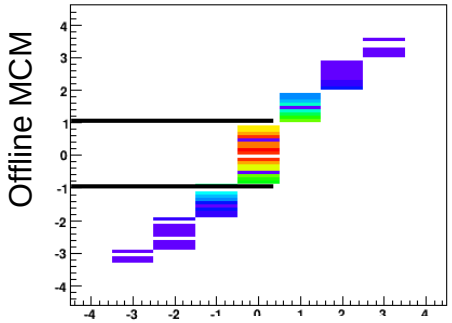
Mean Common Mode Calculation



SALT8b MCM

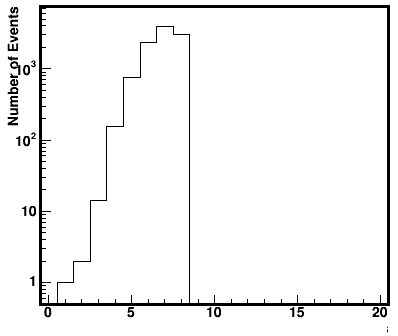


Offline MCM

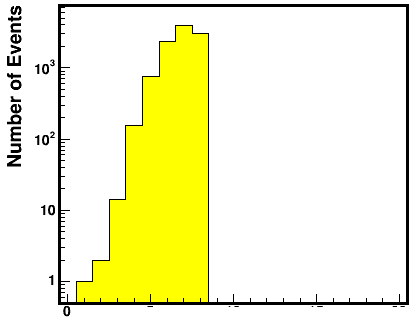


SALT8b MCM

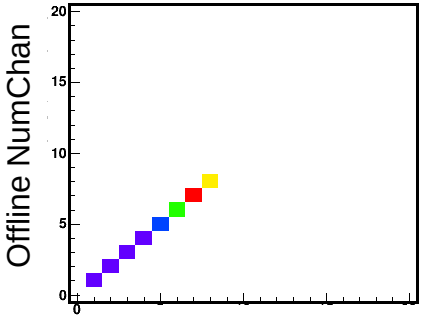
- NZS event packet includes mean common mode shift calculated by SALT8b & the number of channels used in the calculation.
- SALT8b is configured specially to achieve large MCM range or large NumChan range for test purpose.
- MCM & NumChan from offline calculation are consistent with SALT8b calculation.
- MCM is truncated in SALT8, it is better to be rounded if it is not difficult to do.
- MCM & NumChan each has 8 bits data including 1 parity bit, which is not necessary. We should remove it to accommodate NumChan=128.



SALT8b NumChan



Offline NumChan



SALT8b NumChan

A Few Minor Issues

1) SALT8b responds to Synch, BxVeto, NZS, & HeaderOnly commands correctly.

7	6	5	4	3	2	1	0
~~Calib~~	Synch	~~Snapshot~~	BxVeto	NZS	HeaderOnly	~~FEReset~~	BXReset

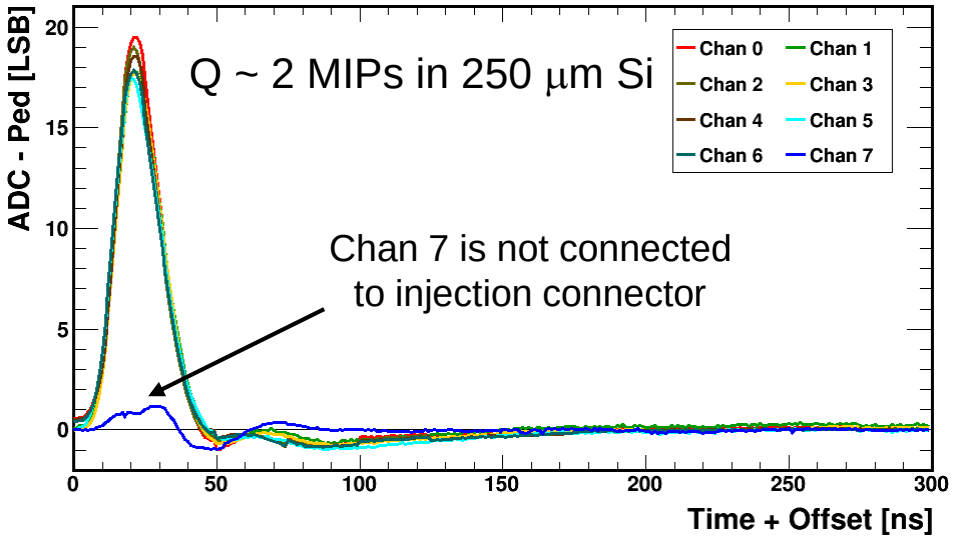
To BXReset SALT8b generates BXID = 0xFFF instead of 0, which will be fixed.

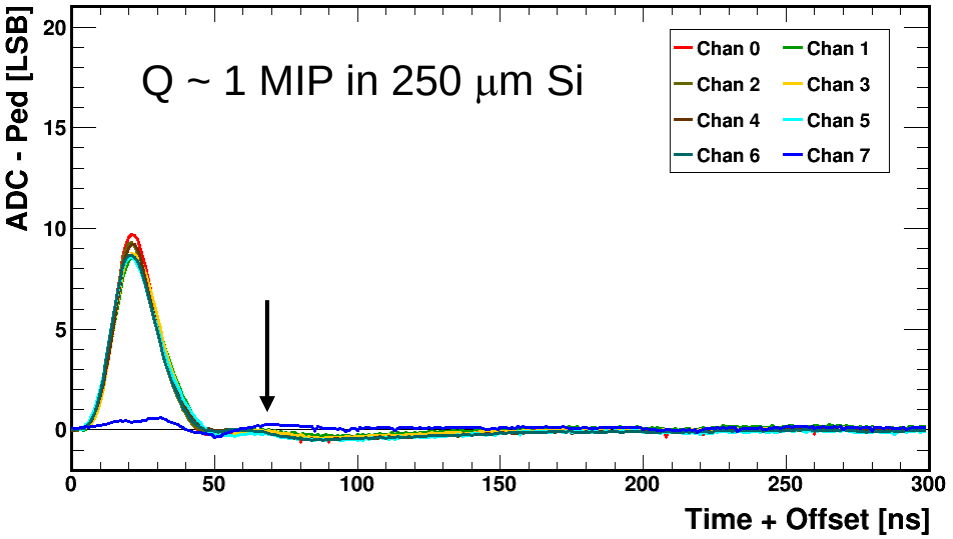
2) ADC behaves abnormally in ch 0,1,4,5 @ value ~ –15, when ADC operates at the default adc_internal_delay=0. Problem disappear when delay is large.

3) SALT8 buffer size is 128 bytes. The ASIC generates truncation packet when buffer is full. The data exhibits issues on certain conditions. For SALT128 the buffer design is totally defferent.

4) In a specially mode (nzs_sel = 01) raw ADCs are supposed to be the output while a few channels are masked. Instead the masked signals are output.

Pulse Shape From Test Pulse Calibration

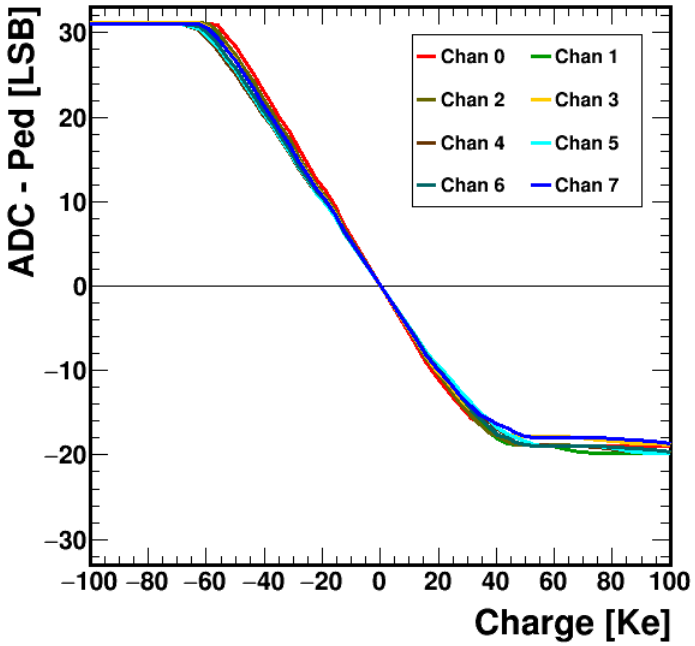




- Inject test pulses to ch 0, 2, 4, & 6, or ch 1, 3 & 5, one group at a time.
- In SALT8a we observed a 2nd peak or shoulder at ~ T_{peak} + 50 ns.
- It could be due to power routine layout (found by Krakow group).
- It is expected that with 1 MIP the shoulder is much smaller.

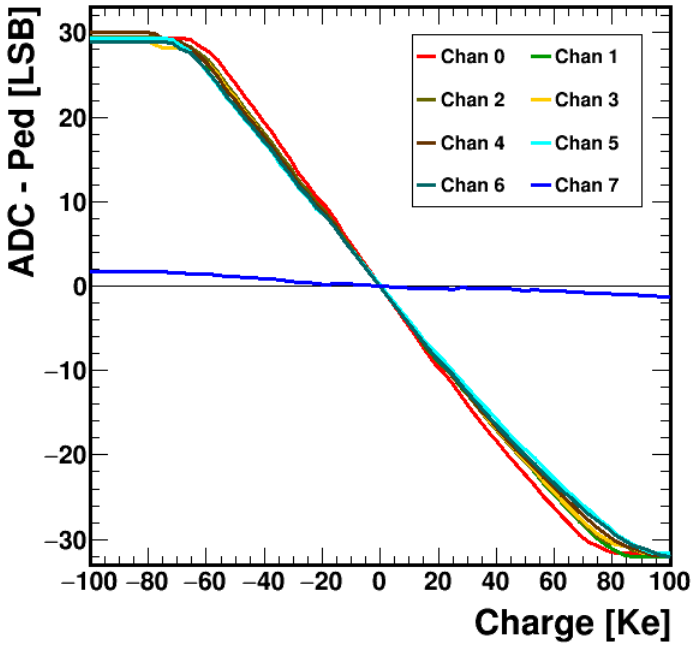
Gain Curve

SALT8a



It saturates earlier with positive charge.

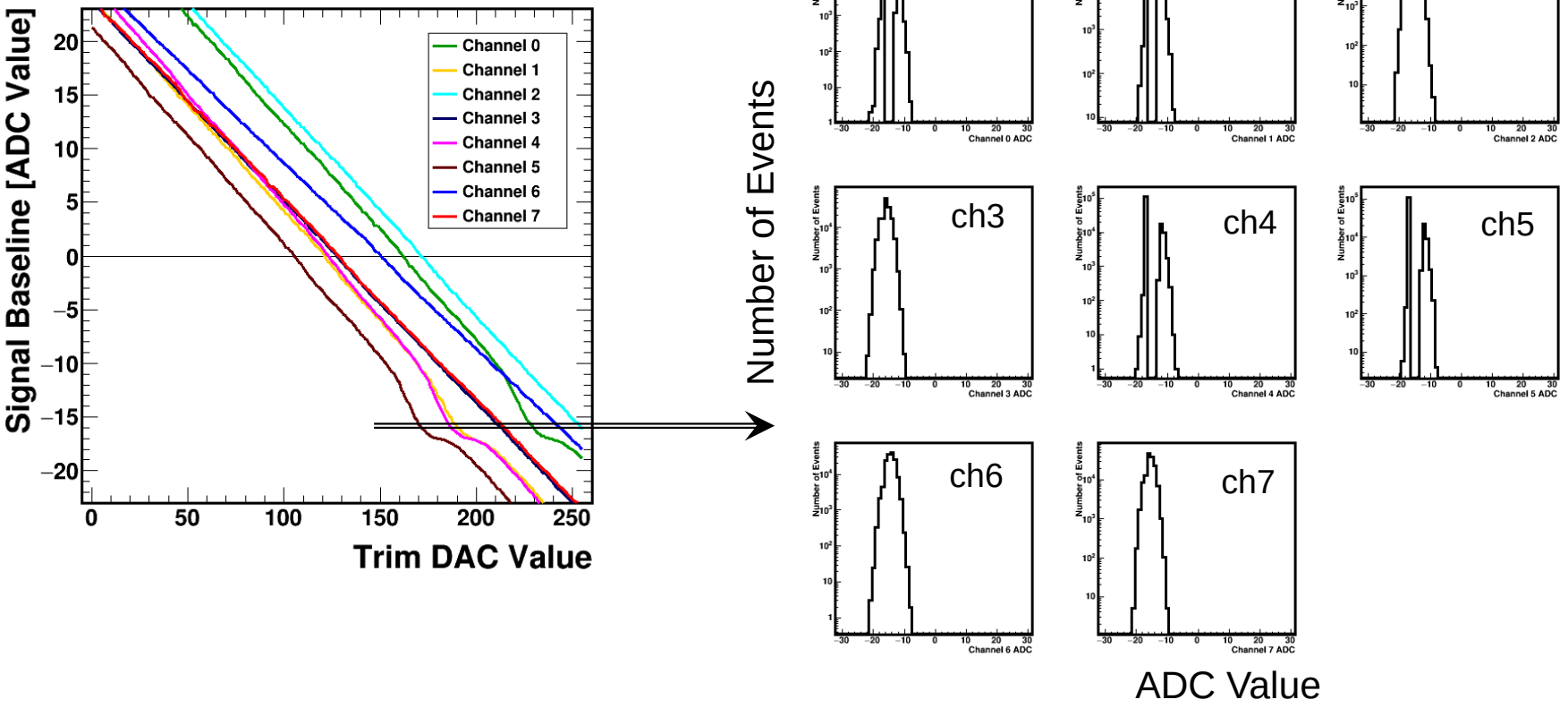
SALT8b



The gain curve is symmetric.

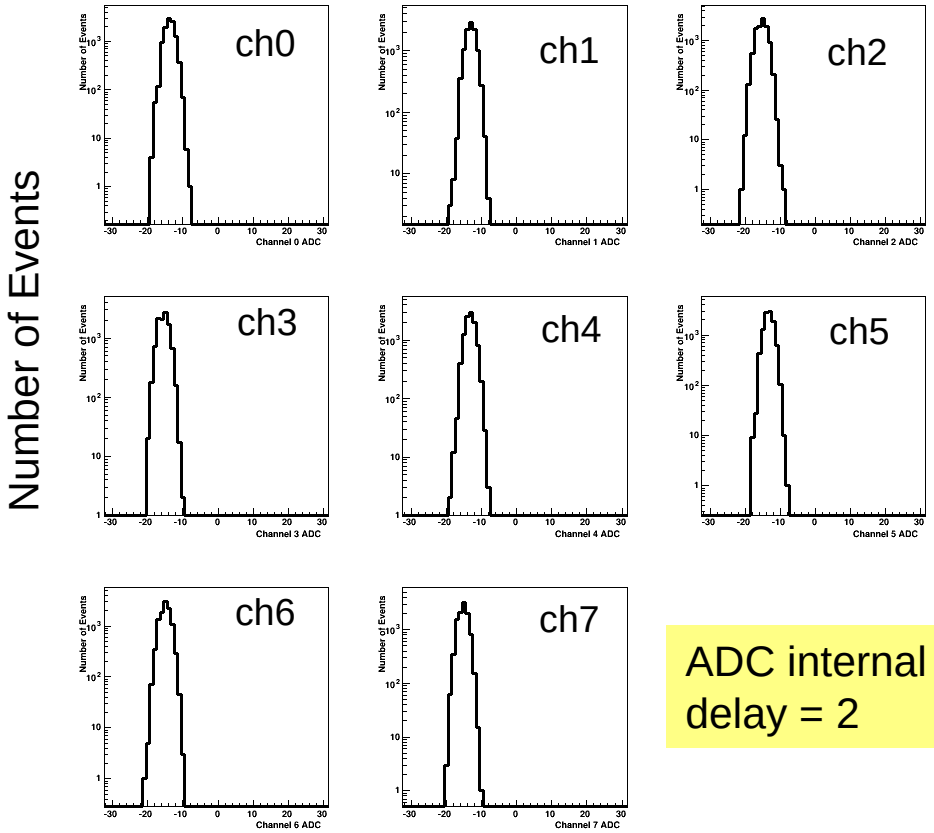
ADC Issue (I)

- With default setting we observed abnormal ADC behavior at ADC ~ -15 in pulse shape calibration & trim DAC scan.
- It is clear in the 2x gain trim DAC scan with large noise.
- It only happens in channels 0, 1, 4, & 5 that there are gaps of ADC = -14, -15, -16.



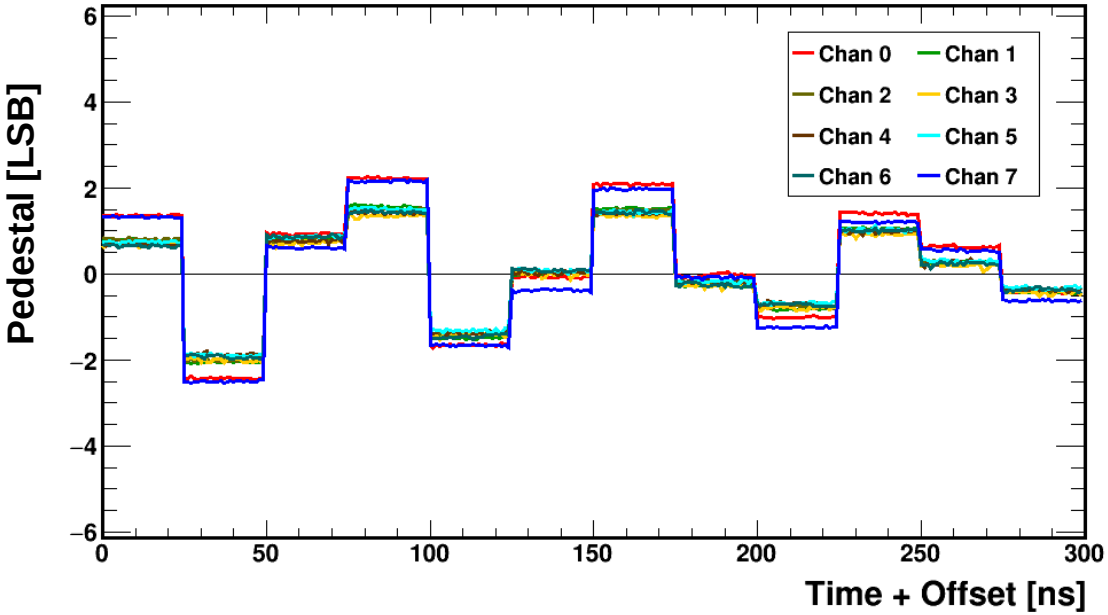
ADC Issue (II)

- It is found that “ADC internal delay” changes this behavior. The default value is 0. When the value is changed to 1-7, ADC acts normally.
- Marek confirmed that “in channels 0,1,4,5 we have slightly slower comparator than in other 4 channels”. However, “it is a bit strange that you see it only for negative baseline”
- We change ADC internal delay default value to 2.



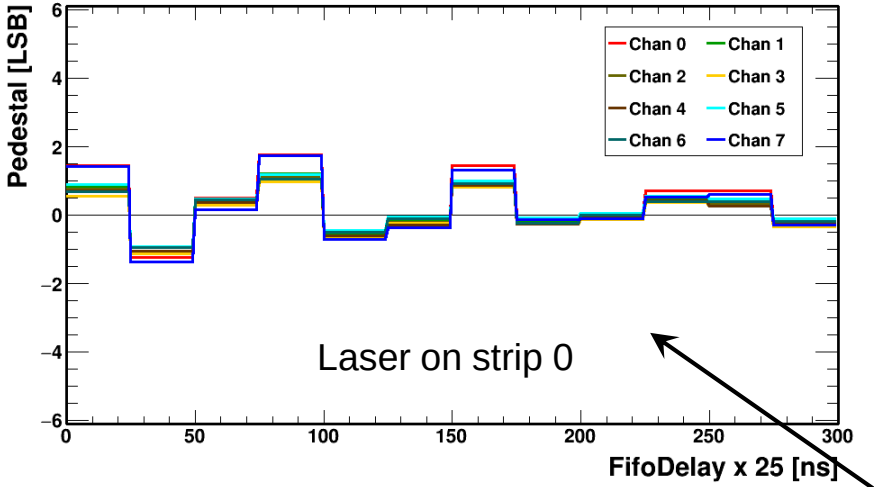
ADC internal delay = 2

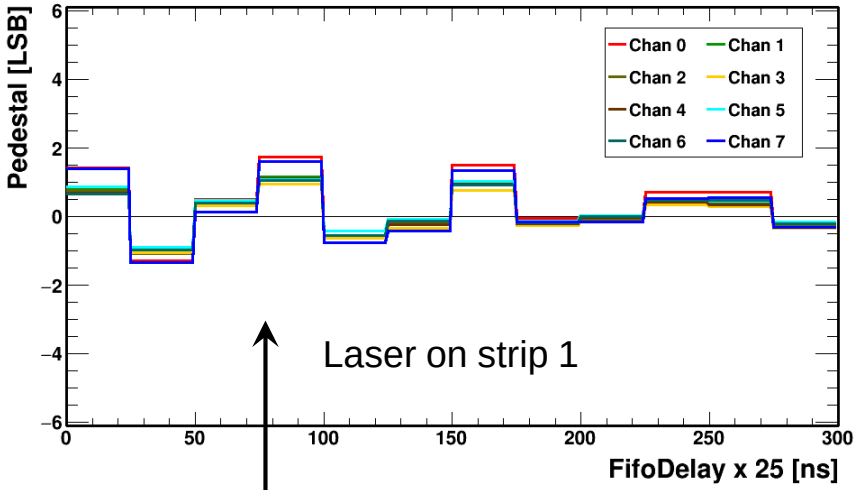
Pedestal for Different FIFO Delays (I)



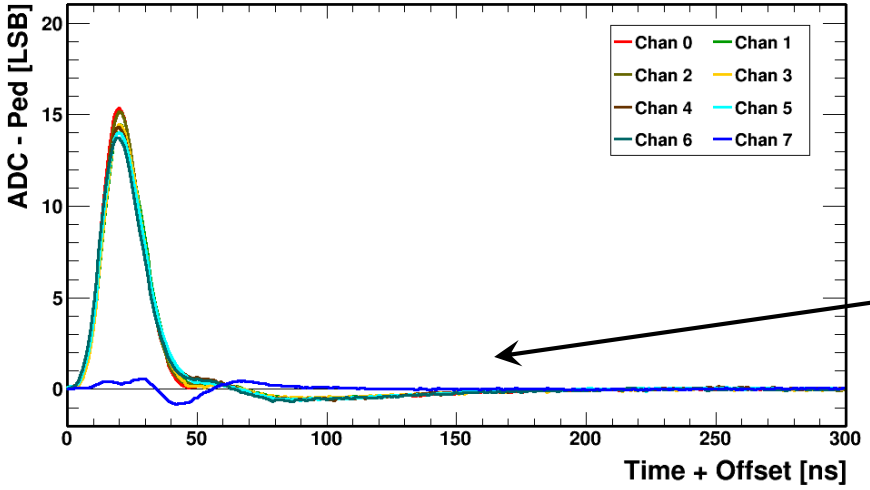
- Pulse shape calibration is done with FIFO delay (25 ns step), & 25 wave forms (for 0-24 ns in 1ns step).
- In setup that was prepared for laser test, where cables are long (~1.8m HDMI cable & I2C cable). We found that pedestal changed for different FIFO delay.
- In normal data taking the FIFO delay is fixed. Thus this is not a problem. However, I am still curious on the source.
- It seems very significant when the cables are short. We will try to reproduce with long cables on SALT8a or SALT8b.

Pedestal for Different FIFO Delays (II)



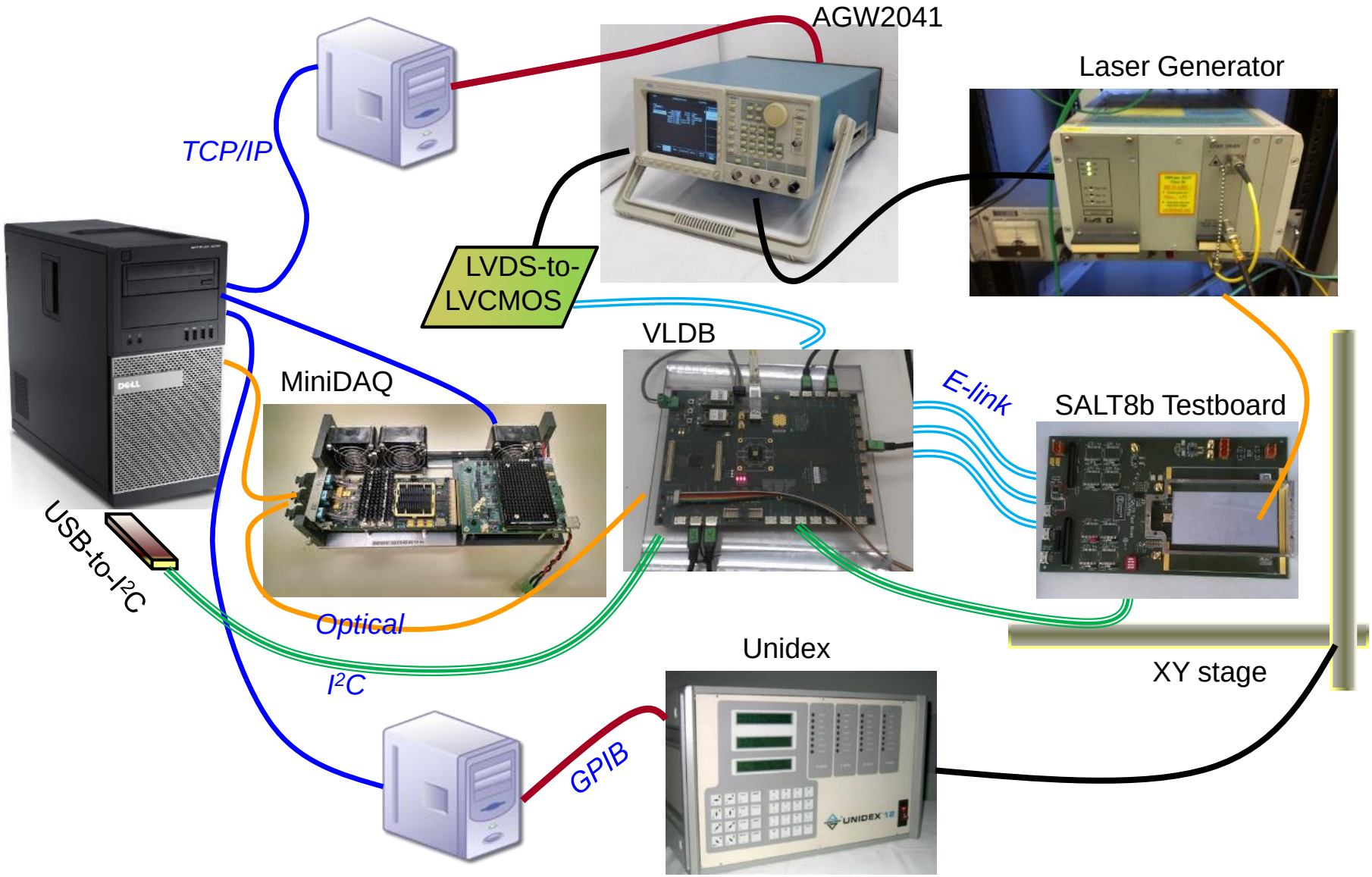


Changes are consistent at different runs for the same physical setting.



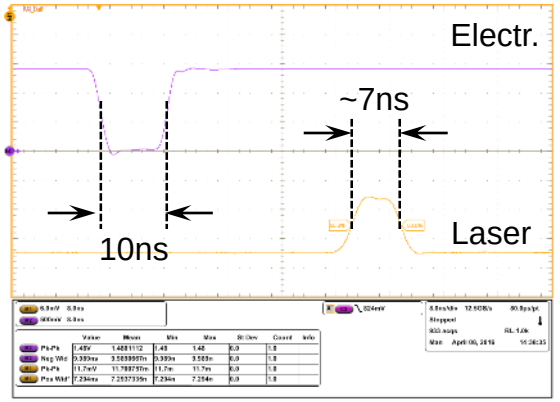
Changes are insignificant for the same SALT8b & TB board, with shorter cables.

System Configuration For Laser Test

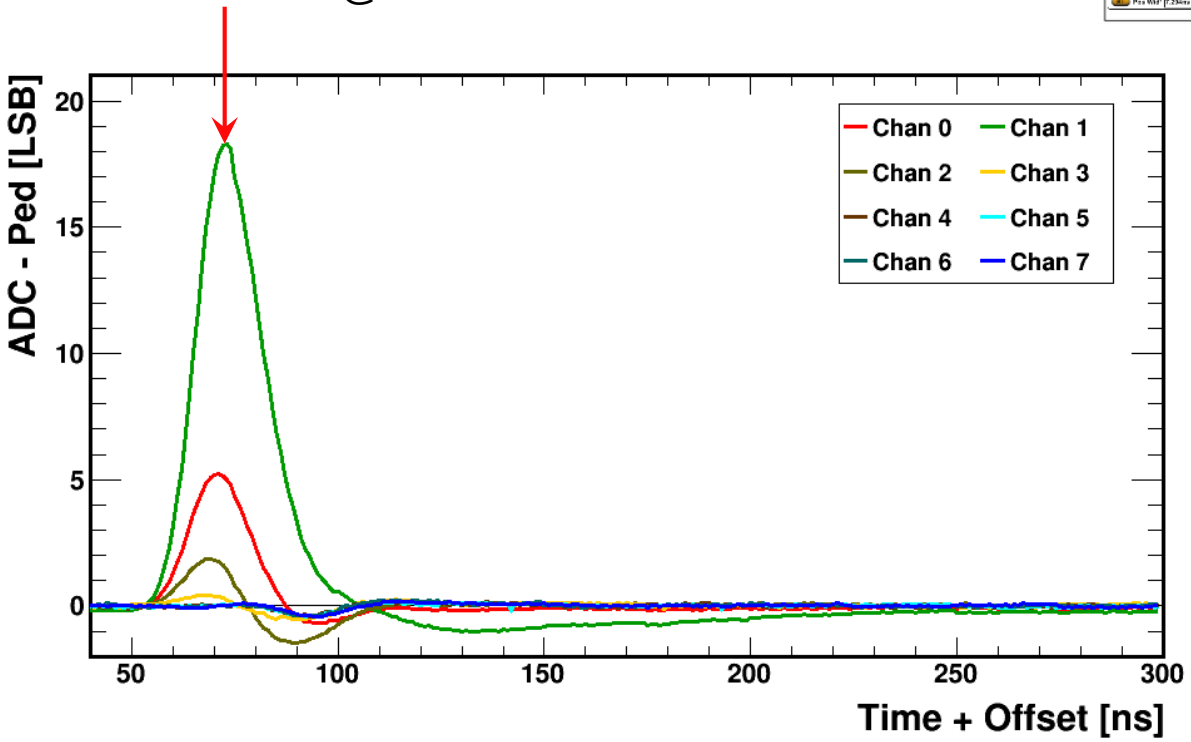


Cross Strip Laser Scan

- Inject pulse to laser generator of width ~10 ns, height 1.3V, 1.56V. Output width ~ 7 ns, energy deposition ~ 1 & 2 MIPs.
- Focused laser beam, spot size ~ 10 μm.

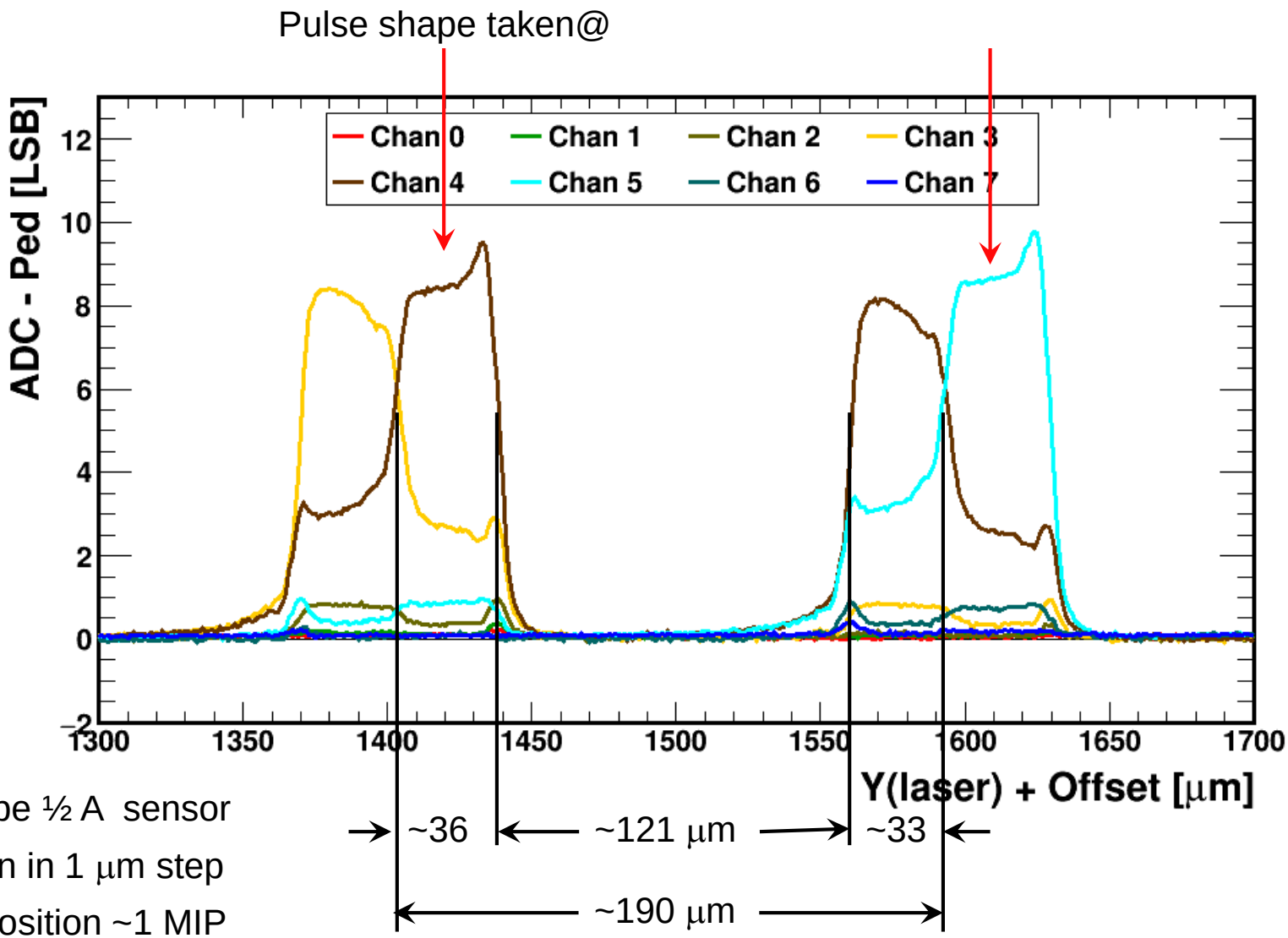


Y scan taken @ 72 ns



Laser is centered on strip 1, ~20 μm from border between strips 0 & 1

Laser Scan Across Strips

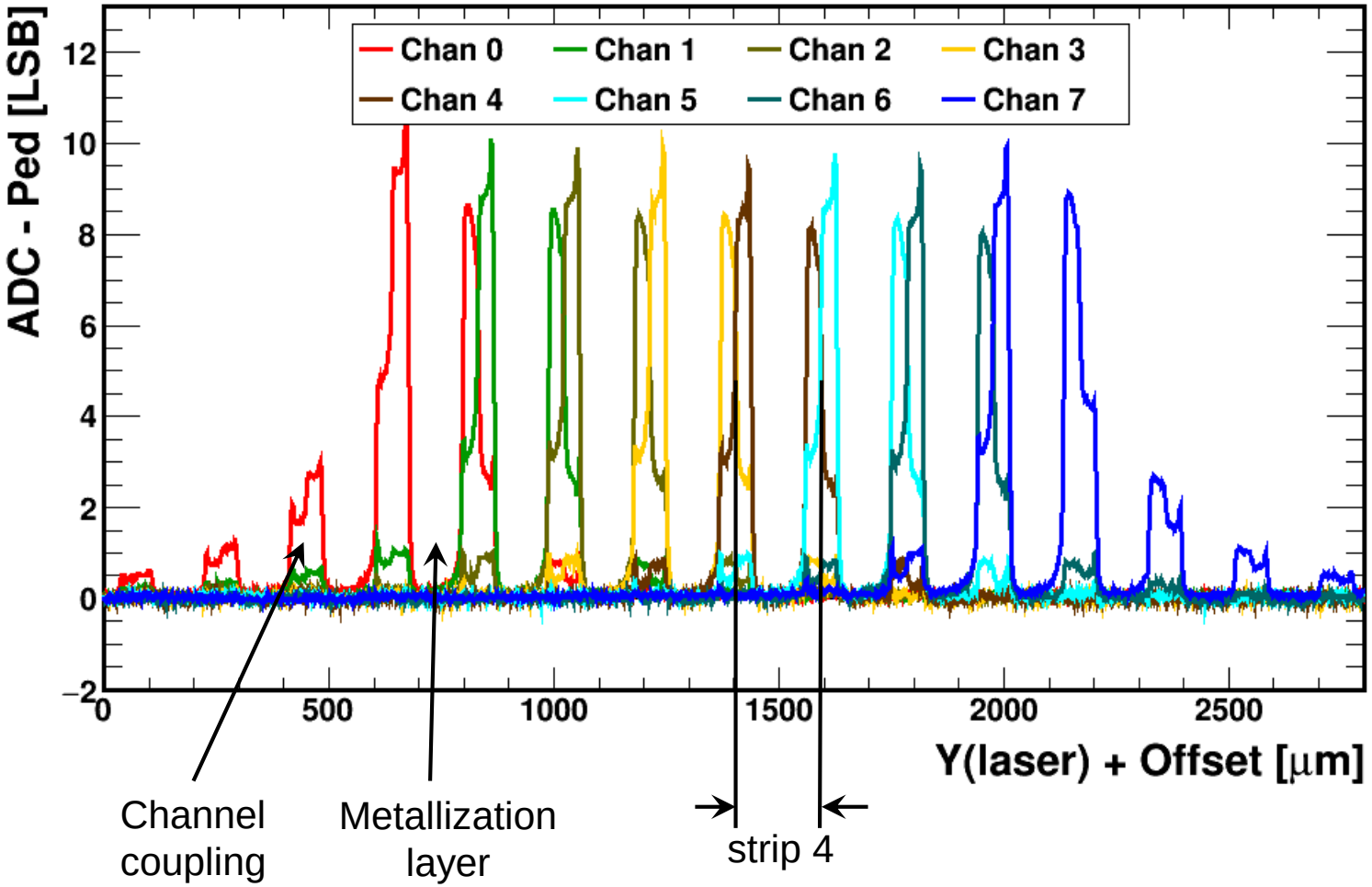


P-type ½ A sensor

Scan in 1 μm step

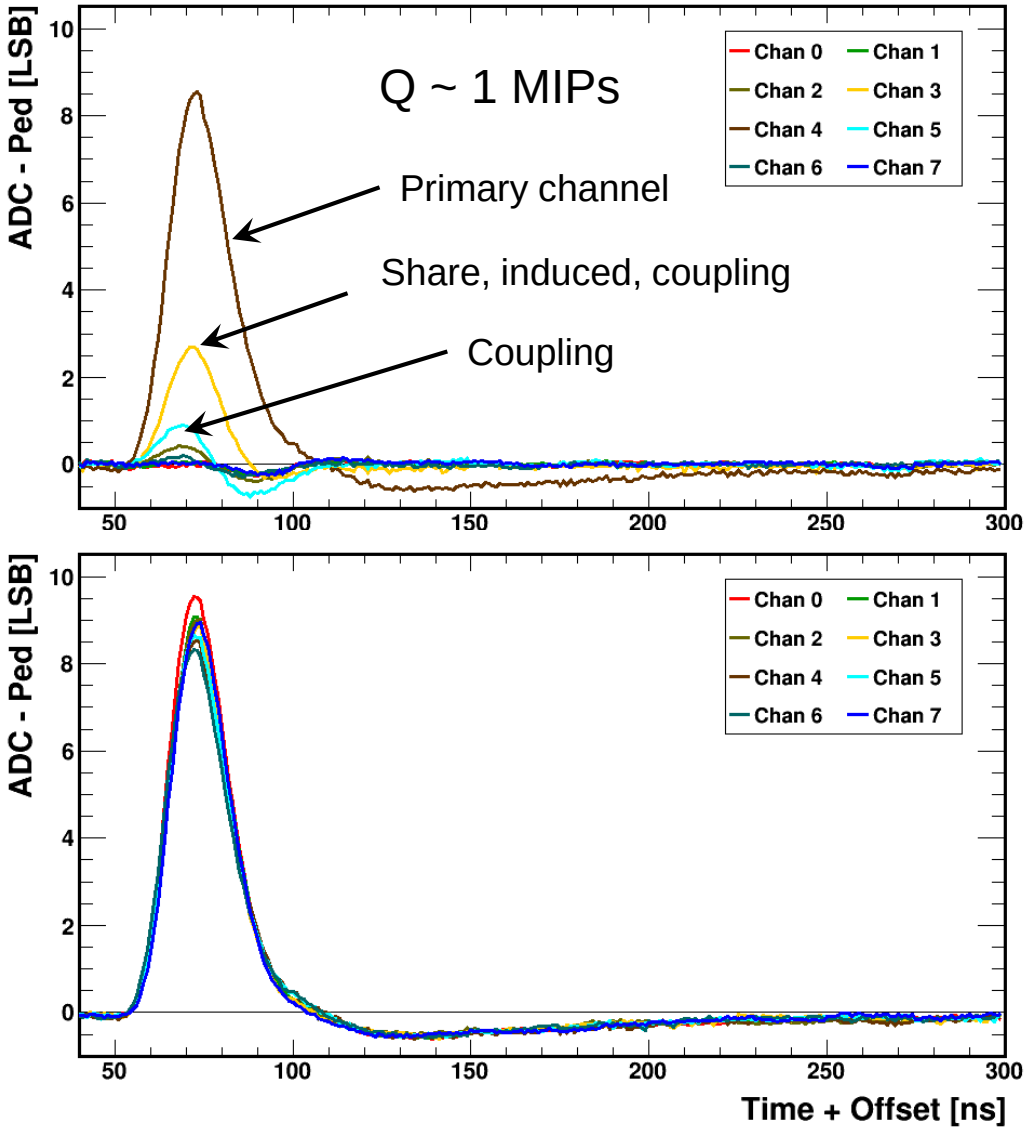
Deposition ~1 MIP

Laser Scan Across Strips (Zoom Out)



Difference of same edges: 190.0-190.9 μm

Pulse Shape Using Laser Source



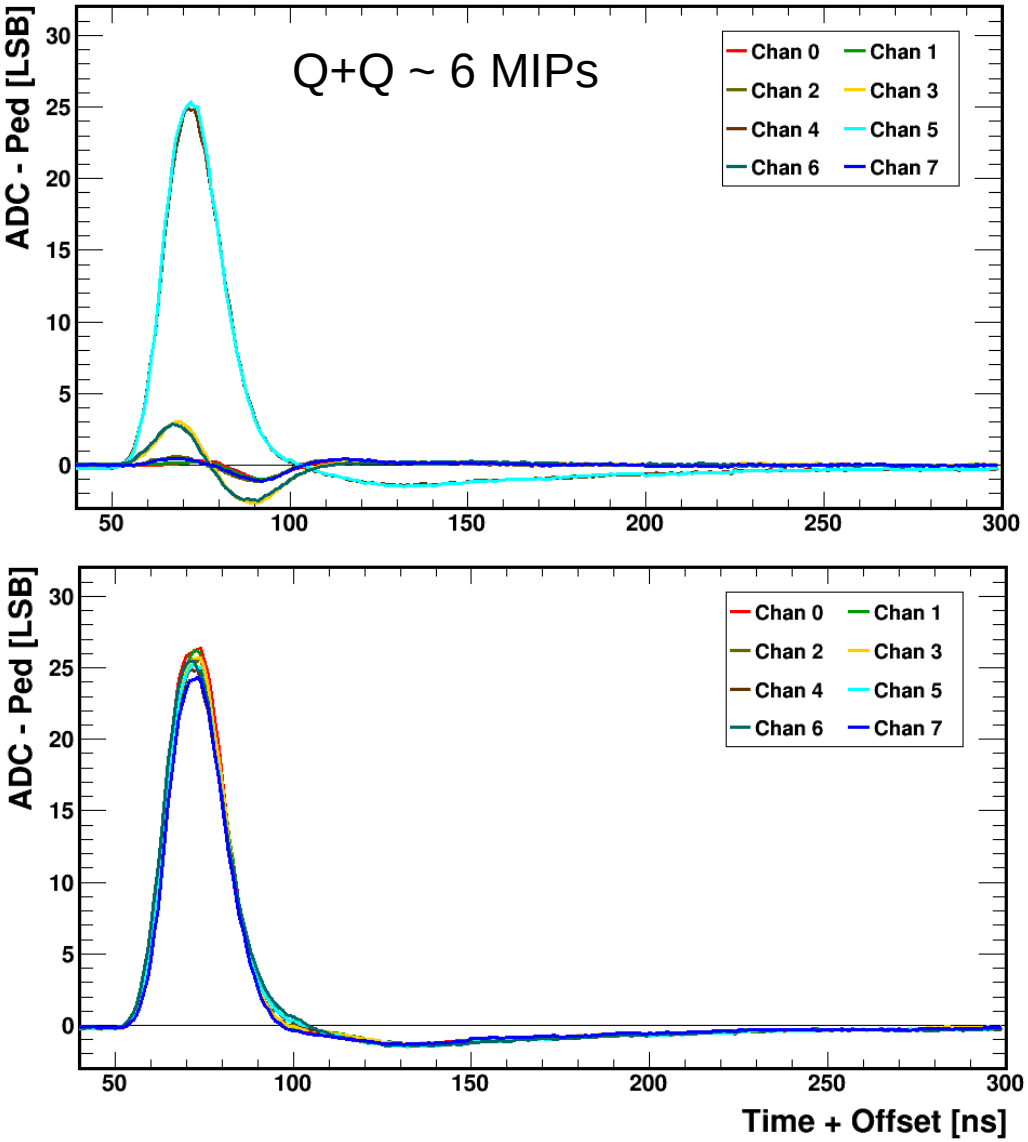
Laser beam of ~7 ns width.

The laser beam is centered on strip n, ~20 μm from the border of strips n-1 & n (n=4 in this plot).

In each of 8 runs, laser beam is centered on strips one by one.

Collection of pulse shapes from all channels that are hit by laser beam in each run.

Pulse Shape of Larger Charge



Laser beam is tuned to be a little bit wider.

Laser beam is centered at a border of adjacent channels. Both channels have similar amount of energy deposition. And the ADCs are not saturated.

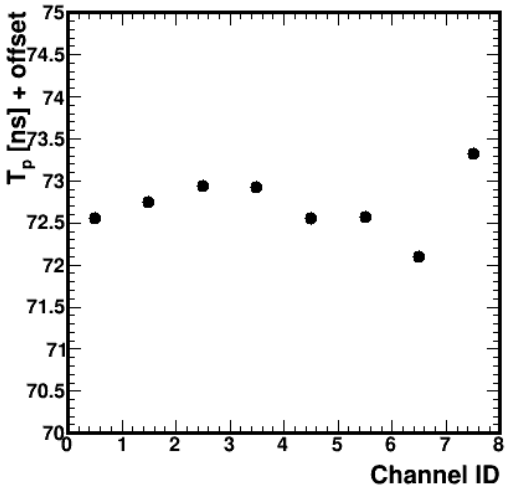
Total energy deposited ~ 6 MIPs.

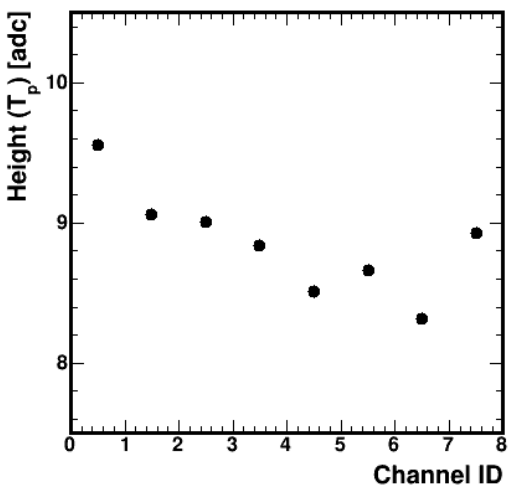
We want to see if the effect of 2nd peak / shoulder is more significant.

It is really difficult to say that the effect is stronger.

Comparison of 8 Channels In Laser Test

Peaking time uniformity is reasonable

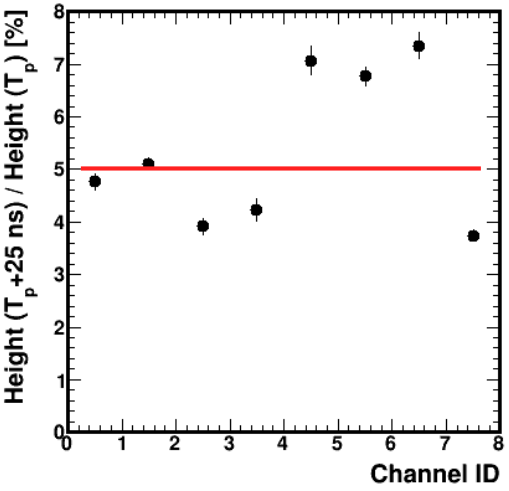


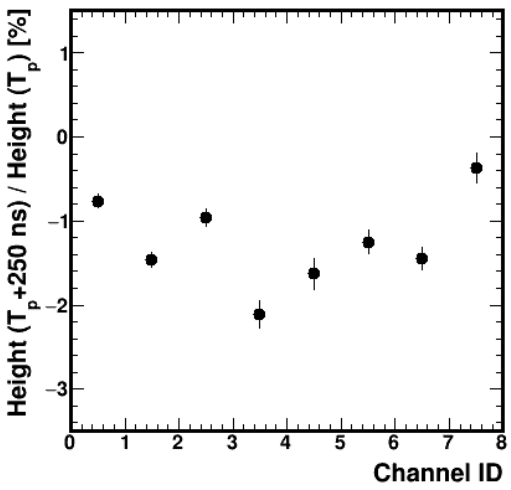


Q ~ 1 MIPs

Non-uniformity also comes from test setup

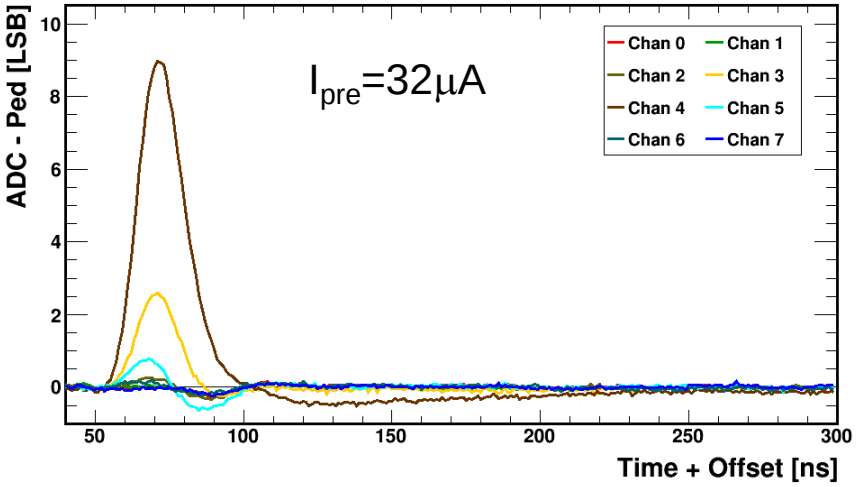
Contribute to spill over

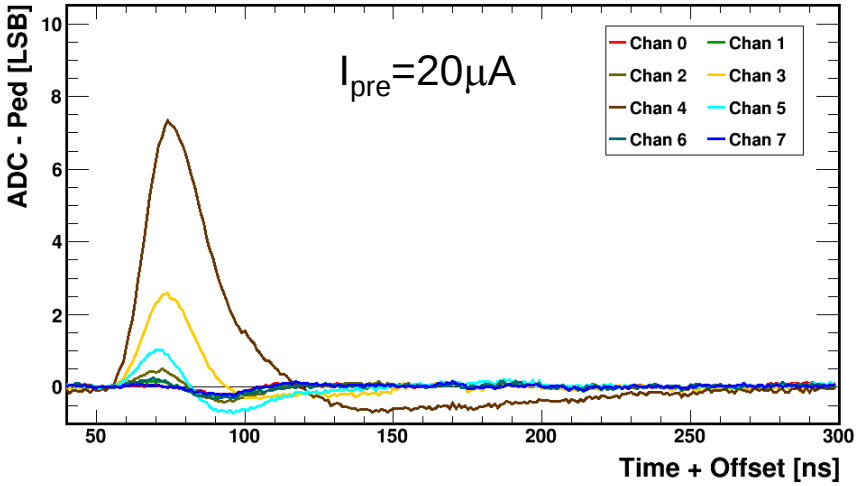


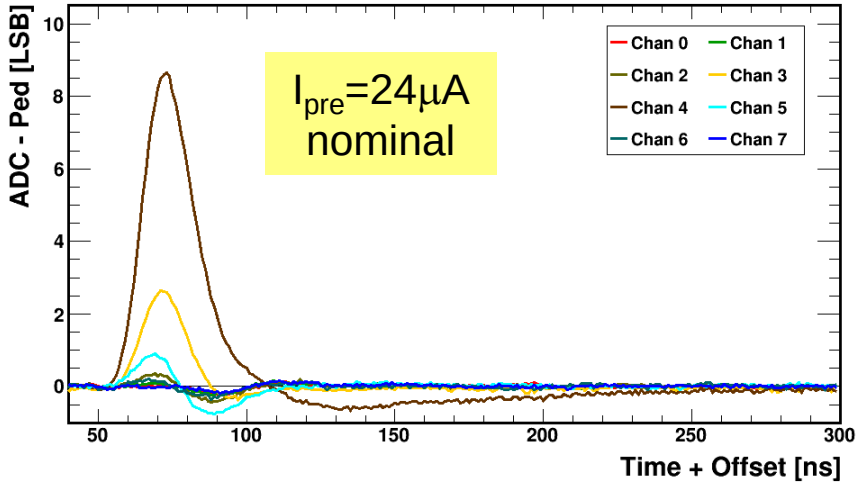


Long term return, Undershoot may need to be reduced

Preamplifier Biasing vs Coupling





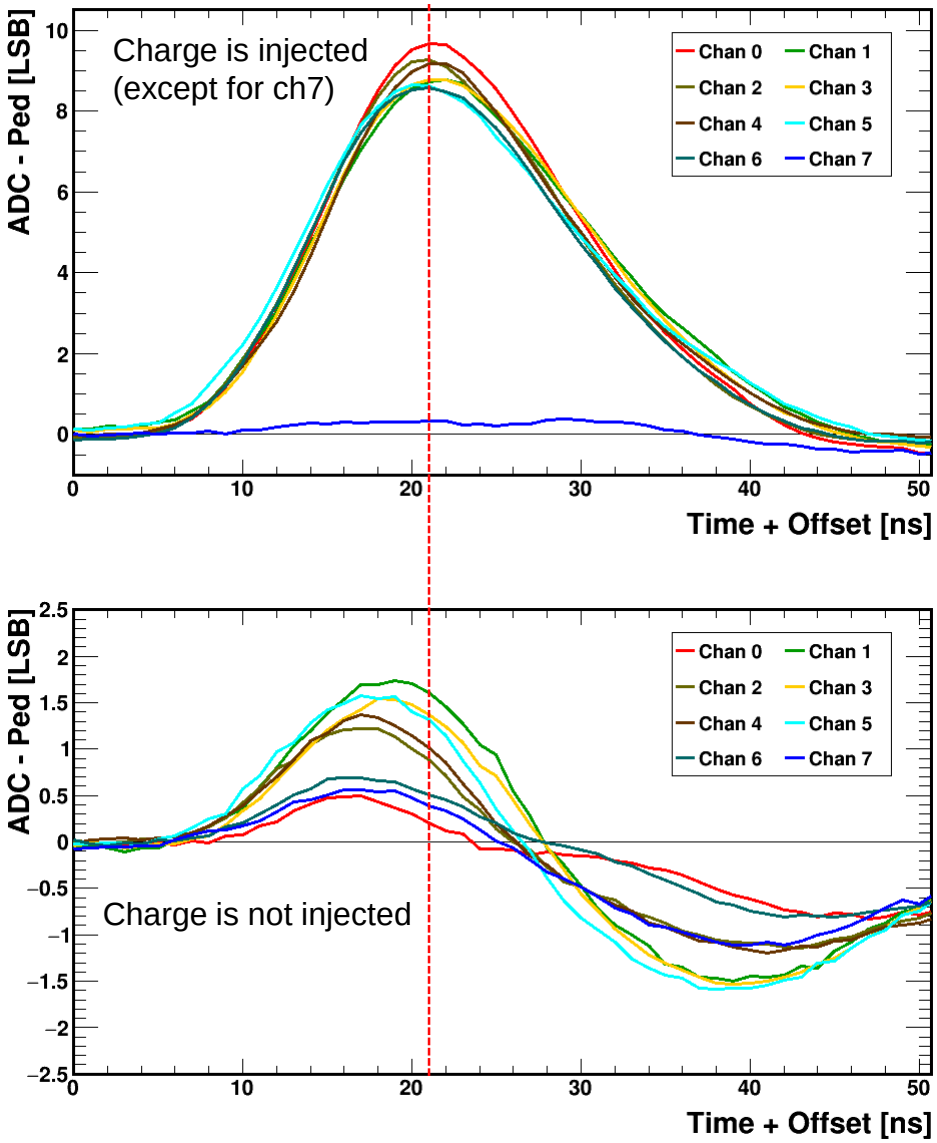


Laser beam is centered on strip/channel 4, ~20 μm away from border of strips 3 & 4.

Preamplifer Bias (μA)	At peak of normal signal		
	Chan 4	Chan 5	Rate (5/4)
32	8.97	0.64	7.1%
24	8.65	0.68	7.9%
20	7.23	0.79	10.9%

Simulation ⇒ ~ 6 – 6.6 %

Coupling From Charge Injection Test



Chn	Q to Test0 ADC	Ratio	Q to Test1 ADC	Ratio
0	9.66		0.21	2.4%
1	1.61	8.5%	8.73	
2	9.28		0.89	5.1%
3	1.37	7.4%	8.78	
4	9.16		1.02	5.9%
5	1.32	7.4%	8.62	
6	8.58		0.51	5.7%
7	0.39	4.5%	0.34	

Ratio = ADC_n / (ADC_{n+1}+ ADC_{n-1})

From laser test we know that there may be coupling for non-adjacent channels too. This may explain why the ratio is lower when inject to test1 (3 channels instead of 4)

Look Into Near Future

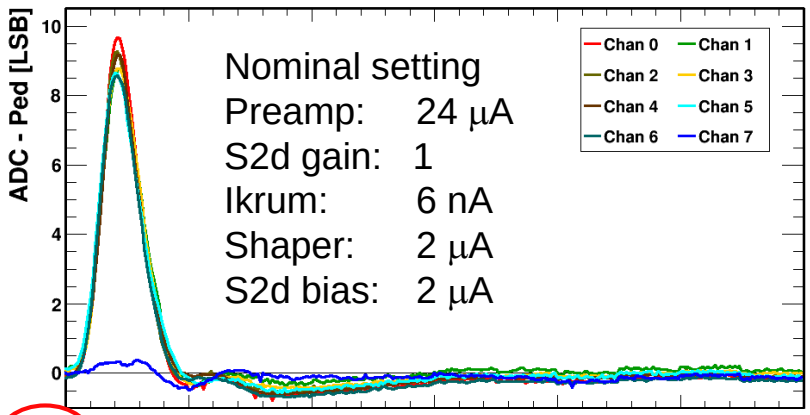
- SALT128 test is similar to SALT8a/b for basic functionalities.
- We will form a test procedure, which can be tailored for SALT production test. Of course scanning of all digital gates is a totally different test.

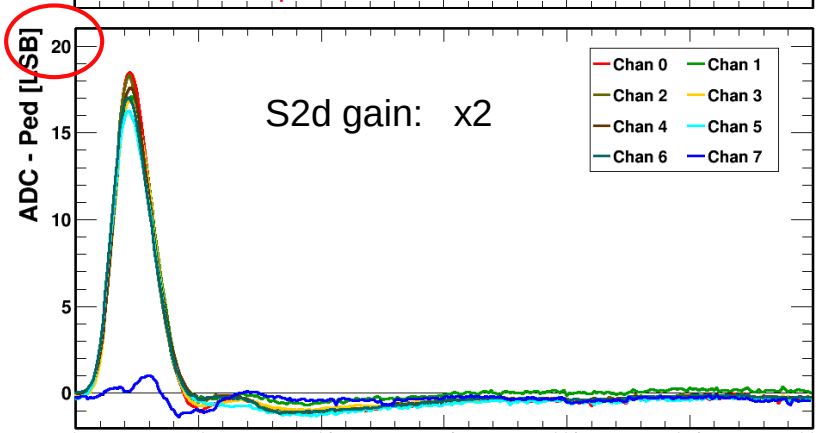
- SALT8a & SALT8b do not have TMR implemented. Thus we can not have SEU test on these chips directly. SALT128 includes TMR in the design. Thus we can test it in radiation directly.
- MGH is fully booked this year. We may wait for cancellation or share beam slot with others.
- CHARM can also provide beam we need but may not match our SALT128 production & test plan.

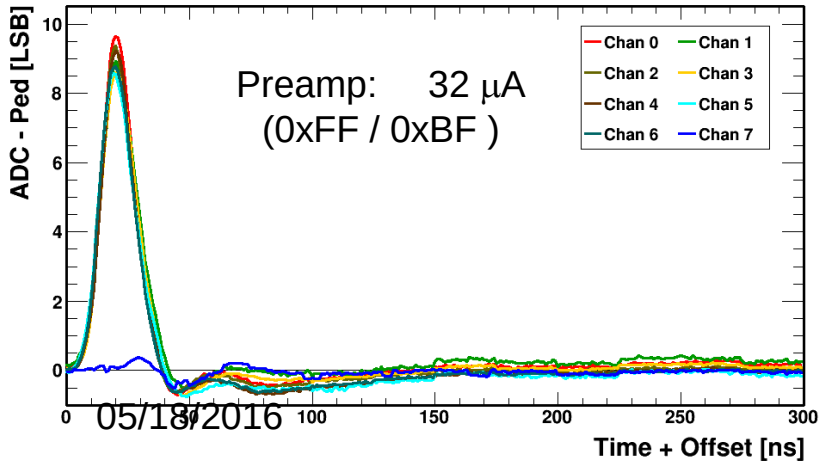
- TID effects can be tested on SALT8b using the CERN X-ray facility, now that it is tested. We need to decide whether we should do it soon or wait for SALT128.

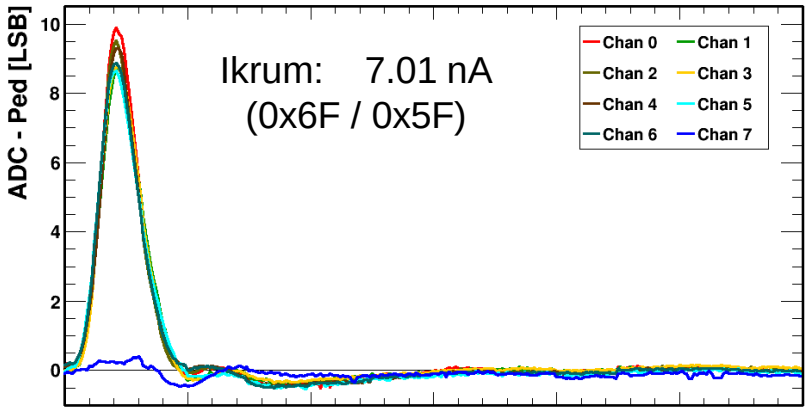
Backup

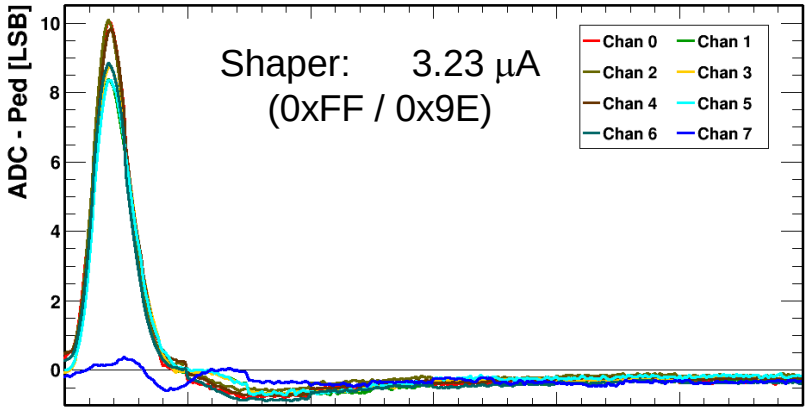
Pulse Shape For Different Settings (I)

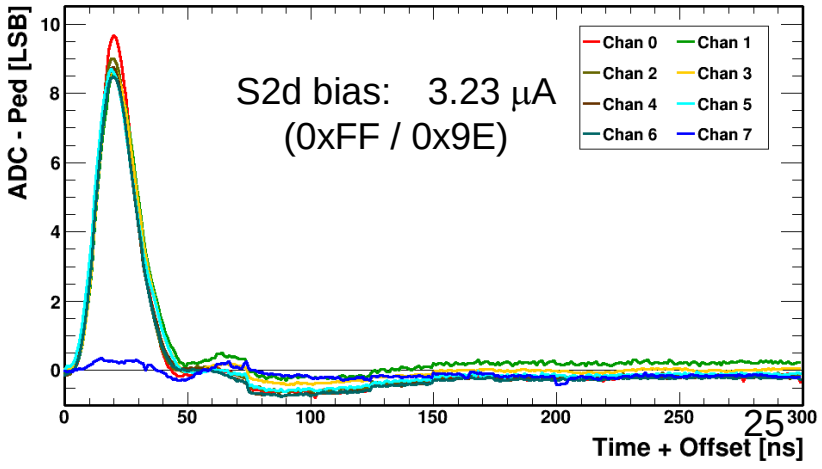




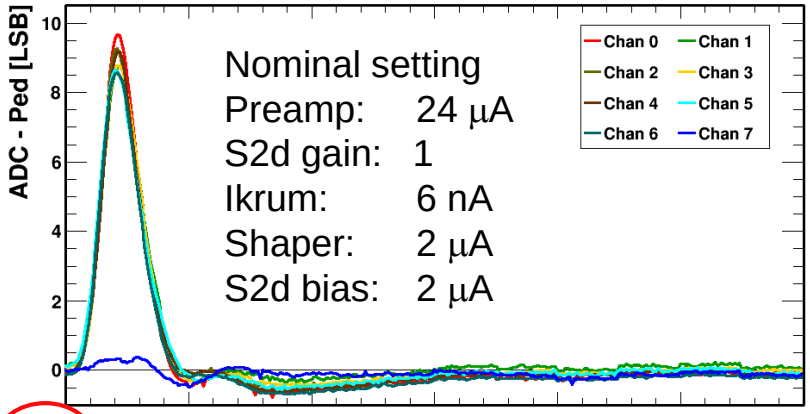


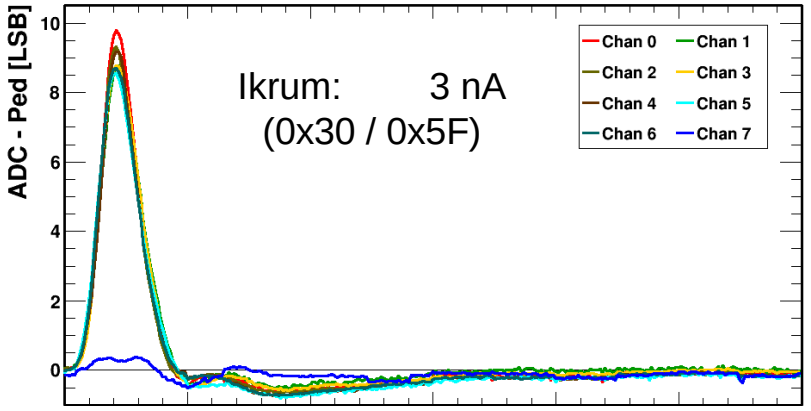


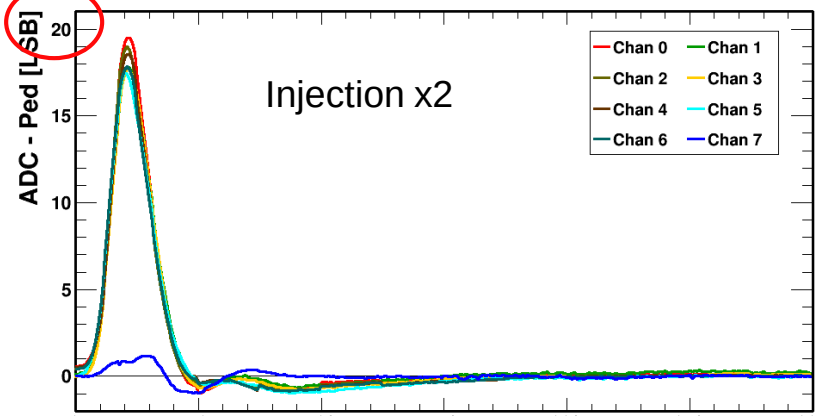


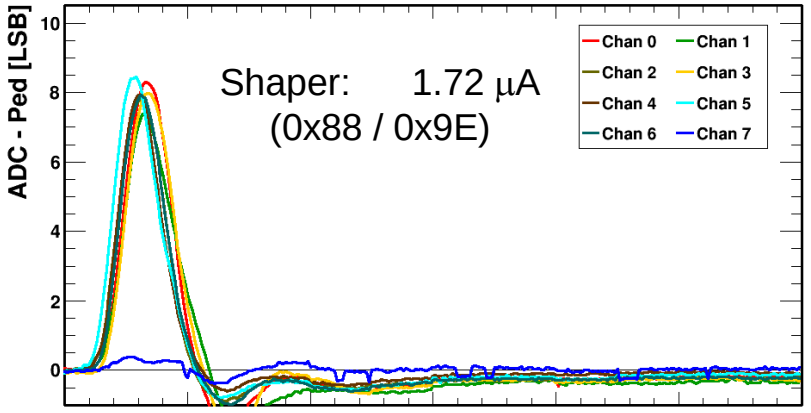


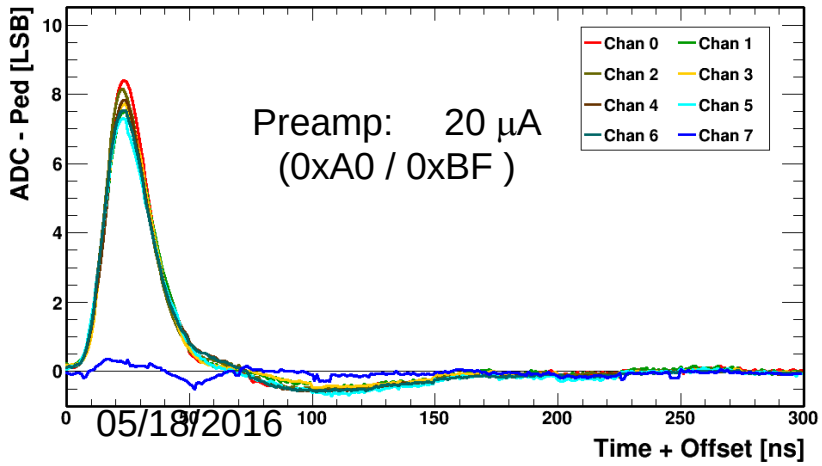
Pulse Shape For Different Settings (II)

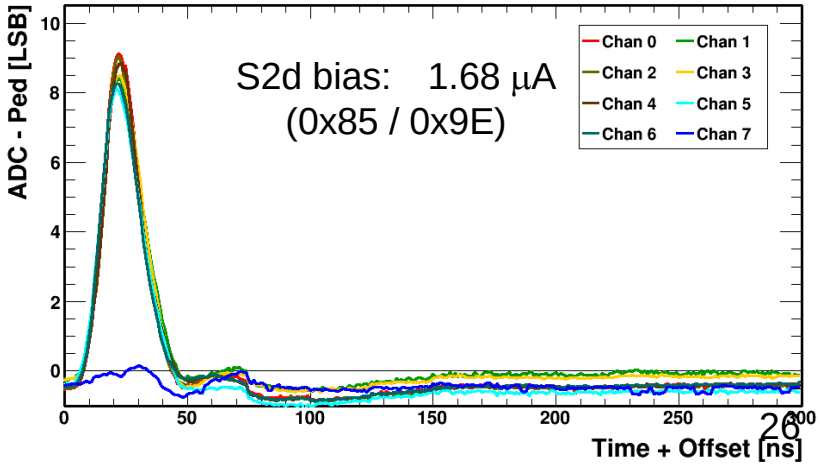










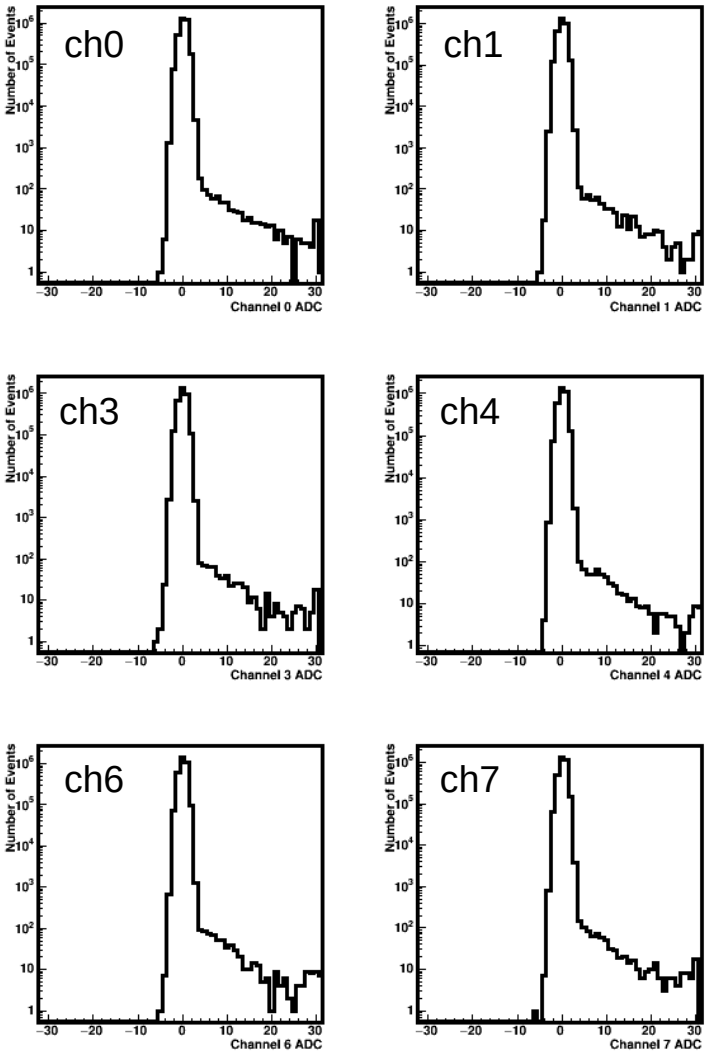


UT Event Packets For SALT8

Header (8-bit)			Length (8-bit)		Data	Comment
BXID	Flag	Parity	Value	Parity		
4-bit	3-bit	1-bit	7-bit	1-bit	8n-bit	
0000_b	110_b	0_b	not present			Idle packet (append if no enough data)
bxid	100_b	*				BXVeto, HeaderOnly, or EmptyEvent (nHits=0)
bxid	010_b	*	nHits	*		Truncated event (nHits>63, or BufferFull)
bxid	000_b	*	nBytes	*	data	Normal event (nHits≤63)
bxid	001_b	*	$111\ 1111_b$	1_b	data	NZS packet, true length is fixed in the firmware
12-bit bxid			12/20/28-bit pattern			Synch packet, fill one whole frame

- The event packet formats were initially byte-aligned, with a variable size (8 or 16) of header+length.
- The formats were re-optimized for efficiently use of TELL40. The updated format is implemented in SALT128, not SALT8.
- Certain issues found in SALT8 are irrelevant for SALT128.

Signal Of Beta Source



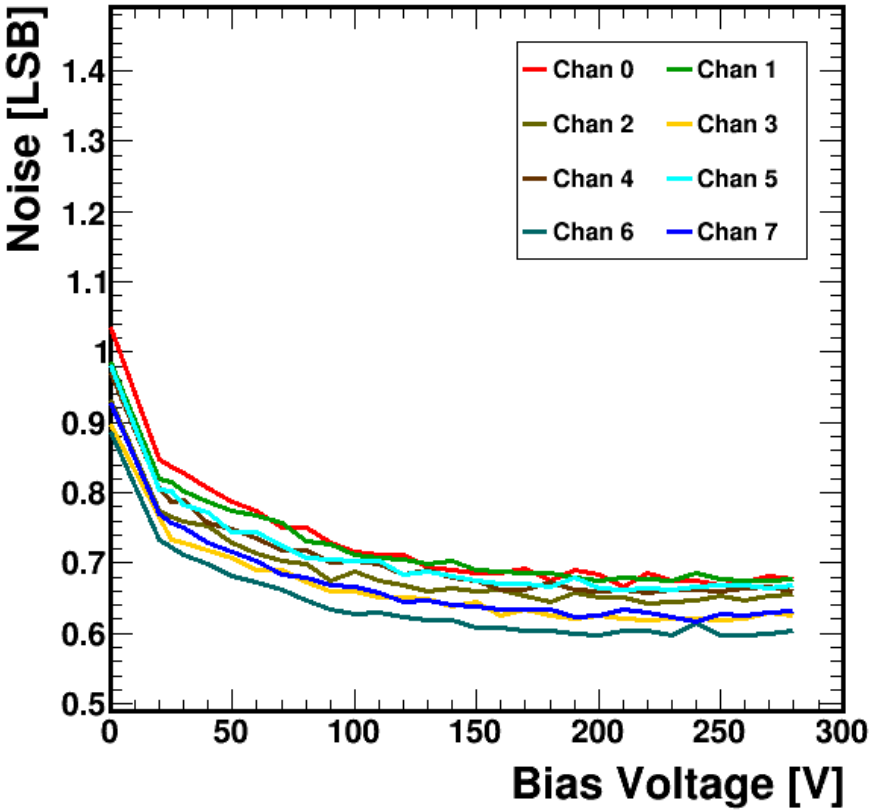
Thanks to help from Ray Mountain

Sr90 beta source: 0.546 & 2.28 MeV

Non-synchronous DAQ with random trigger.

Tails due to beta source.

Noise Vs Bias Voltage

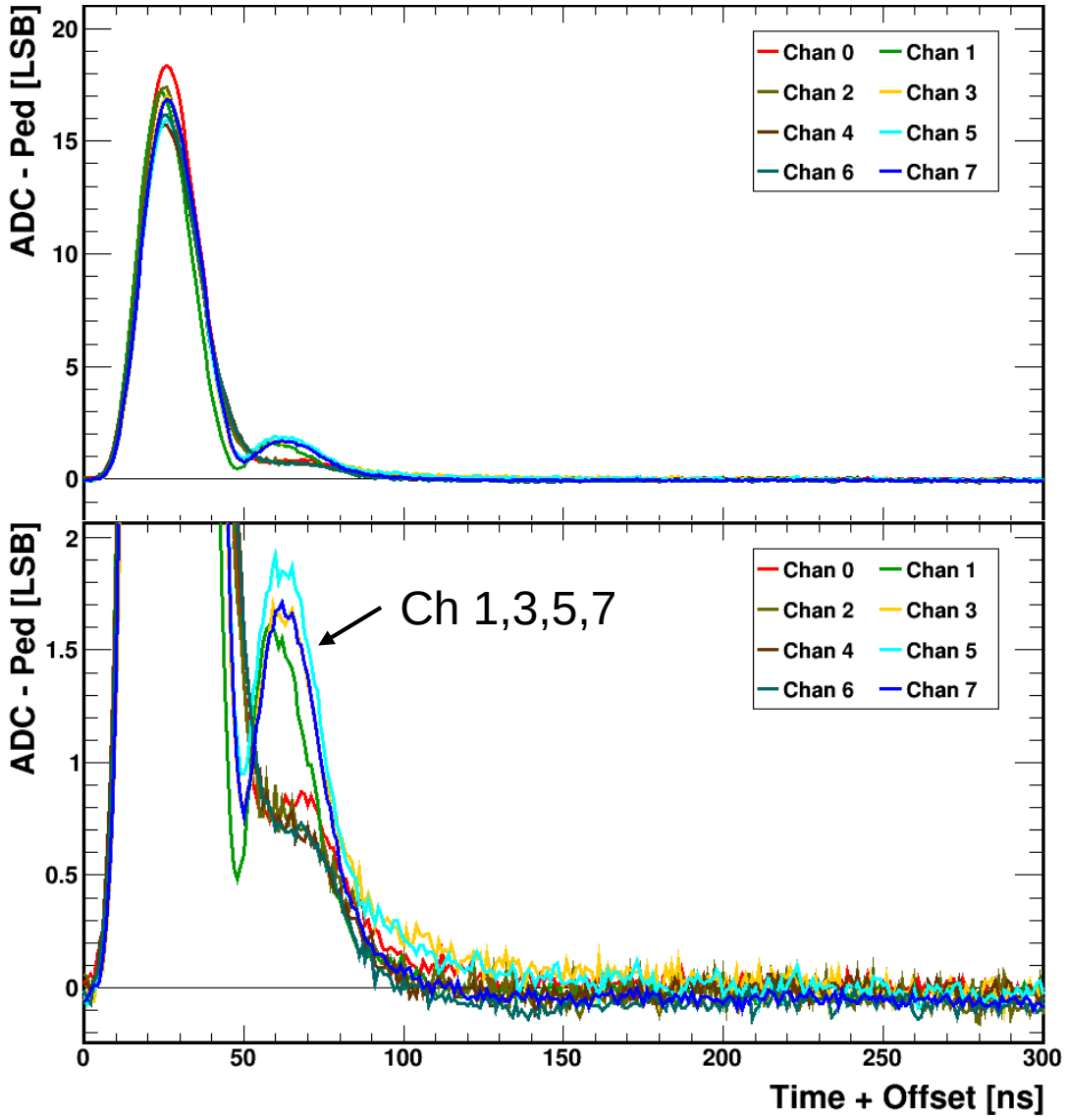


Gain ~ 0.45 ADC LSB / Ke

Not quite sure about the value of capacitance between strips.

P-type sensors (250 μm & 200 μm thick) are biased at 200 V for most tests.

Pulse Shape With Capacitor Arrays



SALT8a

Ch 0-3: 10 pF
Ch 4-7: 15 pF

Channels that are supplied by TEST1 (ch 1,3,5,7) have the 2nd peaks.

Ch 0,2,4,6 have shoulders

It seems associated with charge injection routes. To be further studied with real sensor.

Crosstalk From Simulation

- Crosstalk was simulated at Krakow (Marek Idzik)
  - C_{bulk} = 0, Preamp bias current default (DAC=15), C_{ac}=100 pF.
  - $C_{interstrip}$ = 2×5 pF, cross talk = 6%.
  - $C_{interstrip}$ = 2×4 pF, cross talk = 4.6%.
  - $C_{interstrip}$ = 2×3 pF, cross talk = 4.6%.
  - $C_{interstrip}$ = 2×2 pF, cross talk = 2.2%.

- Half-A sensor: P-type, 250 μm thick, 190 μm pitch, $C_{interstrip}$ ~ 2×5 pF, C_{bulk} < 3 pF, C_{ac} > 100 pF.

Breakdown of Power Consumption

- Currents are measured on SALT8b test board:
  - VDDD+VDDPST 25.94 mA (SW1 on testboard)
  - VDDA_BUF 1.18 mA (SW10)
  - VDDAD+VREFD+VDDADC 2.30 mA (SW6)
  - VDDA 29.52 mA (total – sum of three)

- VDDA includes V_{cm} generated on board ~ 1.2 V / 50 Ω.