AGH UNIVERSITY OF SCIENCE AND TECHNOLOGY

SALT Design I

(**S**ilicon **A**SIC for **L**HCb **T**racking)

Marek Idzik on behalf of AGH-UST

Faculty of Physics and Applied Computer Science
AGH University of Science and Technology

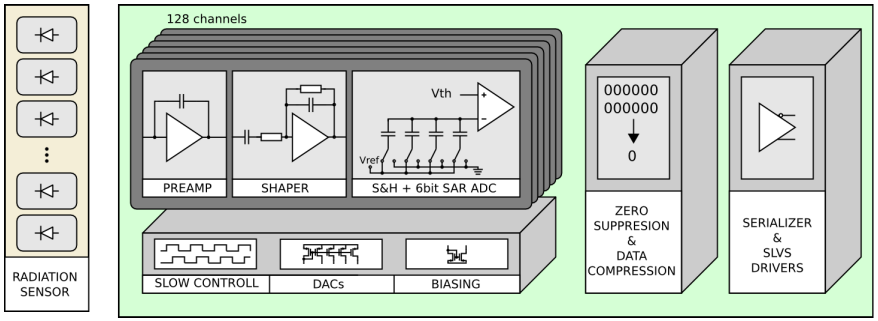
INFN Milano LHCb UT workshop
Milano 17-19 May 2016

Outline

- Introduction
- SALT architecture and design
  - Analog and Mixed-Mode
  - Other...
- Simulations, Status and Plans

Introduction
The goal and short history

The Goal – SALT readout ASIC for UT detector



AGH-UST Design team:

- staff: M. Firlej, T. Fiutowski, M. Idzik, J. Moroń, K. Świentek
- PhD students: Sz. Bugiel, R. Dasgupta, M. Kopeć, M. Kuczyńska

SALT story in short:

- Two submissions (5 ASICs) of key functional blocks (Preamplifier&Shaper, Single-to-Diff converter, 6-bit ADC, SLVS, PLL, DLL) done in IBM CMOS 130 nm - designed&fabricated and mostly tested
- In 2014 collaboration decided to move to TSMC CMOS 130 nm
- In February 2015 a large submission – 8 chips, including SALT8 and various blocks, were submitted in TSMC 130 nm – partially tested, problems with ESD/pads (mainly FE and ADC chips)
- In November 2015 SALT8 version 2, 8-channel FE&ADC chips plus other blocks (e.g. bandgaps) submitted, just fabricated, SALT8 tested by JC
- June 2016 we will submit complete 128-channel SALT chip (why not May ?)

Introduction
SALT – Specification

- TSMC CMOS 130 nm technology
- 128 channels, Front-end&ADC in each channel
- Input Pitch 80 um (plus ground pads on the sides!!!), Output pitch =140um
- Sensor: capacitance 5–20 pF, AC coupled
- Both input signal polarities (p-in-n and n-in-p sensors)
- Input charge range ~ 30ke$^-$
- Noise: ENC ~ 1000e$^-$ @10pF + 50e$^-$/pF
- Pulse shape: T_{peak} ~25 ns, very short tail: ~5% after 2*T_{peak}
- Crosstalk < 5%
- ADC: 6-bit resolution (5-bit/polarity), 40MS/s
- DSP functions: pedestal and common mode subtraction, zero-suppression
- Serialization&Data transmission: 320 Mbps e-links to GBT, SLVS I/O
- Slow control: I2C
- Power < 6 mW/channel
- Radiation hardness ~ 30 MRad

Introduction
SALT documentation

SALT ver 3 chip documentation

Miroslaw Firlej, Tomasz Fiutowski, Marek Idzik,
Jakub Moron, Krzysztof Swientek
Szymon Bugiel, Roma Dasgupta, Marika Kuczynska

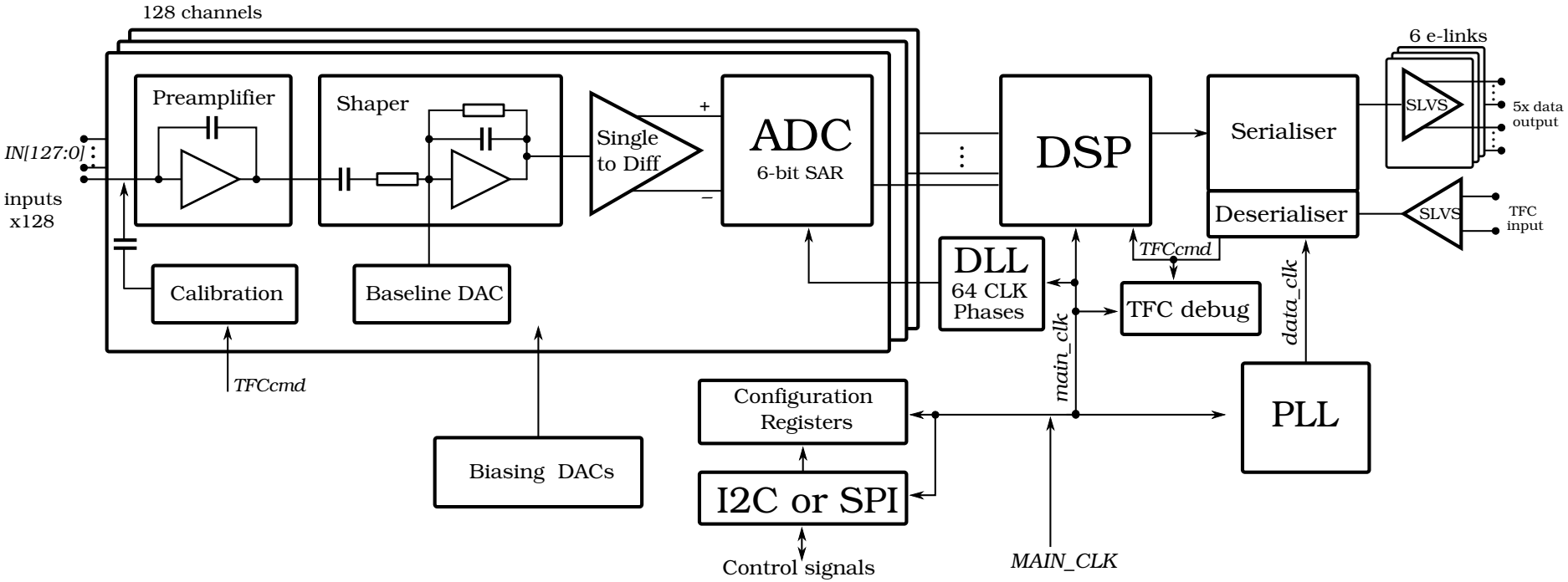
Created: January 2016

Last change: May 13, 2016

Contents

SALT documentation is not yet completed, work in progress...

Introduction
SALT Architecture

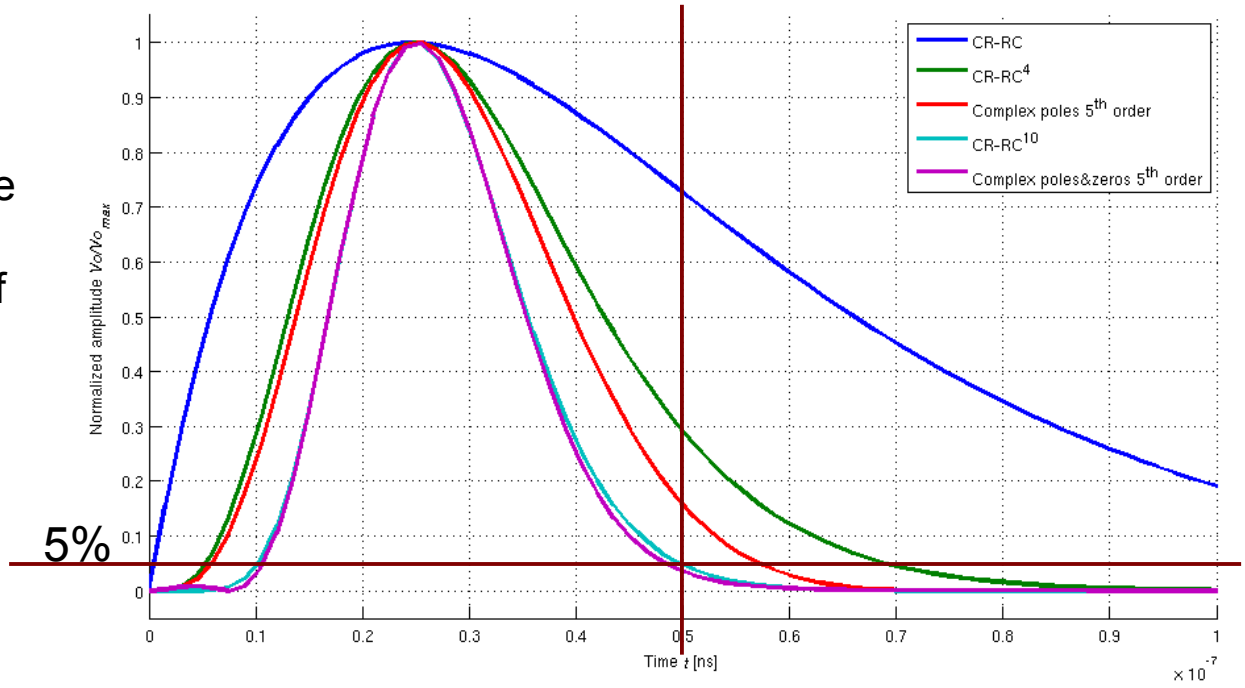


Most of key blocks of SALT were included in 8-channel prototypes called SALT8 version1&2. In SALT8 version2 important parts (e.g. ELT transistors for small currents, new Single to Diff) have been improved or corrected. But since SALT is a very complex chip several features will appear only in next submission...

SALT design
Front-end considerations

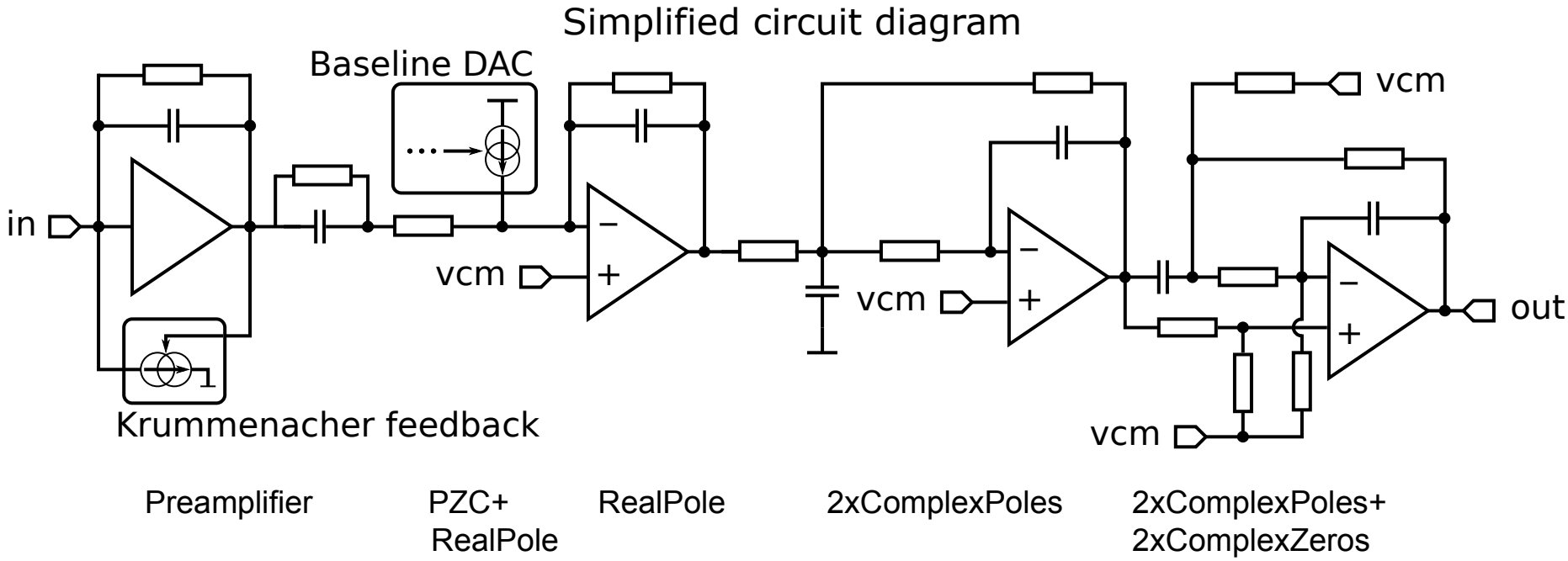
Is it possible, with realistic shaper complexity and power consumption, to shorten the pulse tail to decrease to 5% of pulse amplitude after $2*T_{peak}$?

Matlab simulations of the front-end response for various configurations of poles and zeros in the shaper transfer function



Introducing complex poles and zeros in transfer function one can shorten the pulse tail to the required goal

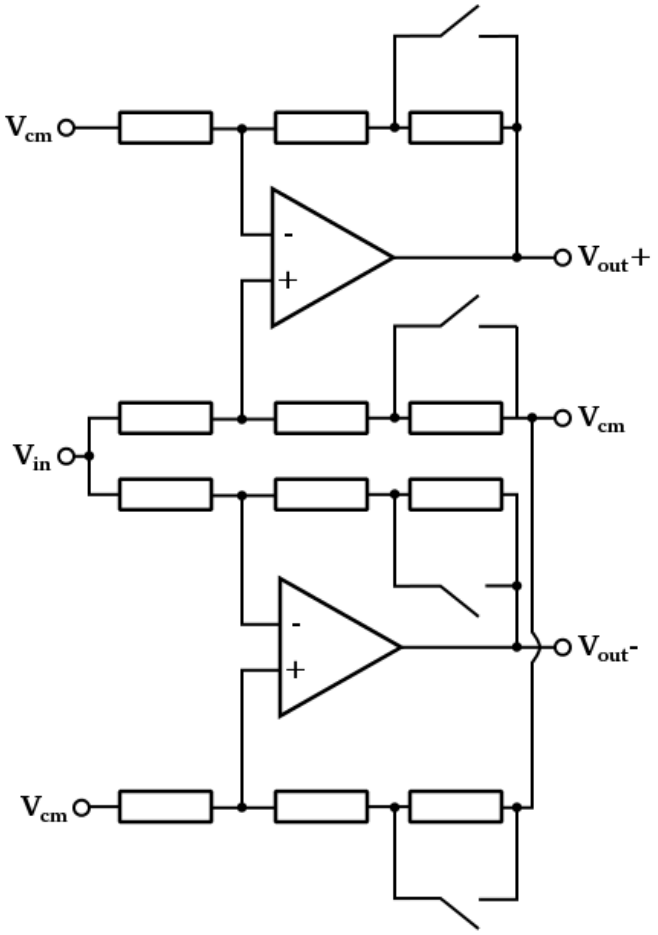
SALT design
Preamplifier and Shaper



- 3-stage shaper gives the requested pulse with short tail
- Common mode (vcm) is kept at half power supply to work with both pulse polarities

Same as in SALT8 version 2

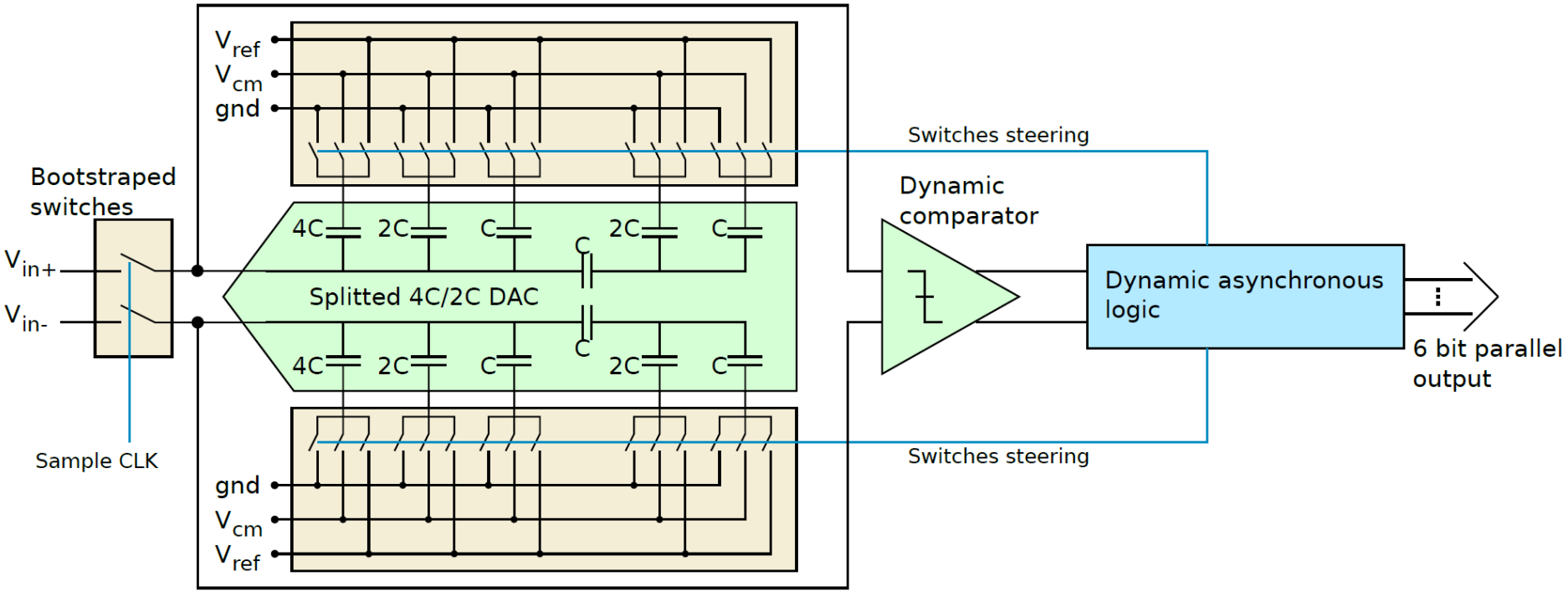
SALT design
Single to Differential Converter (S2Diff)



- Pseudo-differential solution based on single- ended amplifiers chosen
- Additional gain by 2 may be obtained in S2Diff

Same as in SALT8 version 2

SALT design
6-bit ADC

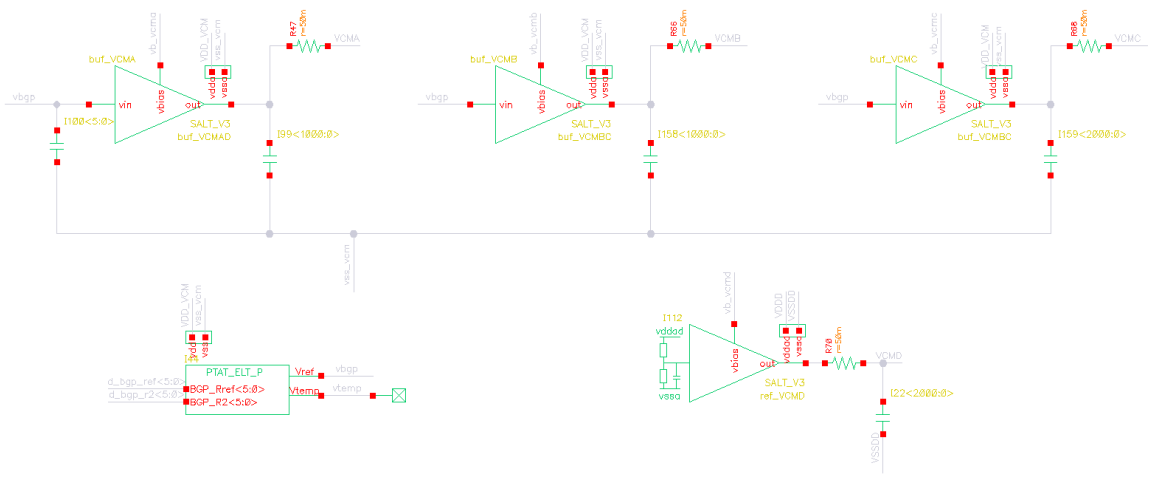


Main features:

- SAR architecture, 6-bit resolution
- 40 MSps nominal sampling rate
- Split DAC with MCS switching scheme
- Asynchronous logic

Same as in SALT8 version 2

SALT design
Common mode voltages generation and bandgap reference



Newly designed for SALT

Reference signals:

- Bandgap reference of 0.6V. The circuit includes also temperature sensor
- VCMA 0.6V for first two shaper stages
- VCMB 0.6V for third shaper stage
- VCMC 0.6V for single-to-differential
- VCMD 0.6V common mode voltage for ADC

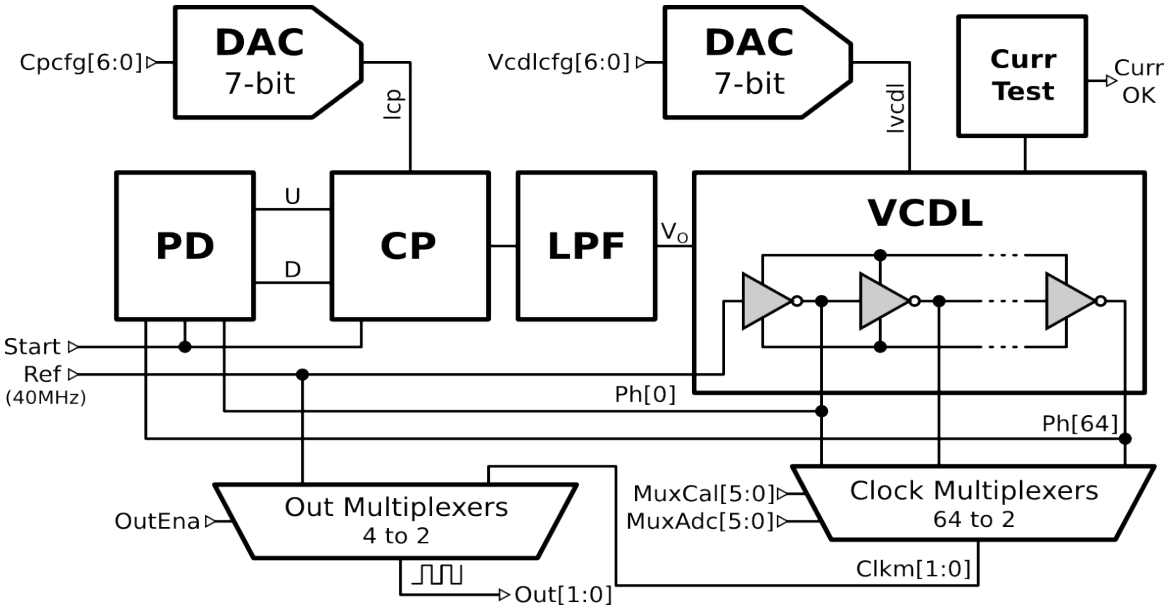
SALT design
Biasing, Calibration Monitoring, ….

Other Analog&Mixed-mode components:

- Two test channels (one on each side), various signals are buffered and go to pads
- Calibration circuit (set separately for each channel)
- 7 DACs setting various biases: preamp, Krummenacher, shaper, S-2-Diff, Calibration, SLVS-Ibias, SLVS-Vref. Could be readout via test-pads
- Six Monitoring 6-bit ADCs: Vctl-PLL, Vctl-DLL, 7 DACs multiplexed to 2 ADCs, PTAT-temperature, Vref-bandgap

Mostly newly designed for SALT or modified

SALT design
DLL



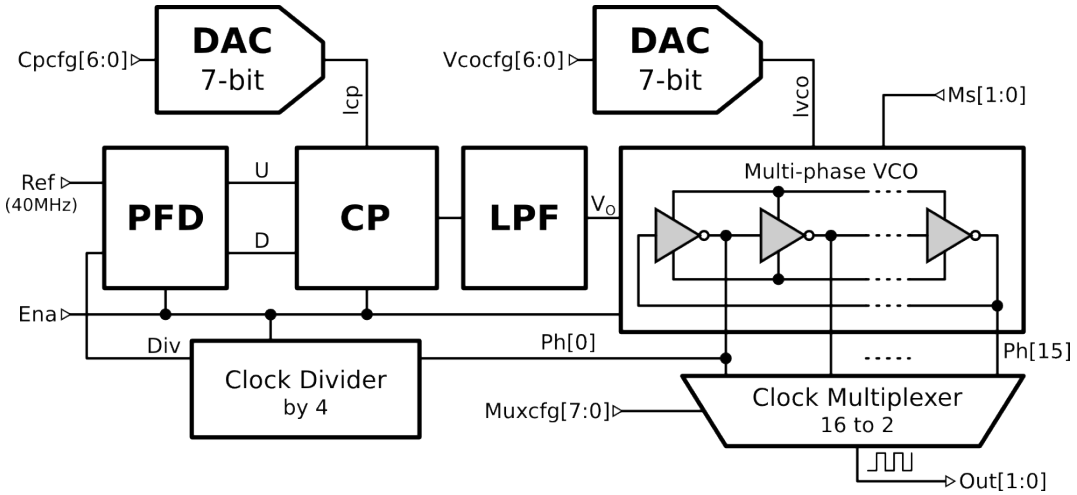
DLL features:

- Operating frequency: 40MHz
- 64 clock phases
- Two slectable output phases
- VCDL Current Test Logic
- Power < 2mW @ 40MHz
- Jitter < 15 ps @ 40MHz

PFD change to PD to improve radiation hardness

Monitoring and calibration improved

SALT design
PLL



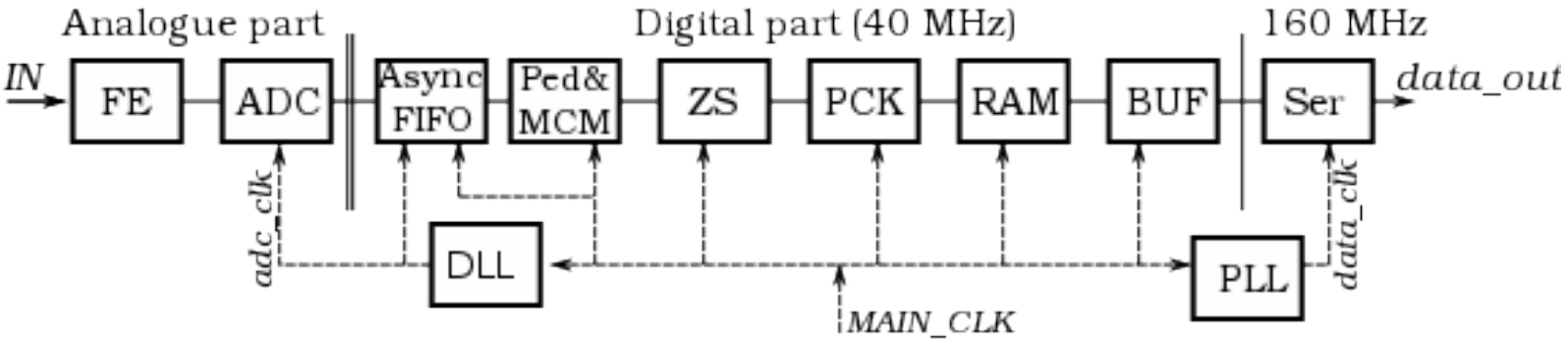
PLL features:

- Output frequency 160MHz
- Divider by: 4
- Reference frequency 40MHz
- 16 phases available
- Two slectable output phases
- Power < 2mW @ 160MHz
- Jitter < 10ps @ 160MHz

Practically, the same as in SALT8 version 2

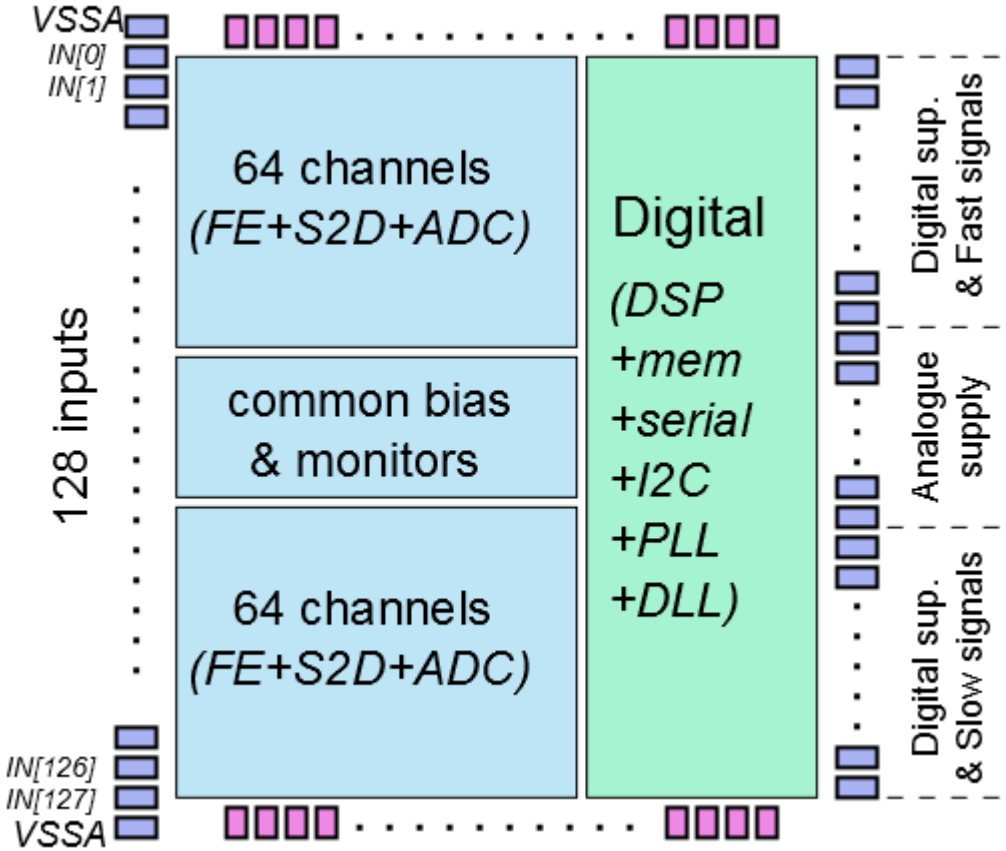
(not used functionality removed)

SALT design
DSP and Data Processing Chain



Many changes → Krzysztof

SALT integration
Floorplan and layout



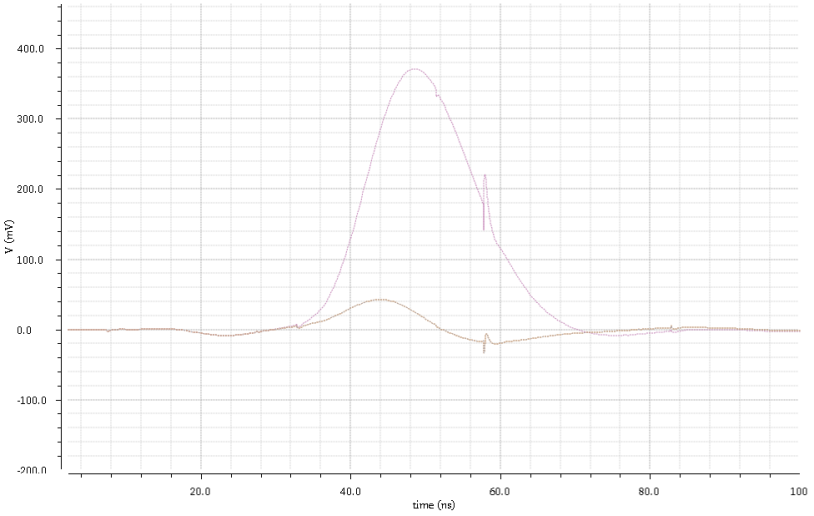
Completly new → Tomek

SALT – simulations, status and plans

- Layout of 128 channels
  - Analog&Mixed-mode just completed → Tomek
  - Digital in progress → Krzysztof
- Top level simulations – by now done either on schematic or only part of extracted view (lack of computing power/memory)
- When taking into account realistic supply network various parameters

  – crosstalk, disturbances, PSRR deteriorate, how much ?

  → we need 128-channel simulation on extracted view



Schematic 128 channels,
Cdet=3pF, Cint=2x5pF

SALT – simulations, status and plans

- Last week we managed to prepare a workstation with ~300GB of RAM
- We have managed to extract the netlist of 128 channels of Analog&Mixed-mode part
- First simulations just started (~week for simple run)
- Few words about power…
- ….
- Submission planned for mid-June