1. Padring

Floorplan block diagram is shown of the 128-channel prototype of Silicon ASIC for LHCb Tracking (SALT) Application Specific Circuit (ASIC) is shown in figure 1. Front (left in figure 1) pads have 80 μm pitch while back (digital) pads are placed in 140 μm pitch.

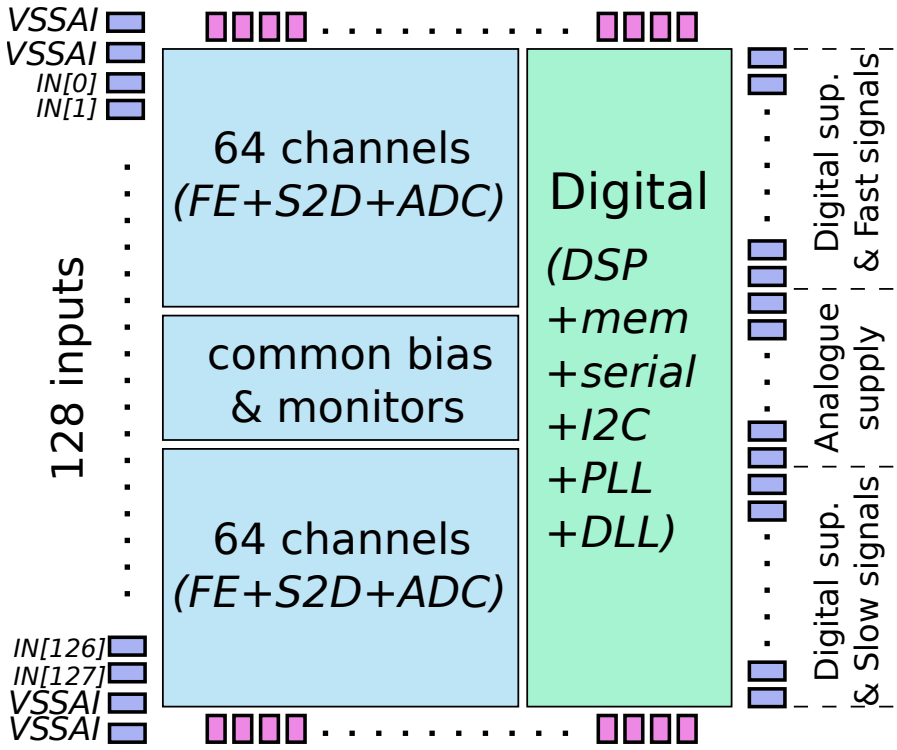

Figure 1: Floorplan of the SALT ASIC

The pad ring of the ASIC is shown in figures: 2 (input), 5 (back), 3 (top), and 4 (bottom). Input and back pads are longer then top and bottom pads. The former will be first used for wafer screening and thereafter bonded to hybrid, the latter are intended only for wafer screening.

Table 1: Pad list of the top side; all pads here are only for tests purpose; pads marked with (W) are intended for wafer screening (there is no power supply provided for the test pads buffers inside the ASIC – during tests all power supply pads have to be connected)

No	Name	Type	Description
From LEFT			
1	*PRE_BUF*[0]	voltage out	Test channel[0]: buffered pre-amp output
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Table 1 – continued from previous page

No	Name	Type	Description
2	*SH1_BUF*[0]	voltage out	Test channel[0]: buffered shaper 1st stage output
3	*SH2_BUF*[0]	voltage out	Test channel[0]: buffered shaper 2nd stage output
4	*SH_BUF*[0]	voltage out	Test channel[0]: buffered shaper 3rd stage output
5	*AP_BUF*[0]	voltage out	Test channel[0]: buffered s2d positive output
6	*AN_BUF*[0]	voltage out	Test channel[0]: buffered s2d positive output
7	*I_BUF*[0]	current in	Test channel[0]: buffers biasing current (default 25uA from *VDDA_BUF*[0])
8	*VSSPST_BUF*[0]	ESD (W)	Test pads ESD ground
9	*VSSA_BUF*[0]	power	Test pads buffers ground
10	*VDDA_BUF*[0]	power+ESD (W)	Test pads buffers and ESD power
11	*VCMA*	voltage out (W)	Common mode voltage A test pad
12	*VCMB*	voltage out (W)	Common mode voltage B test pad
13	*VCMC*	voltage out (W)	Common mode voltage C test pad
14	*VCMD*	voltage out (W)	Common mode voltage D test pad
15	*V_PRE_DAC*	voltage out (W)	Pre-amp biasing DAC output
16	*V_KRUM_DAC*	voltage out (W)	Krum biasing DAC output
17	*V_SH_DAC*	voltage out (W)	Shaper biasing DAC output
18	*DATA_CLK_OUT_P*	SLVS out	Data clock output
19	*DATA_CLK_OUT_N*	SLVS out	Data clock output

Table 2: Pad list of the bottom side; all pads here are only for tests purpose; pads marked with (W) are intended for wafer screening (there is no power supply provided for the test pads buffers inside the ASIC – during tests all power supply pads have to be connected)

No	Name	Type	Description
		From LEFT	
1	*PRE_BUF*[1]	voltage out	Test channel[1]: buffered pre-amp output
2	*SH1_BUF*[1]	voltage out	Test channel[1]: buffered shaper 1st stage output
3	*SH2_BUF*[1]	voltage out	Test channel[1]: buffered shaper 2nd stage output
		Continued on next page	

Table 2 – continued from previous page

No	Name	Type	Description
4	*SH_BUF*[1]	voltage out	Test channel[1]: buffered shaper 3rd stage output
5	*AP_BUF*[1]	voltage out	Test channel[1]: buffered s2d positive output
6	*AN_BUF*[1]	voltage out	Test channel[1]: buffered s2d positive output
7	*I_BUF*[1]	current in	Test channel[1]: buffers biasing current (default 25uA from *VDDA_BUF*[1])
8	*VSSPST_BUF*[1]	ESD (W)	Test pads ESD ground
9	*VSSA_BUF*[1]	power	Test pads buffers ground
10	*VDDA_BUF*[1]	power+ESD (W)	Test pads buffers and ESD power
11	*ADC_INP*	voltage in	Test channel[1]: ADC positive input
12	*ADC_INN*	voltage in	Test channel[1]: ADC negative input
14	*V_S2D_DAC*	voltage out (W)	S2D biasing DAC output
15	*V_PULSE_DAC*	voltage out (W)	Calibration test pulse amplitude DAC output
16	*V_SLVS_VBIAS_DAC*	voltage out (W)	SLVS biasing DAC output
17	*V_SLVS_INREF_DAC*	voltage out (W)	SLVS biasing DAC output
18	*SCAN_ENABLE*	CMOS in (W)	Scan/normal mode selection (pulled down)
19	*SDI*	CMOS in (W)	Scan chain input
20	*SDO*	CMOS out (W)	Scan chain output
21	*TEST_MODE*	CMOS in (W)	Switches chip into test mode (pulled down)

Table 3: Pad list of the back side; pads marked with (W) are intended for wafer screening (there is no default value for any input signal provided inside the ASIC, all signal pads have to be connected)

No	Name	Type	Description
From BOTTOM			
1	*VDD*	power	Digital supply
2	*VSS*	power	Digital ground
3	*VDD*	power	Digital supply
4	*VSS*	power	Digital ground
Continued on next page			

Table 3 – continued from previous page

No	Name	Type	Description
5	*VDDPST*	ESD	Digital ESD supply
6	*ID*[0]	CMOS in	I^2C address
7	*ID*[1]	CMOS in	I^2C address
8	*ID*[2]	CMOS in	I^2C address
9	*I2C_SCL*	CMOS in	I^2C clock line
10	*I2C_SDA*	CMOS inout	I^2C data line
11	*RST_N*	CMOS in	Asynchronous reset
12	*MAIN_CLK_N*	SLVS in	Main clock input (40 MHz)
13	*MAIN_CLK_P*	SLVS in	Main clock input (40 MHz)
14	*VSSPST*	ESD	Digital ESD ground
15	*VDD*	power	Digital supply
16	*VSS*	power	Digital ground
17	*VDD*	power	Digital supply
18	*VSS*	power	Digital ground
RING POWER CUT			
19	*VDDADC*	power	Analogue ADC supply
20	*VSSADC*	power	Analogue ADC ground
21	*VDDADC*	power	Analogue ADC supply
22	*VSSADC*	power	Analogue ADC ground
23	*VDDADC*	power	Analogue ADC supply
24	*VSSADC*	power	Analogue ADC ground
25	*VREFD*	power	Analogue ADC supply
26	*VSSADC*	power	Analogue ADC ground
27	*VREFD*	power	Analogue ADC supply
28	*VSSVCM*	power	Analogue VCM buffers ground
29	*VDDVCM*	power	Analogue VCM buffers supply
30	*VSSVCM*	power	Analogue VCM buffers ground
31	*VDDVCM*	power	Analogue VCM buffers supply
32	*VSSAPST*	ESD	Analogue ESD ground
33	*VDDAPST*	ESD	Analogue ESD supply
34	*VSSAPST*	ESD	Analogue ESD ground
35	*VDDAPST*	ESD	Analogue ESD supply
36	*VSSAPST_IN*	ESD	Analogue input pads ESD ground
37	*VDDAPST_IN*	ESD	Analogue input pads ESD supply
38	*VSSAPST_IN*	ESD	Analogue input pads ESD ground
39	*VDDAPST_IN*	ESD	Analogue input pads ESD supply
40	*VSSAI*	power	Analogue input transistor ground
41	*VDDA*	power	Analogue front-end supply
42	*VSSAI*	power	Analogue input transistor ground
43	*VDDA*	power	Analogue front-end supply

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Table 3 – continued from previous page

No	Name	Type	Description
44	*VSSAI*	power	Analogue input transistor ground
45	*VDDA*	power	Analogue front-end supply
46	*VSSA*	power	Analogue front-end ground
47	*VDDA*	power	Analogue front-end supply
48	*VSSA*	power	Analogue front-end ground
49	*VDDA*	power	Analogue front-end supply
50	*VSSA*	power	Analogue front-end ground
51	*VDDA*	power	Analogue front-end supply
RING POWER CUT			
52	*VSS*	power	Digital ground
53	*VDD*	power	Digital supply
54	*VSS*	power	Digital ground
55	*VDD*	power	Digital supply
56	*VSSPST*	ESD	Digital ESD ground
57	*DDR_TFC_N*	SLVS in	TFC command input negative
58	*DDR_TFC_P*	SLVS in	TFC command input positive
59	*DDR_OUT_N*[0]	SLVS out	Data output [0] negative
60	*DDR_OUT_P*[0]	SLVS out	Data output [0] positive
61	*DDR_OUT_N*[1]	SLVS out	Data output [1] negative
62	*DDR_OUT_P*[1]	SLVS out	Data output [1] positive
63	*DDR_OUT_N*[2]	SLVS out	Data output [2] negative
64	*DDR_OUT_P*[2]	SLVS out	Data output [2] positive
65	*DDR_OUT_N*[3]	SLVS out	Data output [3] negative
66	*DDR_OUT_P*[3]	SLVS out	Data output [3] positive
67	*DDR_OUT_N*[4]	SLVS out	Data output [4] negative
68	*DDR_OUT_P*[4]	SLVS out	Data output [4] positive
69	*DDR_OUT_N*[5]	SLVS out	Data output [5] negative
70	*DDR_OUT_P*[5]	SLVS out	Data output [5] positive
71	*VDDPST*	ESD	Digital ESD supply
72	*VSS*	power	Digital ground
73	*VDD*	power	Digital supply
74	*VSS*	power	Digital ground
75	*VDD*	power	Digital supply
TOP of the ASIC			

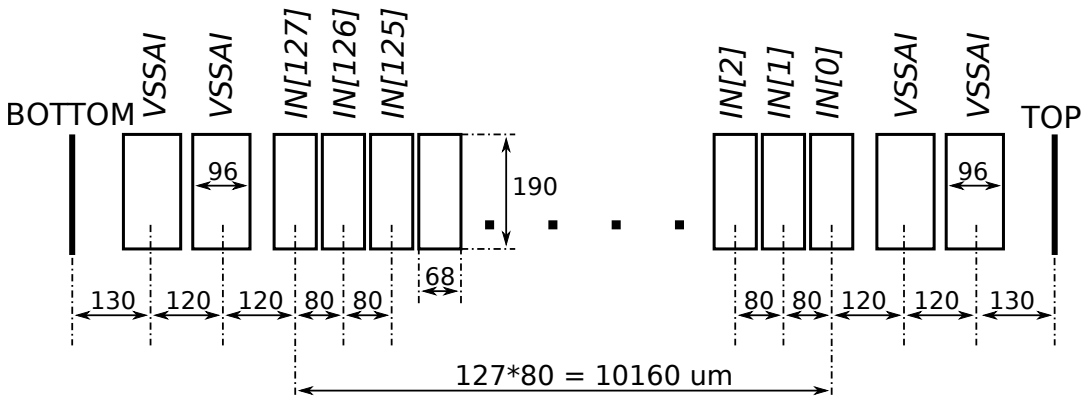

Figure 2: Front pads size and position

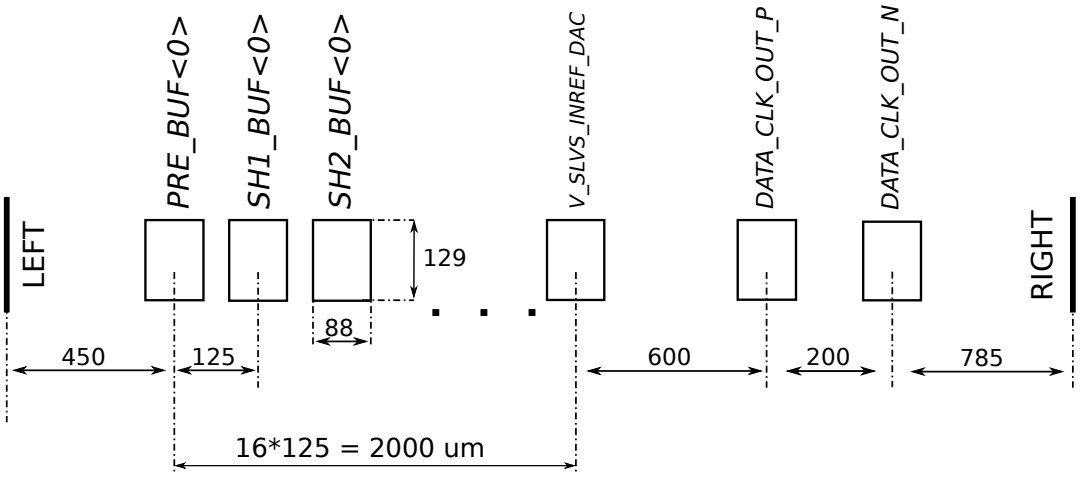

Figure 3: Top pads size and position

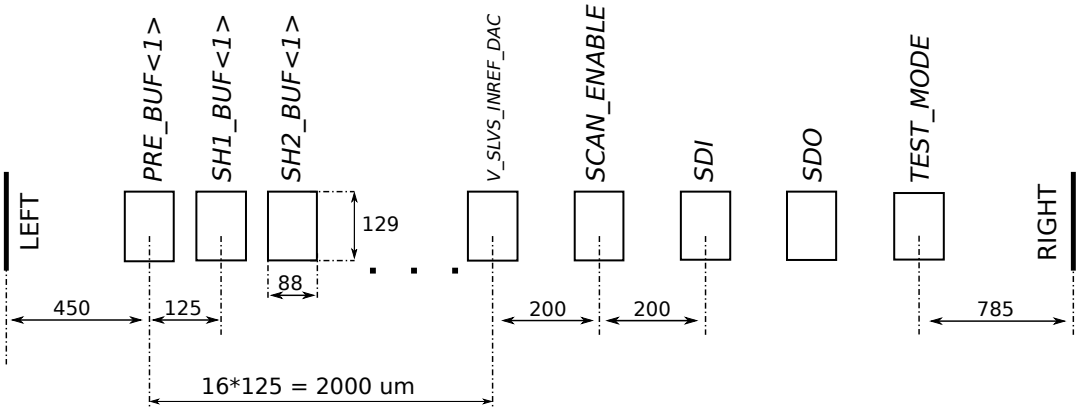

Figure 4: Bottom pads size and position

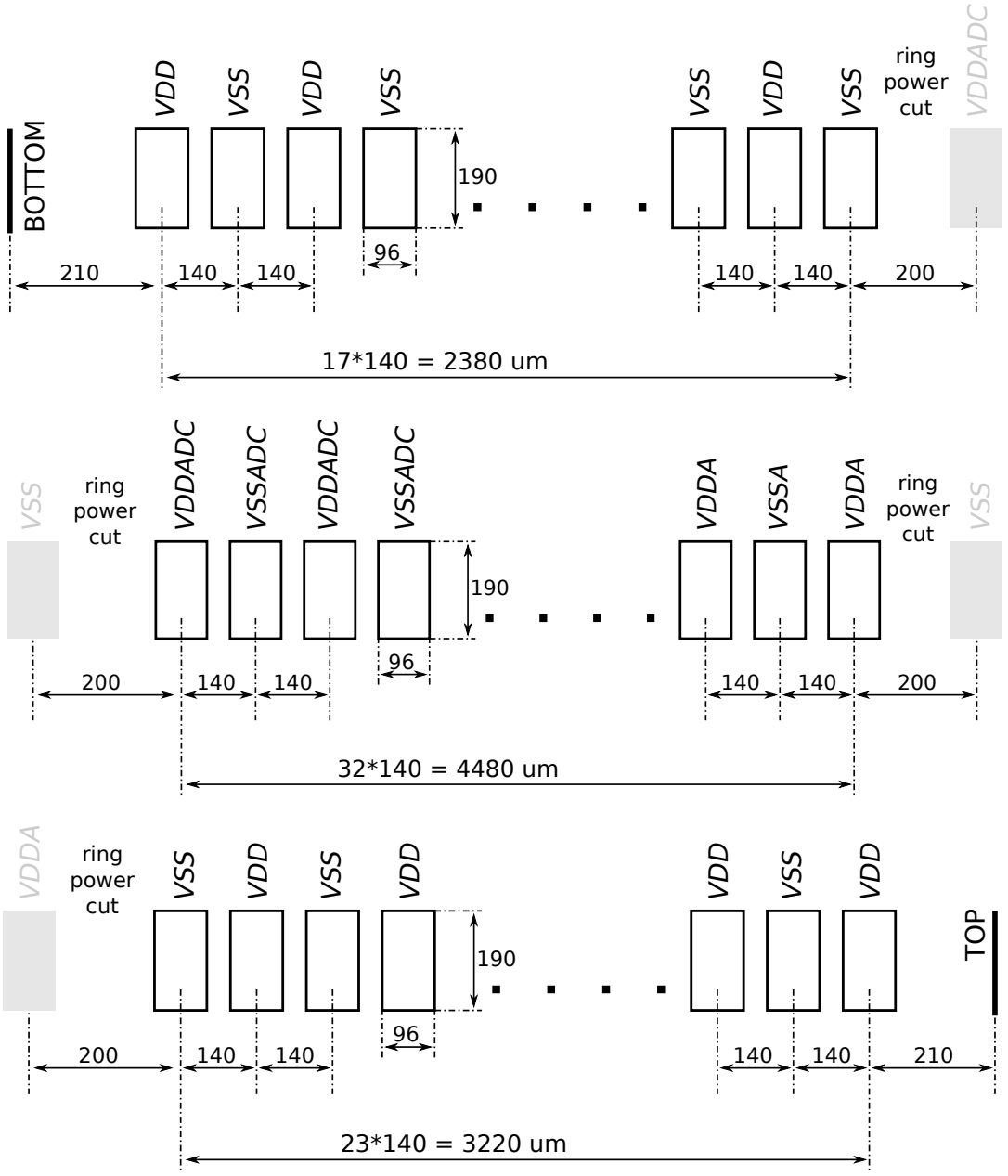

Figure 5: Back side pads size and position