AGH University of Science and Technology

Analog & Mixed-mode Integration

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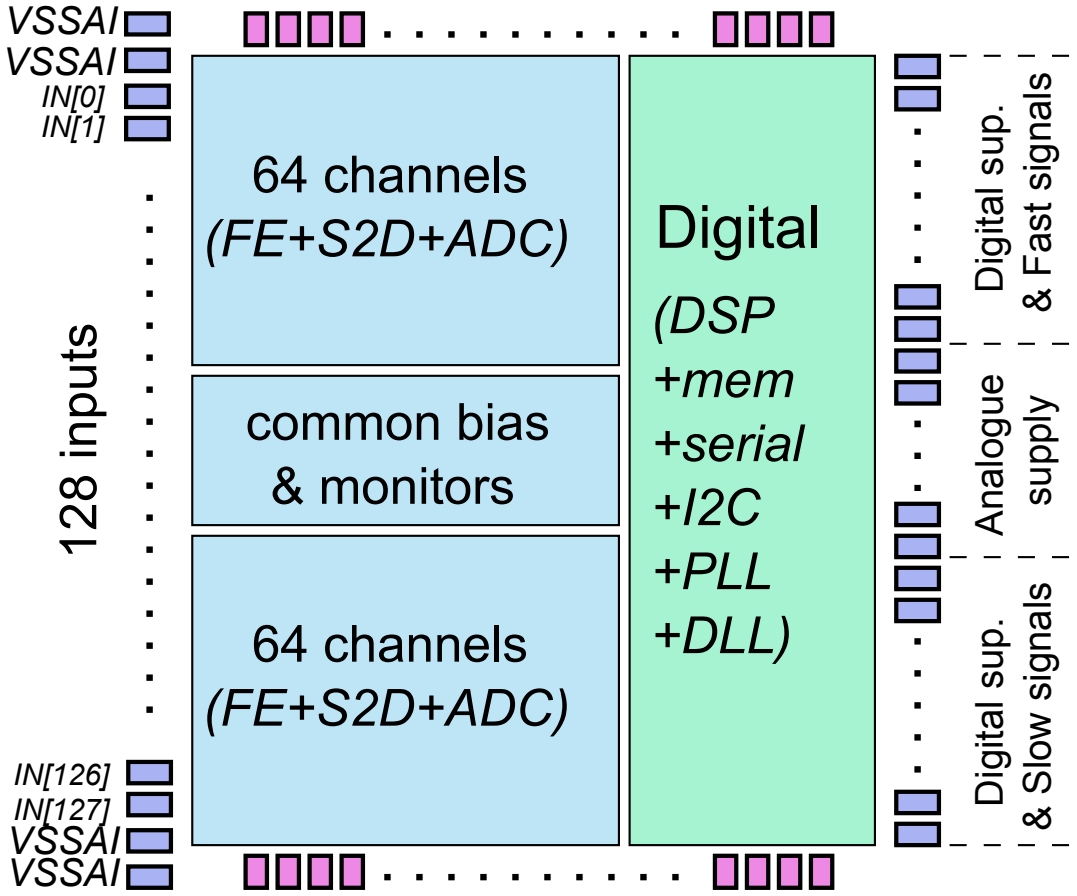
Workshop for internal review of the LHCb Upstream Tracker project
18 May 2016

Floorplan

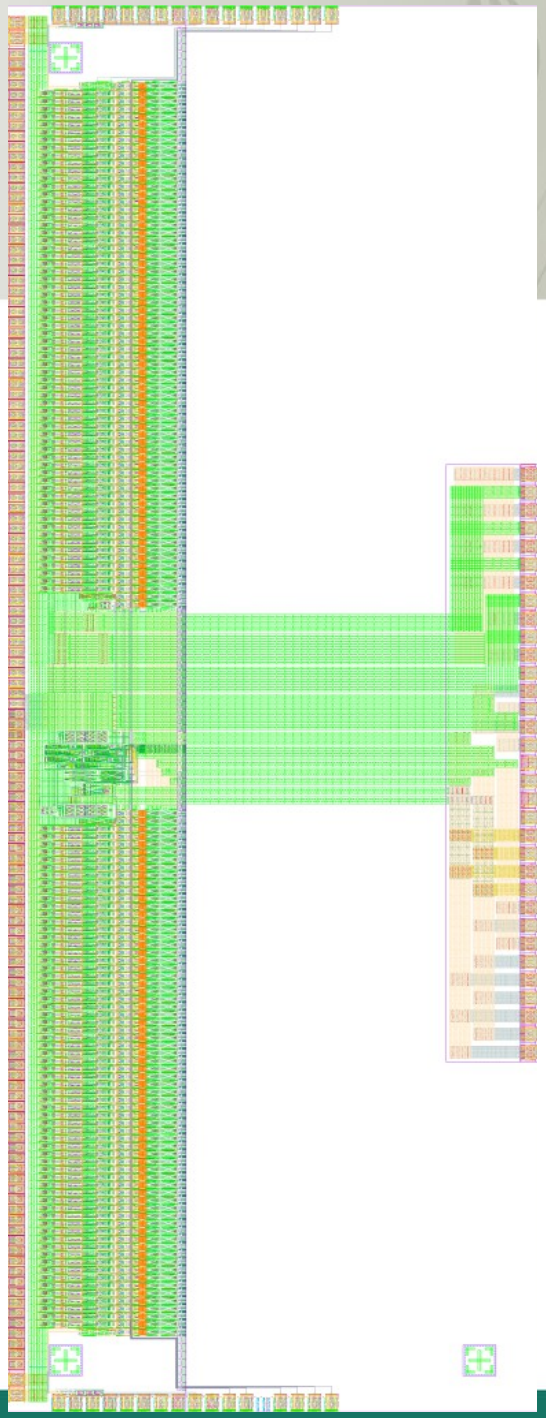


- Power supply and communication provided from the rear edge (right in the picture)
- Debug and test pads located on top and bottom edges
- Pads pitch
  - input (left) 80 um
  - VSSAI (left) 120 um
  - rear edge 140um
  - top & bottom: analogue 100 um
    digital 200um

Layout

Chip dimensions:

- Ana & mixed-mode: 1385um x 10900um
- Digital: **2650**um x 10900um
- Total: **4035**um x **10900**um



Pads used in the design

Analog domain (tpa013nv3):

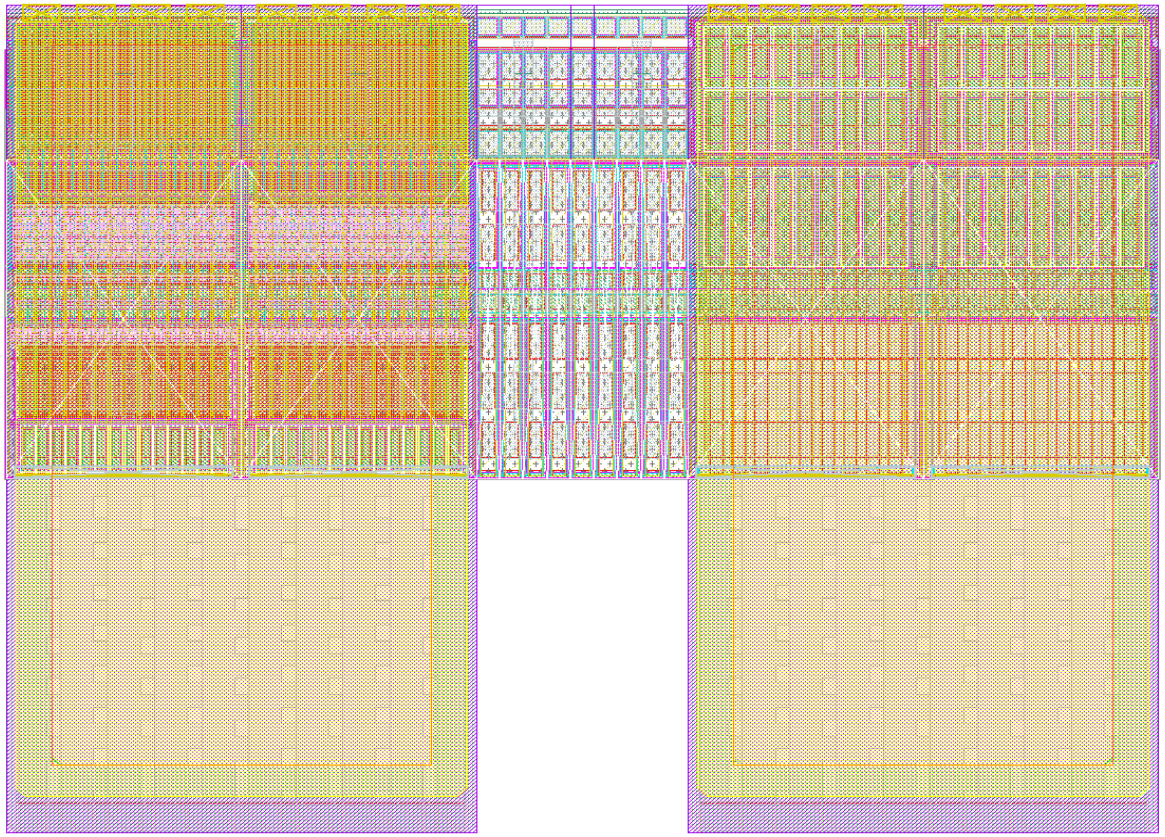
- PVDD3AC – VDDA_BUF
- PVSS3AC – VSSA, VSSAI, VSSA_BUF
- PVSS2AC – VSSPST_BUF
- PDB1AC (with CDM) – 64 INPUTS, VCMA
- PDB1AC (without CDM) – TEST PADS
- PDB3AC – VCMB-D,
- **SOFICS OVT (with CDM)– 64 INPUTS**

Digital domain (tpd013nv2):

- PVDD2CDG – VDDAPST
- PVDD1ANA – VDDA, VDDAPST_IN, VDDVCM, VDDADC, VREFD
- PVSS2CDG – VSSAPST
- PVSS1ANA – VSSA, VSSAI, VSSAPST_IN, VSSVCM, VSSADC

Openings: 68um x 190um (INPUT), 88um x **129**um (SIDE),
96um x 190 um (BACK)

VDDx & VSSx pads



Pad structures doubled
Maximum DC Current per opening 100 mA (in 110°C)

Power distribution v1

Average DC currents (total):

- FE + S2D + Biasing + Monitors: ~200mA
- ADC: ~50mA

Minimum M7(UTM) rail widths (110°C):

- FE: ~ 11um
- ADC: ~3um

Used M7(UTM) rails:

- FE: 98um
- ADC: 2 x 42um

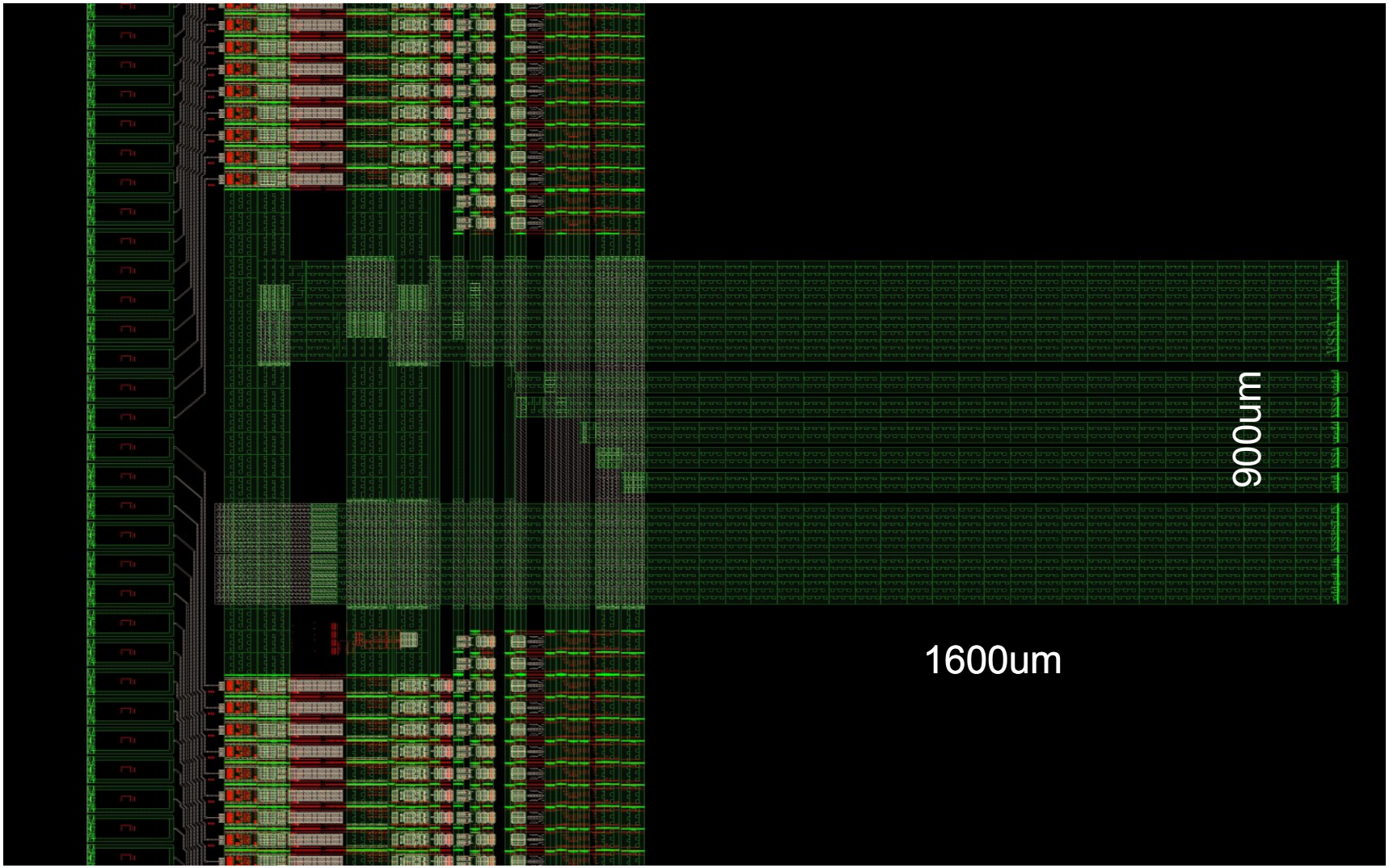
Minimum number of Pads (openings):

- FE: 2
- ADC: 2 x 1 + 1 (VREFD)

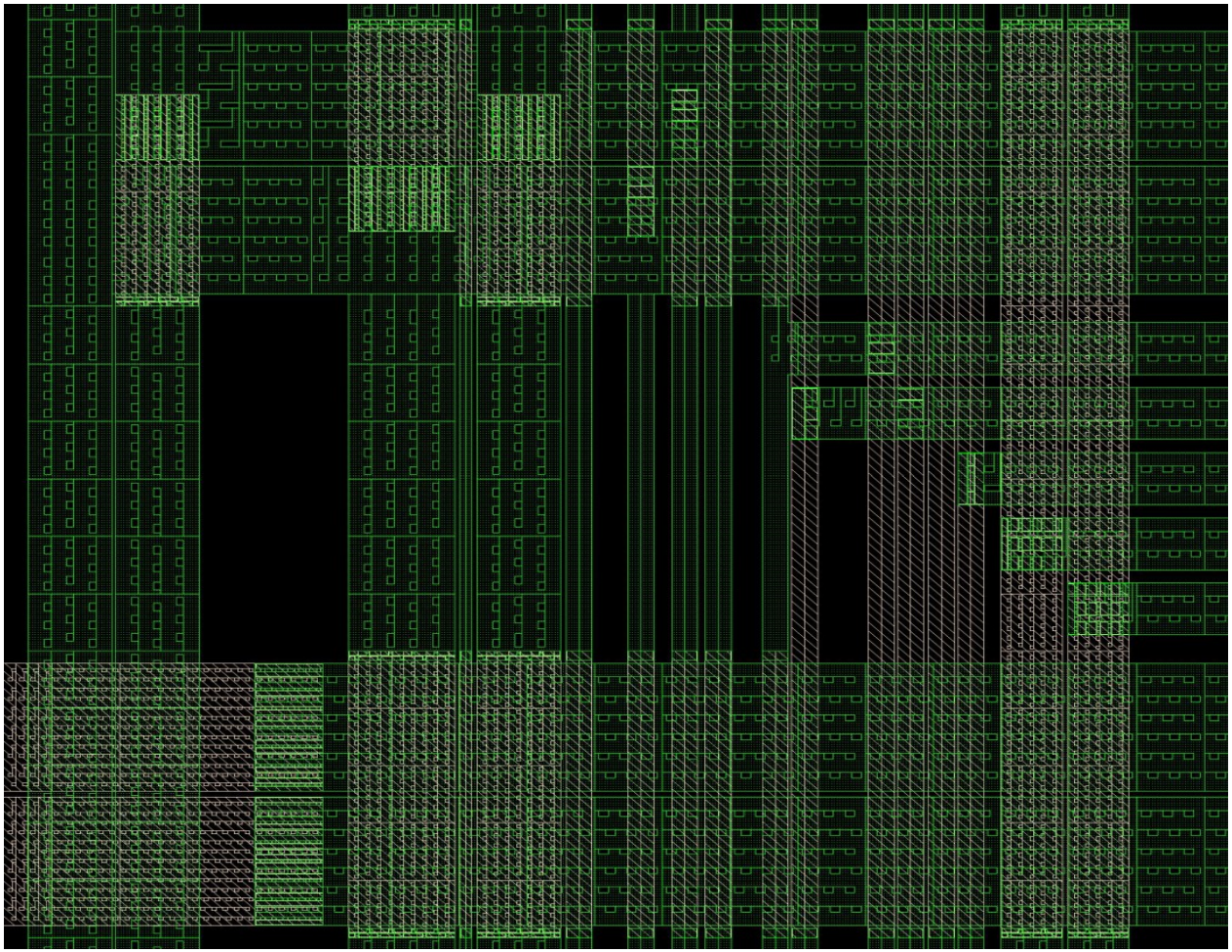
Used number of Pads (openings)

- FE: 2 x 5
- ADC 2 x 2 + 2 (VREFD)

Power distribution v1



Power distribution v1 - details



VDDA

VSSA

FE
2 x 98um

VDDAD

VSSA

VREFD

VDDD

VSSA

ADC
5 x 42um

VDDAPST_IN

INPUT PROTECTION
2 x 98um

VSSPST_IN

2x56um 70um 56um 2x23um 6x23um 2x42um

Power distribution v2

Average DC currents (total):

- FE + S2D + Biasing + Monitors: ~200mA
- ADC: ~50mA

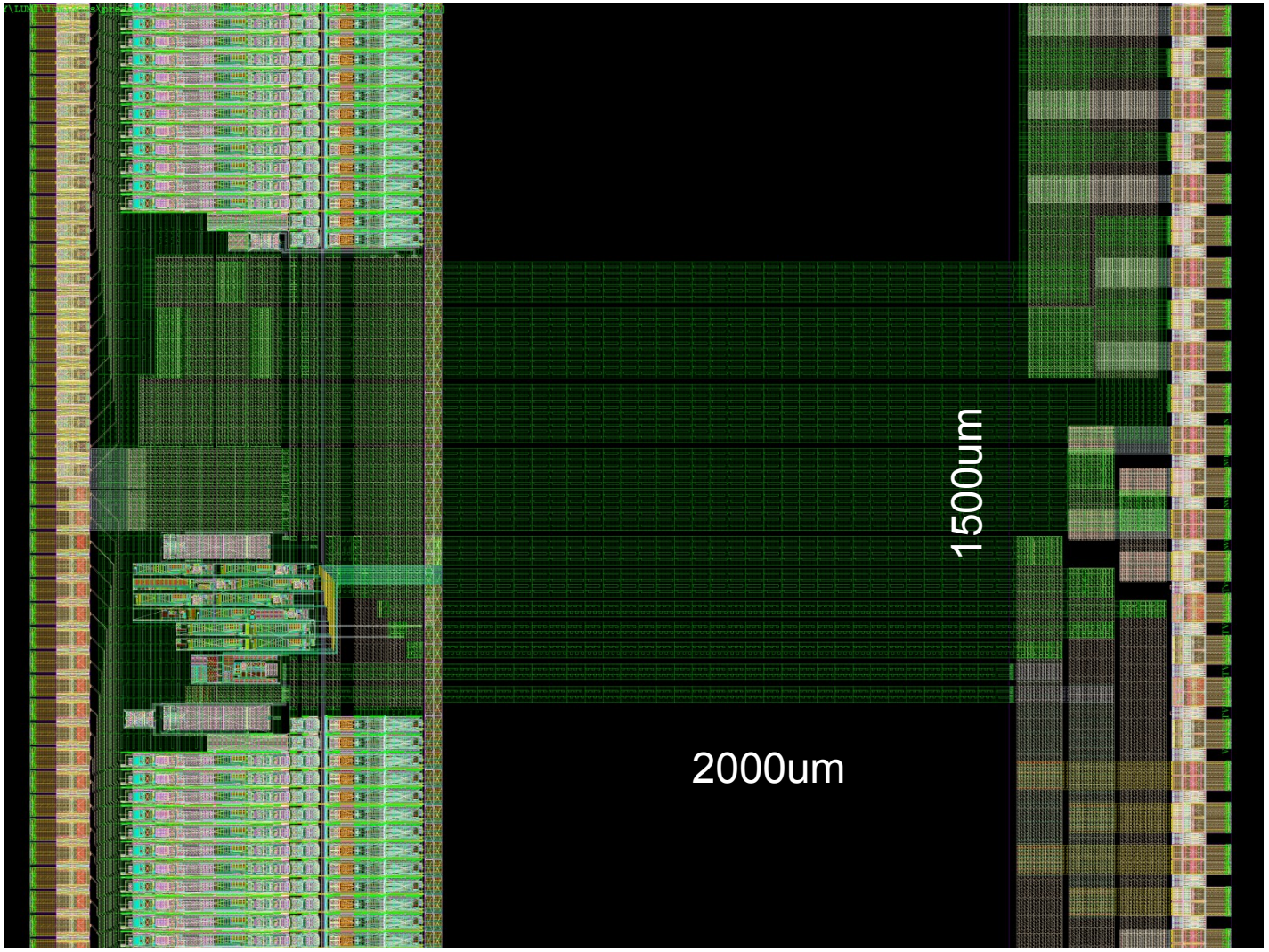
Used M7(UTM) rails:

- FE: 98um + 140um, 168um
- ADC: 2 x 70um, 2 x 42um, 42um
- VCM: 2 x 42um

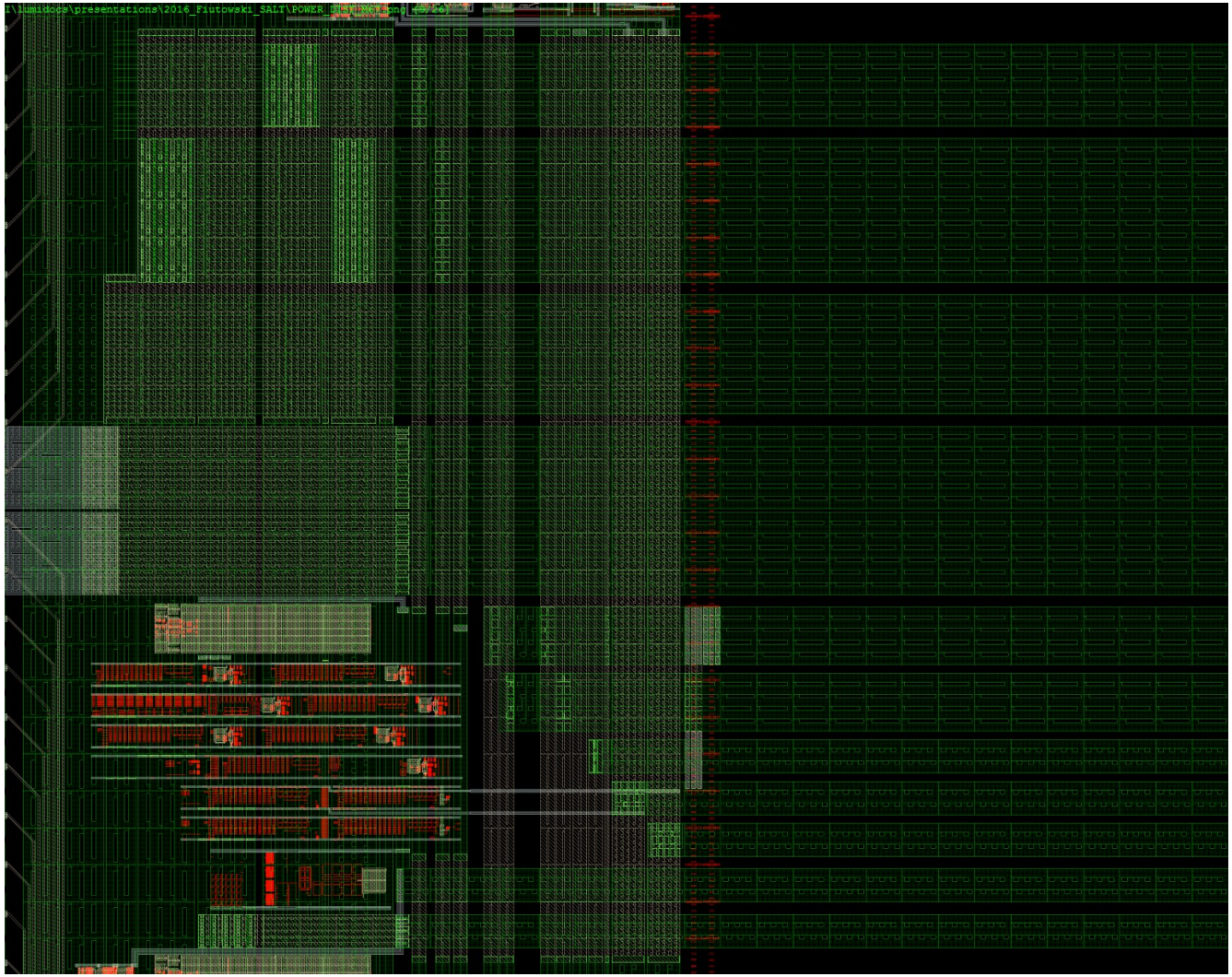
Used number of Pads (openings)

- FE: 6 (VDDA)+ 3 (VSSA) + 3 (VSSAI – back) + 4 (VSSAI – front)
- ADC: 3 (VDDADC) + 4 (VSSADC) + 2 (VREFD)
- VCM: 2 (VDDVCM)+ 2 (VSSVCM)

Power distribution v2



Power distribution v2 - details



VSSA – 98um

VDDA – 168um

VSSAI – 140um+2x98um

VDDAPST_IN – 98um

VSSPST_IN – 98um

VDDADC (ANA) – 70um

VSSADC (ANA) – 70um

VREFD – 42um

VDDADC (DIG) – 42um

VDDADC (DIG) – 42um

VDDVCM – 42um

VSSVCM – 42um

Submission readiness

- Layout of all analogue and mixed-mode blocks is ready
- Power and signals distrubution (wiring) is ready
- Decoupling - simulations in progress