

SALT128 Testing

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Milano, May 18th 2016





Two main branches:

- SALT128 prototype testing
 - PCB similar to the existing one
 - General purpose
 - Compatible with VLDB, COMET, Flex, standalone
 - Immediate production, first priority
- SALT128 production testing
 - To be used with a probe station in the wafer (before dicing)
 - Automate testing as much as possible
 - Specific purpose
 - Intend to construct it around COMET board
 - Interaction with probe station, analysis software, results database, etc
 - Need to design tests (analogue performance, digital functionality, switching coverage, pll performance, PSRR, ADC performance, etc)

Input I need:

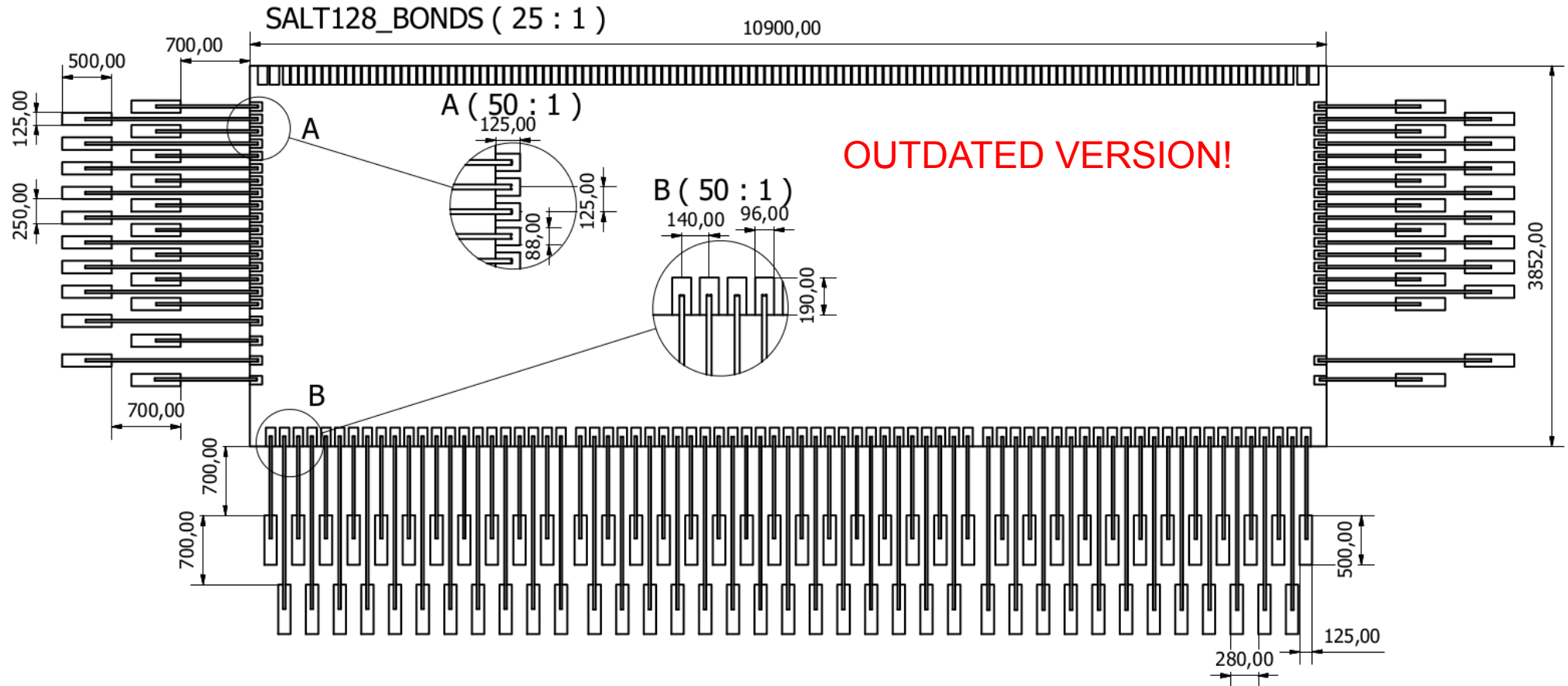
- ASIC: New pinout, exact dimensions, detailed pin functionality ✓
- Detailed list of tests to be done: sort out the changes if any (**I heard common mode?**)
- Feedback: is there anything we would like to change/improve? ✓
- List of cards to deliver: **Who wants them? How many? When?**

Production process only when all input is available: **Today t=0.**

- 3 or 4 weeks for design (inc. circulation, review, ...). Depends on the changes to make
 - **1st or 2nd week of June ?**
- 2 weeks for PCB production (standard procedure) **3rd or 4th week of June ?**
 - ~~1 week express: need to check for availability, very expensive (x2)~~
 - ~~Component sourcing in parallel. It can be slower than 1 week.~~
- 1 week for component soldering (once they start...)
 - Yes, but be aware of availability issues. 1/2 weeks waiting? Outsourcing it?
- 2 days for wire bonding (once they start...)
 - Outsourcing/Volunteers? **Marina volunteered yesterday.**
 - **Ship to Syracuse by mid-July?**

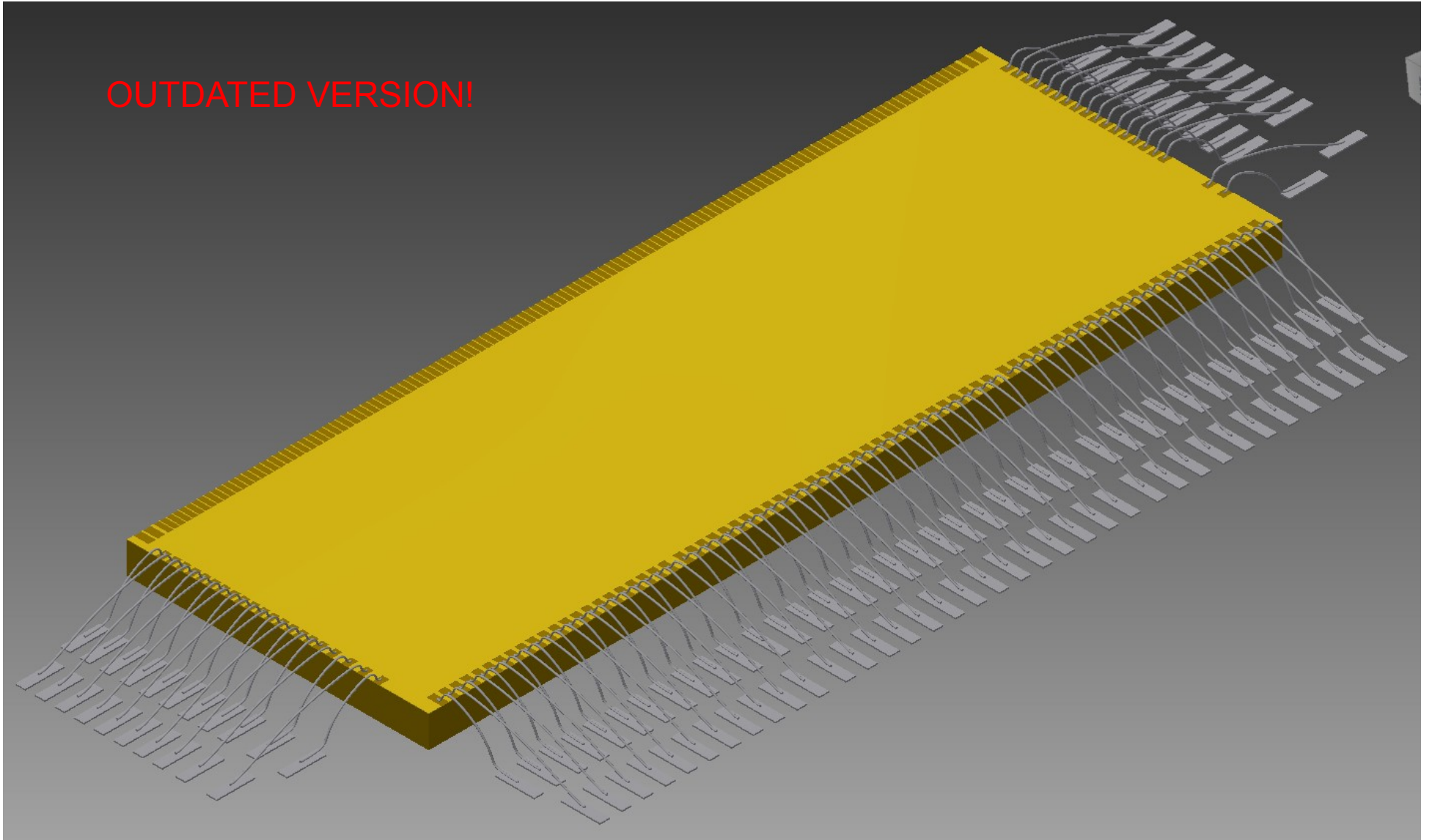
Input I need:

- ASIC: New pinout, exact dimensions, detailed pin functionality (more or less) ✓

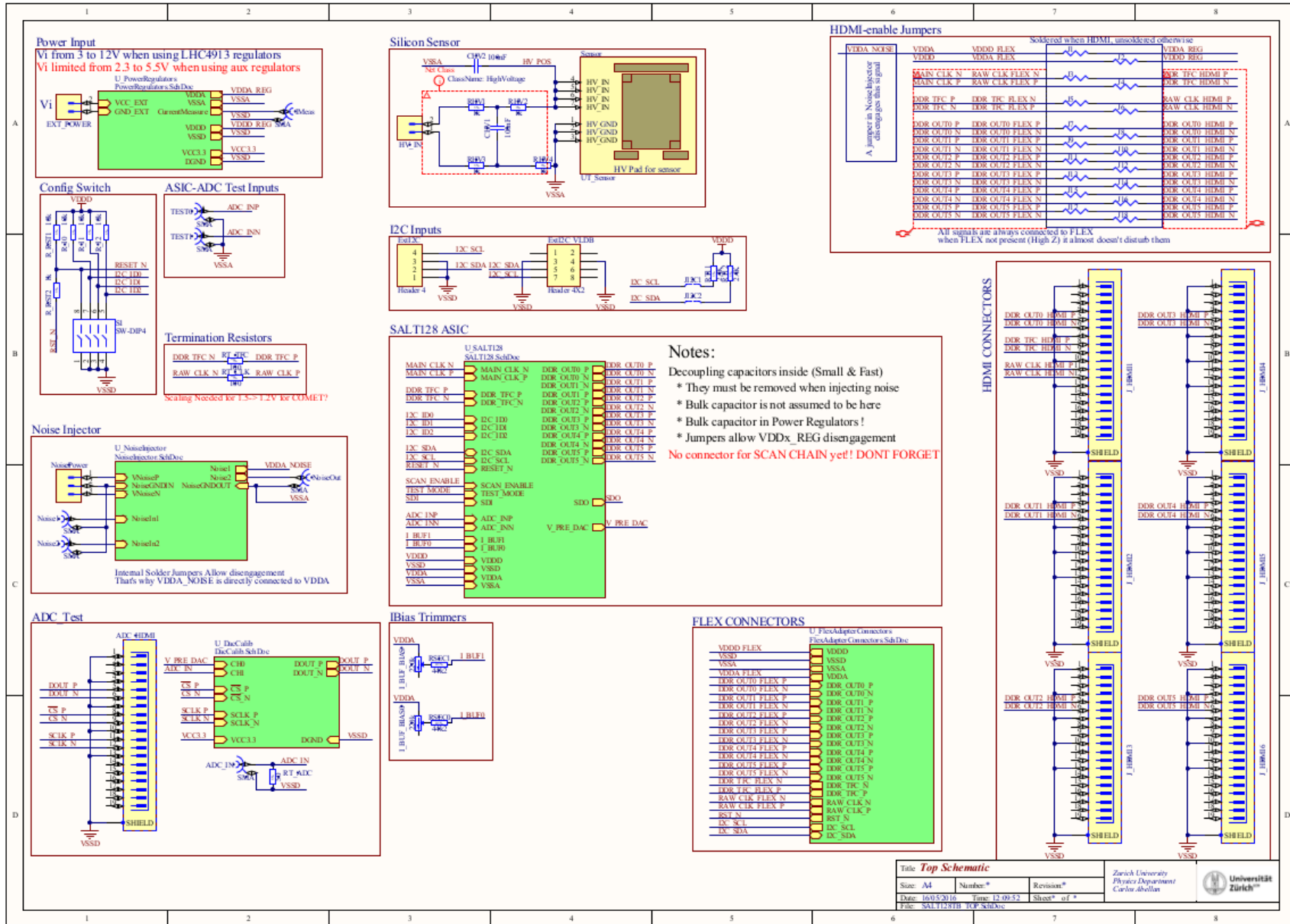


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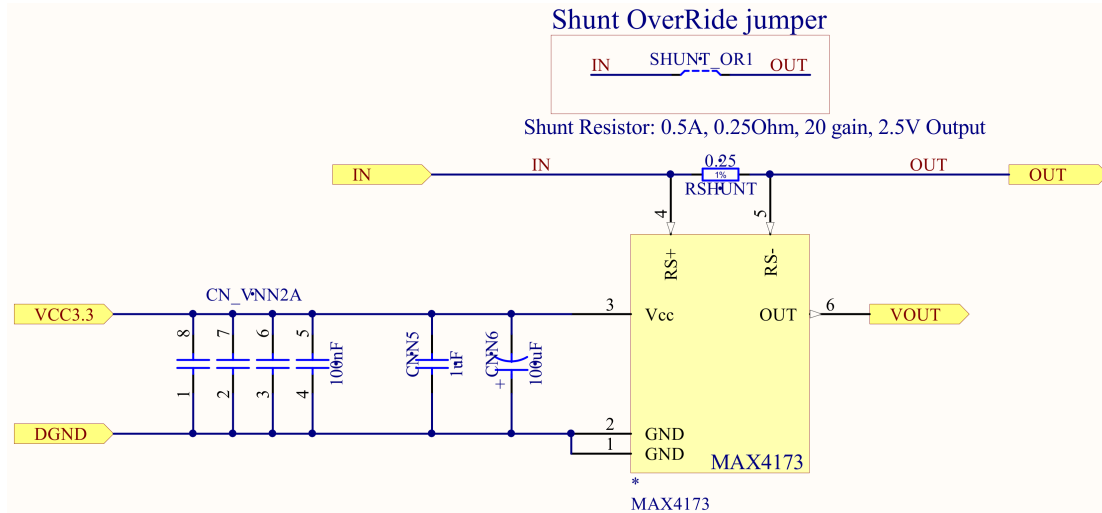
Schematics well advanced:



Title Top Schematic			
Size: A4	Number: *	Revision: *	
Date: 16/05/2016	Time: 12:09:52	Sheet: * of *	
File: SALT128TB_TOP_SchDoc			

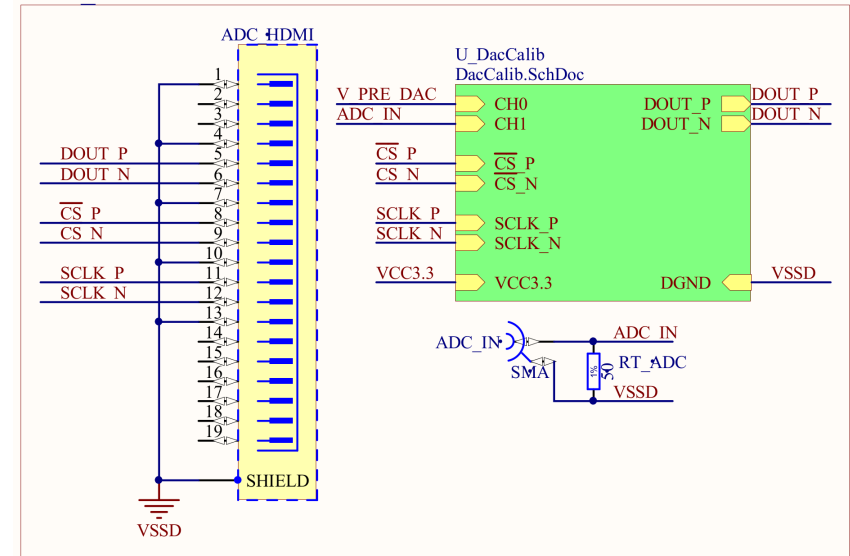
Schematics well advanced. Main changes:

- Less regulators: no one used them anyway...
- Power consumption reading now COTS (MAX4173)



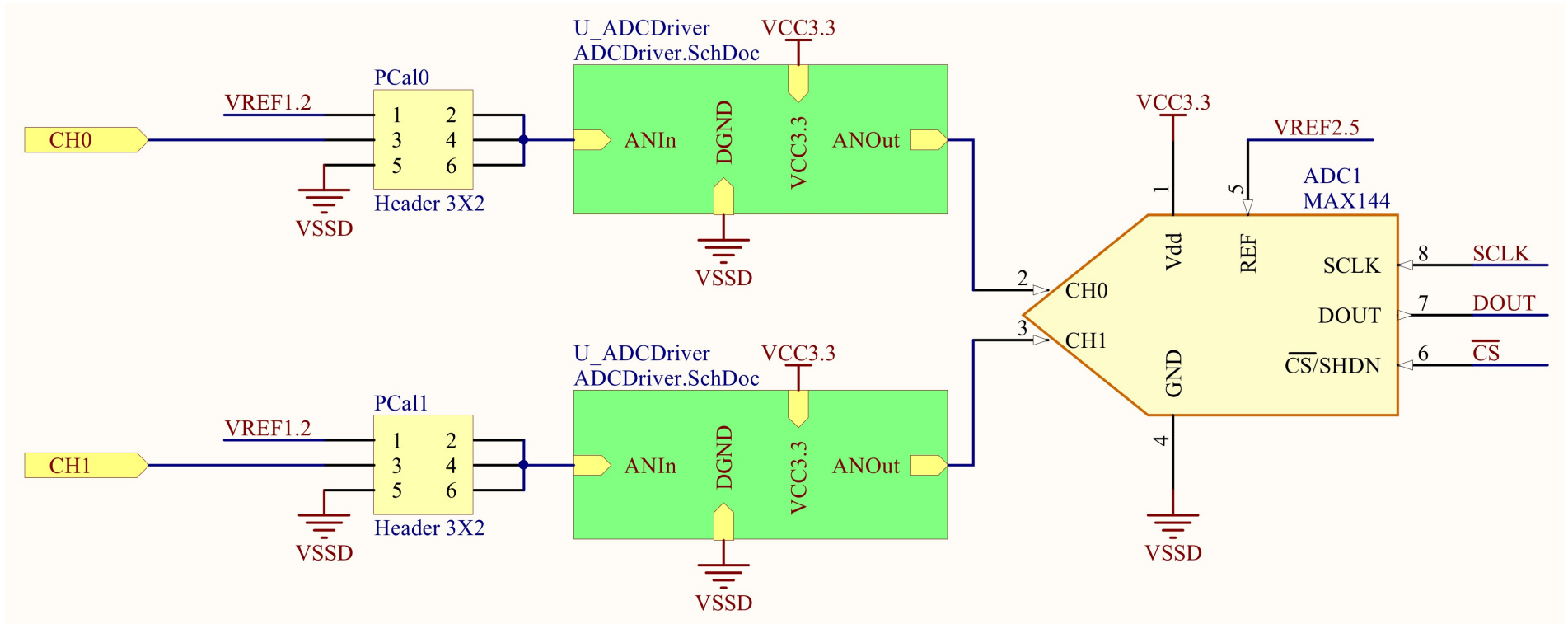
- ASIC now uses 6 e-links instead of 3: where should I map them?
- Profit to test the ADC that will be used for production testing. The e-link configuration is compatible with the ones for SALT.
 - We need to sample 12 channels!!
 - Since it's DC, maybe a relay?

ADC_Test



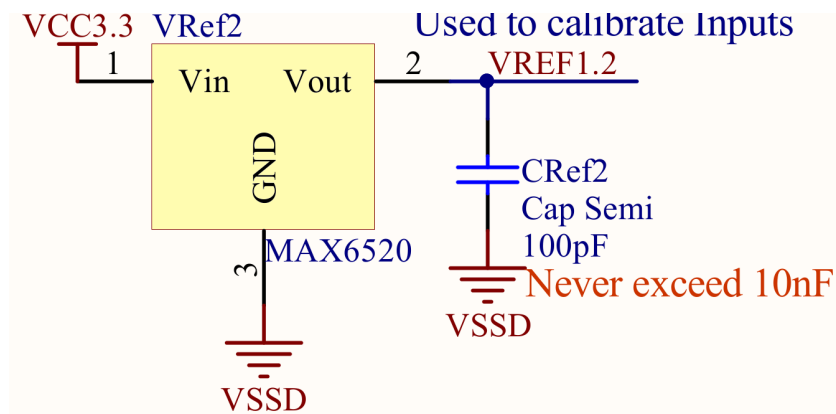
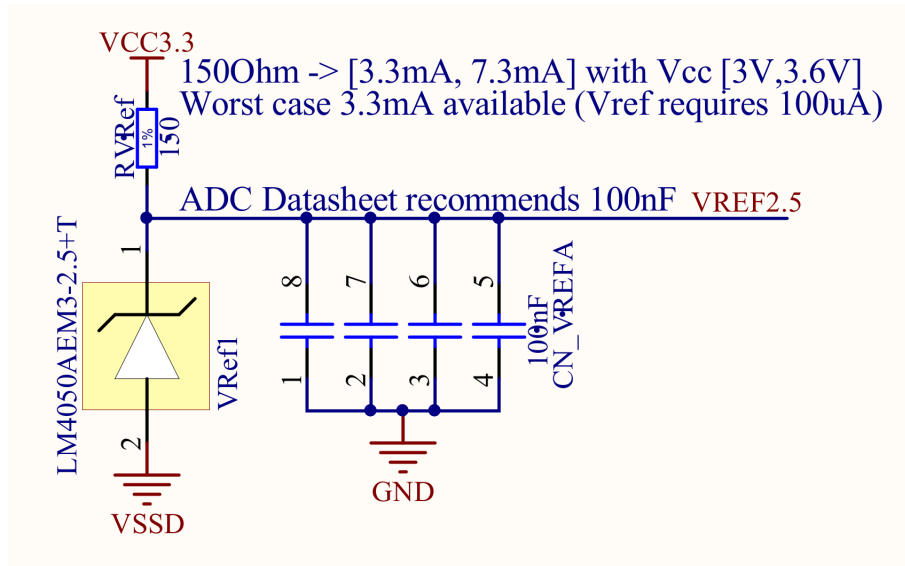
ADC Testing:

- We use a MAX144 2 channel 12 bit @ 100KSPS ADC to sample a 5 bit DAC (could seem like an overkill)

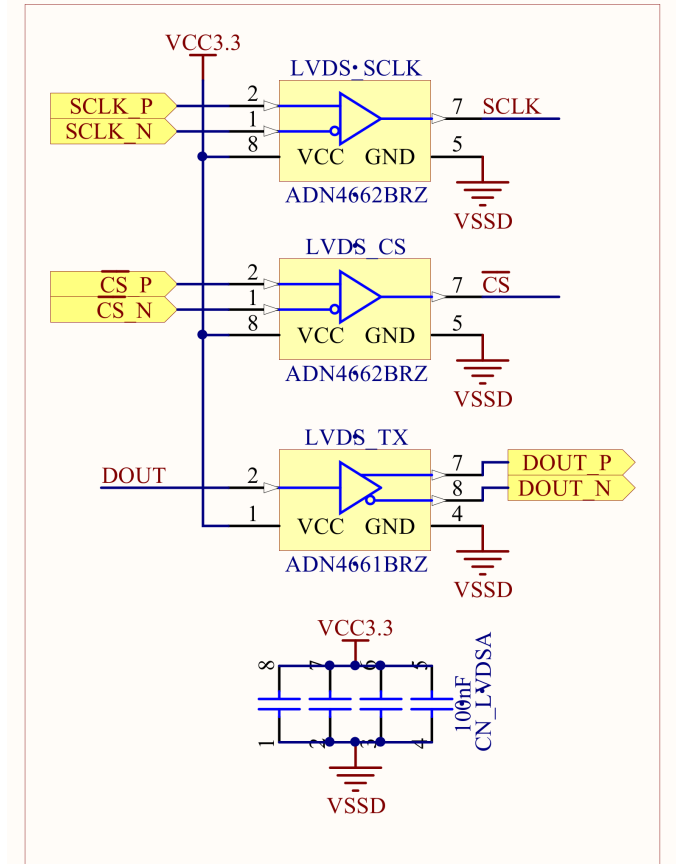


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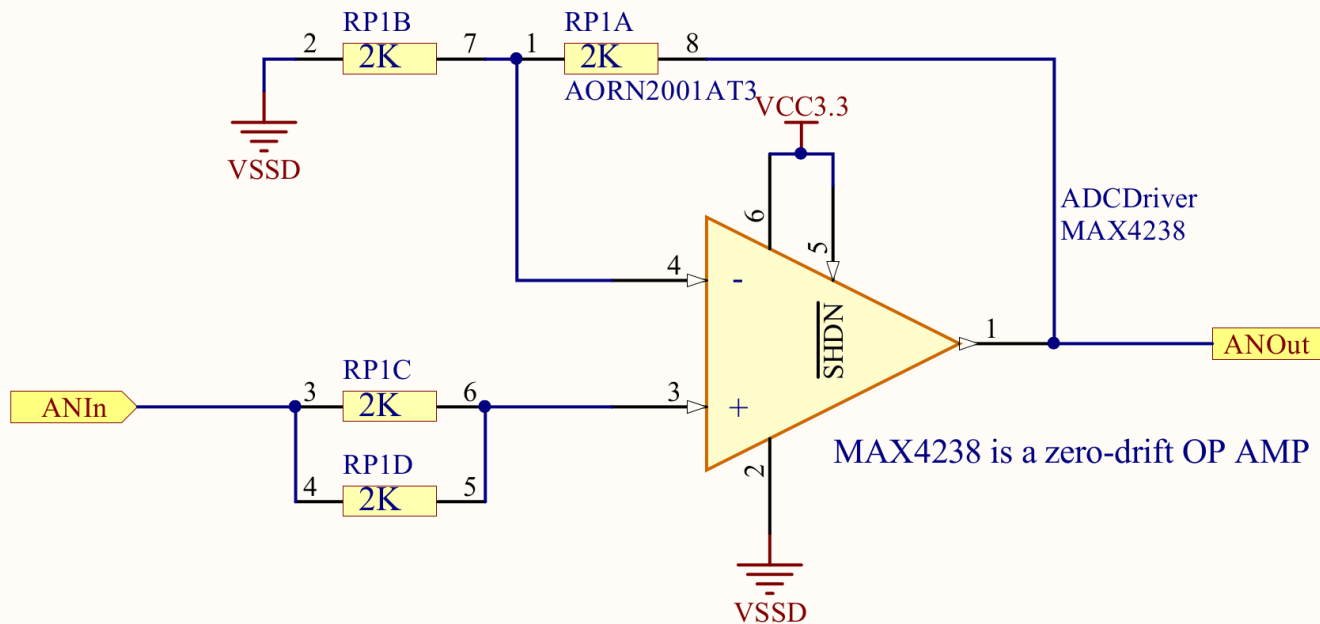
LVDS Transceivers (RX and TX)



ADC Testing:

- We use a MAX4238 (Zero drift) together with precision resistors.
- x2 gain and only used from 0.2V to 0.8V gives better linearity. Uses a compensated V source to calibrate it further.
 - This gives a [0.4, 1.6] output range (smaller than ADC dynamics, but we have many bits left).

AORN2001AT3 is a 4xResistance array that has 0.1% precision and very low PTC (package ensures similar temperatures so constant ratio)



Production process similar to the proto_TB one:

- [New design (I don't dare guesstimating) + 2 weeks for PCB production (standard procedure)+1/2 weeks for component soldering (once they start...)] * 1.5 safety factor
 - Prototype Test Board (a big part can be reused) +
 - ADC to sample and calibrate internal DACs (+ OP amps, + ...)
 - Precise power consumption measurement
 - Any other requests? (Depends on what you want to t[✓]) **Now or never?** ✓
- Probe card: I never designed one. I need to learn the basics, find a company that does it, get time and price estimations, ... Anyone with experience can help me with that?
 - I talked to the people who designed the test system for, some conclusions:
 - Their card has 110 needles (to have an order of magnitude): **(We want 247!!)**
 - 5x Boards = around 12k€
 - We really want to be sure it's perfect before submitting
 - Delivery time estimated in 9 weeks **once everything is accepted**
 - We have to foresee a pipeline not to be stopped while we wait
 - The manufacturer keeps some manufacturing information private
 - We give instructions and they give back closed products, will require several iterations to make sure there is no communication failure (we only want to do it once!)

Input I need:

- Results of the prototype testing: will drive the production tests
- Full-featured COMET board + adequate mini-HDMI daughter boards.
- **Detailed list of tests to be done**, to plan for:
 - Analysis software: Chris Betancourt, Iaroslava Bezshyiko (from Zurich). Online data analysis, report generation, result management, ...
 - Hardware design: automate the measurements (Carlos)
 - Probe card + reuse as much as possible the proto_TB design
 - Probe station interface (MariaPilar)
 - We never operated one. Will require some time to learn.
 - System wide design:
 - Chuck? Wafer manipulation? Clean room equipment? ESD cautions?
 - **HRRR**, logistics, coordination with stave production...
 - Fact: 1 second of test/ ASIC x 6kASICs = 1.67h of testing
 - 10 mins of test / ASIC = 25 working weeks = 6.25 months
(8h/day, 5 day/week)

What we're aiming for:

A Large Ion Collider Experiment

Setup at CERN

Probe card

Wafer

Probe station control

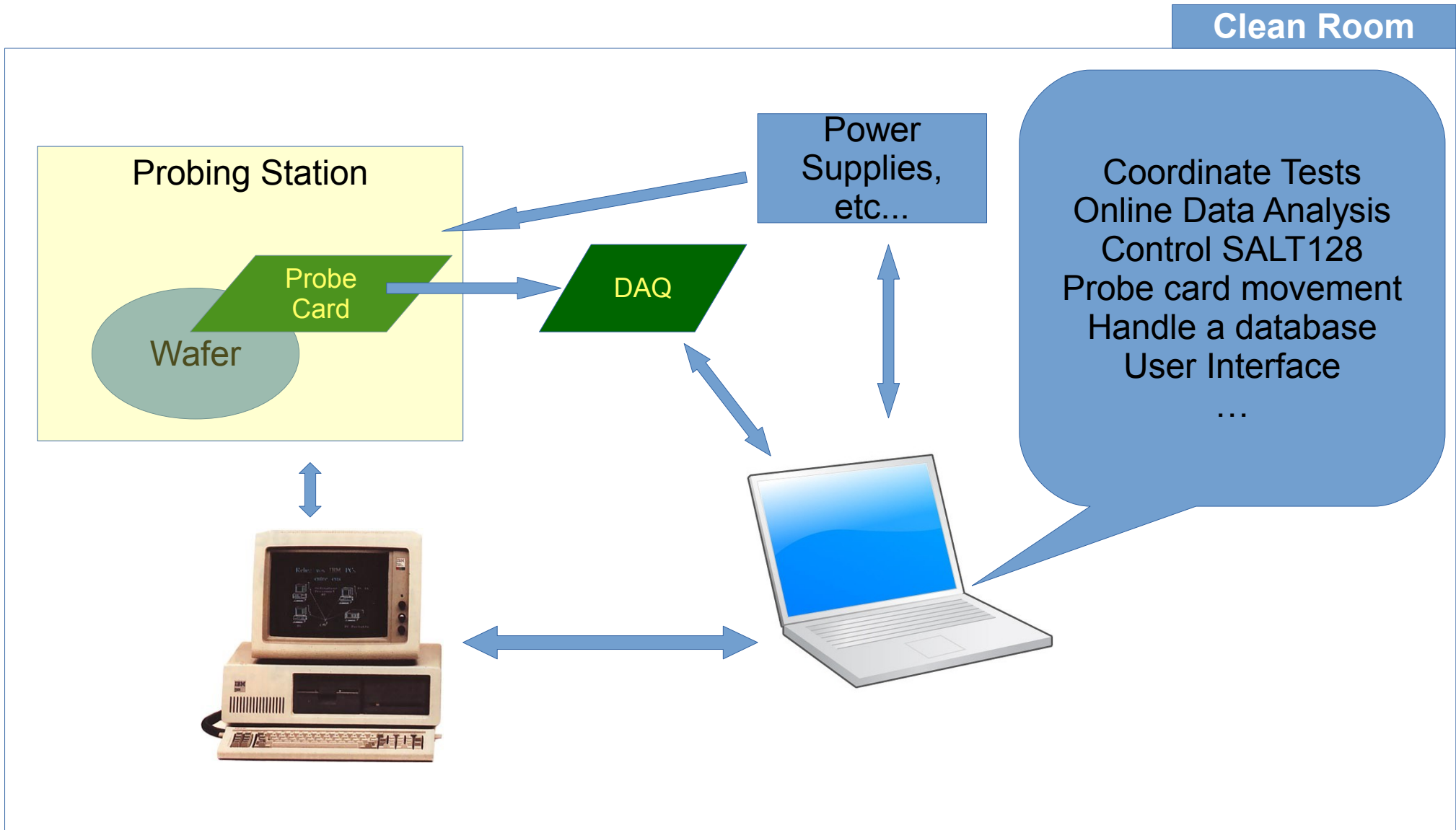
DAQ board + PC

Testing computer

Probecard needles

5th ALICE ITS, MFT and O2 Meeting, P. Riedler

What we're aiming for:



For the prototype testing:

- Where should I put the extra pairs? (Fit cable mapping, ...)
- Will upload schematics to Twiki.
- Need to fix a date for the schematic review.
- A couple of weeks for routing + PCB review
- Production delays

For the production testing:

- Any help from experienced people will be highly appreciated
- I already contacted other groups at CERN who did it, looks like it will take some work
 - 9 weeks production delay!!
 - Very expensive, no room for failure... (will be even slower)
- Full system design: analysis SW, control SW, HW tools, procedures, ...

– Detailed list of tests to be done

- We're going to be busy quite some time with that.

