The UT Electronics Slice Test Plan & Preparation At Syracuse

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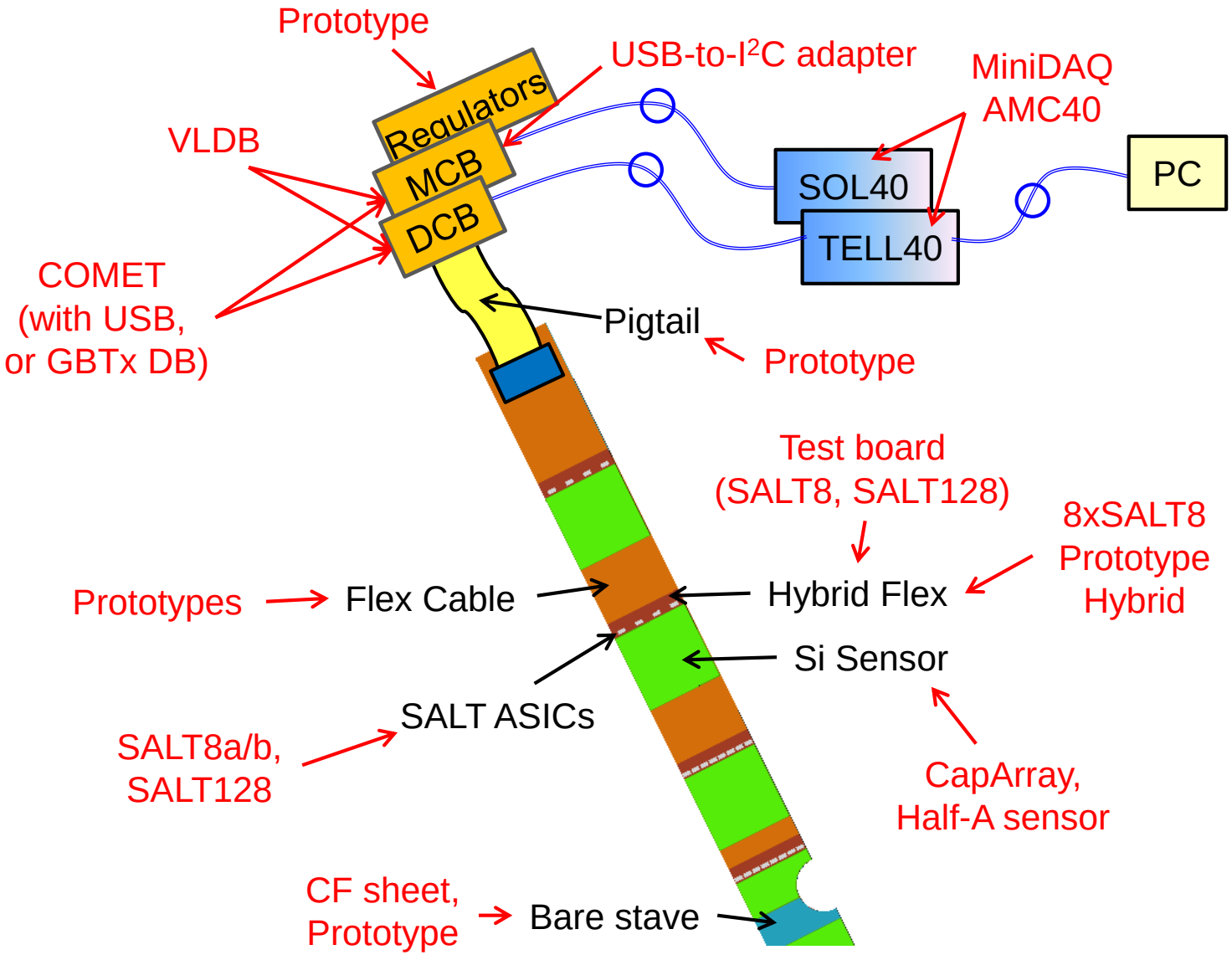
Motivation of Electronics Slice Test

- The UT electronics slice test system is crucial in validating the whole readout scheme, testing and optimizing design of major components.
- We want to test functionalities of individual components and measure their performance when signal and LV/HV powers are routed according to the baseline design of the UT readout system.
- Individual studies include:
  - Check the data integrity in the system, measure signal to noise ratio with baseline configuration.
  - Study power connection, grounding & shielding schemes, measure signal coupling, noise pickup with different configurations.
  - Check digital signal quality in the flex cables, pigtails, & optical fibers by measuring eye diagram and bit error rate.
  - Test ECS protocol and determine: whether the single-ended I^2C works with the expected voltage drop; whether it introduces large noise to the signal; & whether an alternative protocol is needed.

Major Components of The Readout System



Prototypes & Substitutes

Final		Substitutes & Prototypes		
Sensor		CapArray	Half-A	
SALT		SALT8a	SALT8b	SALT128
Hybrid		SALT8 Testboard	SALT128 Testboard	Hybrid_8x8
Stiffener				
Wirebonds		4-ASIC Ada	8-ASIC Ada	
Flex cable		Prototype_1	Prototype_2	Prototype_3
Pigtail		MegArray2ERF8	MegAda	Prototype
Backplane				Prototype
MCB	**ECS**	VLDB	I2C Adapter	
	TFC		COMET with USB interface	COMET + GBTx DB
DCB				
Opt. Fiber		Sample		
TELL40		MiniDAQ1 / AMC40		MiniDAQ2 / PCIe40
SOL40				
Bare Stave		CF sheet	Prototype	
LV Regulator		Prototype		

Use components as close to the final design as possible for realistic tests.

Green color components are available, yellow components are to be produced.

Components of Phase I Slice Test

Final		Substitutes & Prototypes		
Sensor		CapArray	Half-A	
SALT		SALT8a	SALT8b	SALT128
Hybrid		SALT8 Testboard	SALT128 Testboard	Hybrid_8x8
Stiffener				
Wirebonds		4-ASIC Ada	8-ASIC Ada	
Flex cable		Prototype_1	Prototype_2	Prototype_3
Pigtail		MegArray2ERF8	MegAda	Prototype
Backplane				Prototype
MCB	**ECS**	VLDB	I2C Adapter	
	TFC		COMET with USB interface	COMET + GBTx DB
DCB				
Opt. Fiber		Sample		
TELL40		MiniDAQ1		MiniDAQ2
SOL40				
Bare Stave		CF sheet	Prototype	
LV Regulator		Prototype		

MegAda board is now available. We will start phase I slice test right after this workshop.

Objectives of Phase I Slice Test

- In phase I slice test we want to
  - Validate signal integrity with a few differential lines.
  - Investigate effects of I^2C cross talk.
  - Investigate effects of digital analog cross talk.
  - Study general noise immunity.

- Now we have all major components. Phase I test will start right after this workshop.
- If components for phase II are available, some phase I tests may be done directly on the phase II setup.

Components of Phase II Slice Test

Final		Substitutes & Prototypes		
Sensor		CapArray	Half-A	
SALT		SALT8a	SALT8b	SALT128
Hybrid		SALT8 Testboard	SALT128 Testboard	Hybrid_8x8
Stiffener				Prototype
Wirebonds		4-ASIC-Ada	8-ASIC Ada	
Flex cable		Prototype_1	Prototype_2	Prototype_3
Pigtail		MegArray2ERF8	MegAda	Prototype
Backplane				Prototype
MCB	**ECS**	VLDB	I2C Adapter	
	TFC		COMET with USB interface	COMET + GBTx DB
DCB				
Opt. Fiber		Sample		
TELL40		MiniDAQ1		MiniDAQ2
SOL40				
Bare Stave		CF sheet	Prototype	
LV Regulator		Prototype		

A prototype hybrid of 8 SALT8b ASICs to replace the SALT8 testboard.

A COMET board that has GBTx DB + a USB-I^2C adapter to replace VLDB.

We may use prototype bare stave instead of a CF sheet.

Goals of Phase II Slice Test

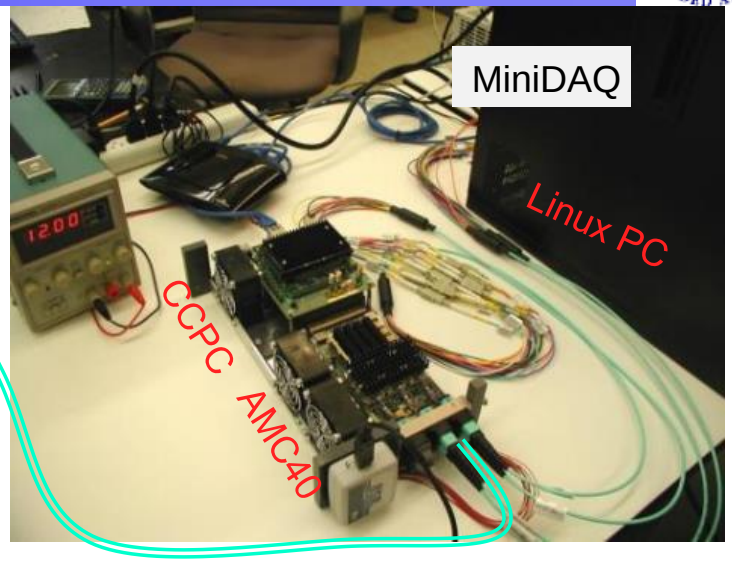
- In phase II test we want to
  - Reproduce tests in phase I with a more realistic setup.
  - Validate the COMET board, especially since it has a fresh implementation of GBTx, & VTRx communication.
  - Test HV distribution system.
  - Generate a realistic voltage drop between the COMET & the FE hybrid to determine if the I^2C communication works.
  - Study signal interference between ASICs.

- Majority of phase I & II tests need to be done before the electronics review on July 1st. There is ~ 1 month left for component production, system setup & test.

Slice Test Phase 3+

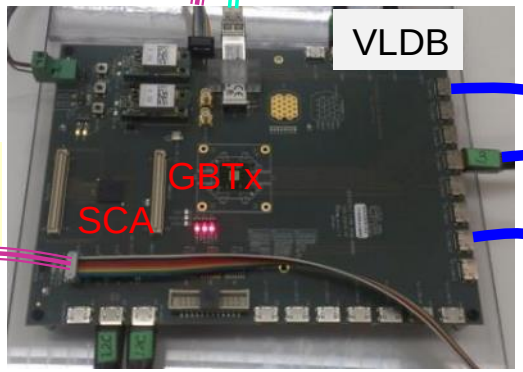
- We will update the slice test plan after phase II basing on how prototype components progress.
- With SALT128 we want to study noise performance, power consumption, channel coupling, …
- Prototype pigtail cable & back plane will be added to the system for signal quality & noise performance measurements etc.
- Use more than one hybrid to measure inter-hybrid interference, and maybe also between 2 sides of stave.
- …

Phase I Slice Test Setup @ Syracuse



I²C signal to config GBTx

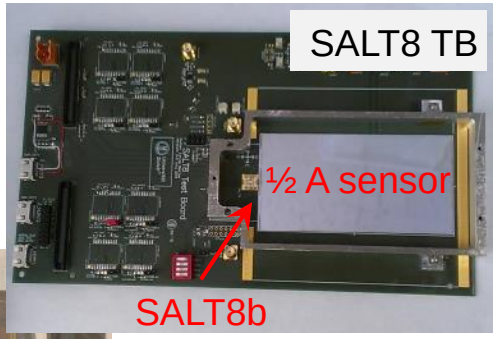
GBT frame data (TFC/ECS & event)



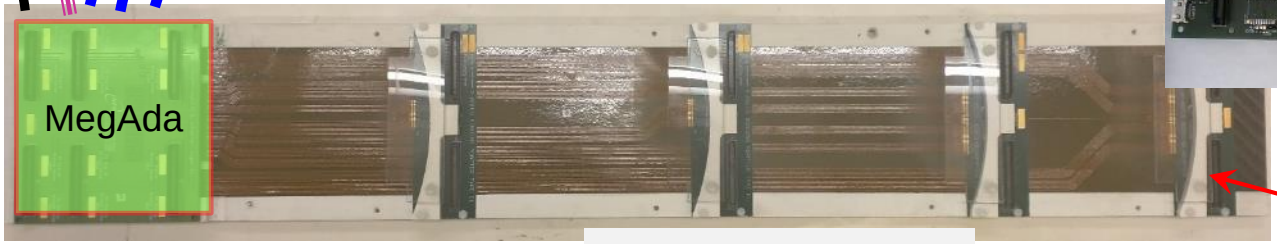
I²C signal to config SALT8

LV

E-link data 320 Mbps



Available now



Flex Cable Assembly

Bonding Adapter

Status of Other Major Components

- Status of major components to be added in the phase II slice test and tests later are presented at this workshop
  - COMET with GBTx daughter card (by Will Parker).
  - Hybrid of 8 SALT8 & new flex cable (by Mauro Citterio)
  - SALT128 (by Marek Idzik, Krzysztof Swientek, Tomasz Fiutowski)
  - SALT128 test board (by Carlos Abellan Beteta)
  - Pigtail cable (by Maria Del Pilar Peco Regales)
  - Prototype bare stave (by Ray Mountain)

- Other components:
  - MegAda: It is available now. I will bring 1 or 2 back to Syracuse.
  - MiniDAQ2: One system is purchased for UMD, available this summer.
  - LV regulator: We have one prototype from Brian Hamilton.

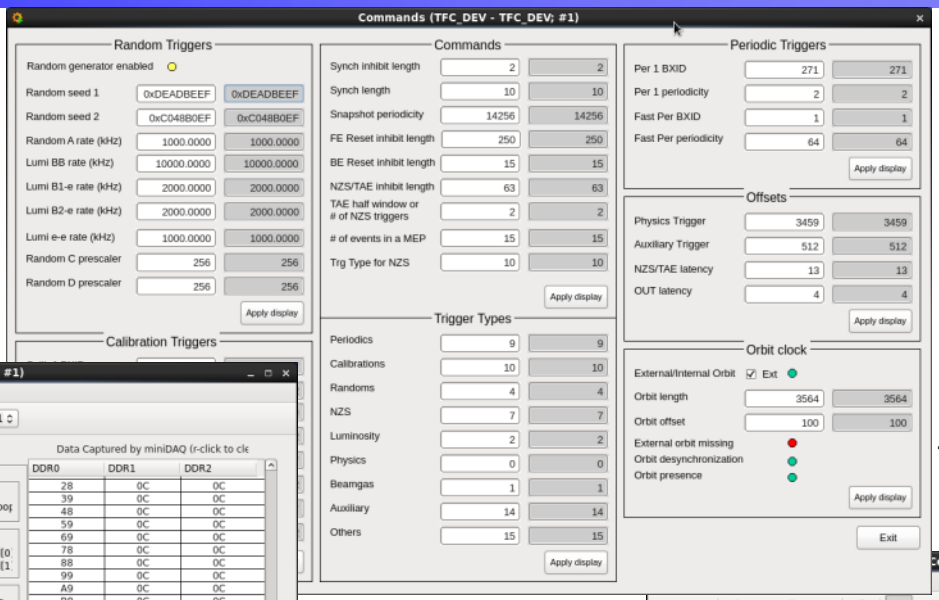
The DAQ System

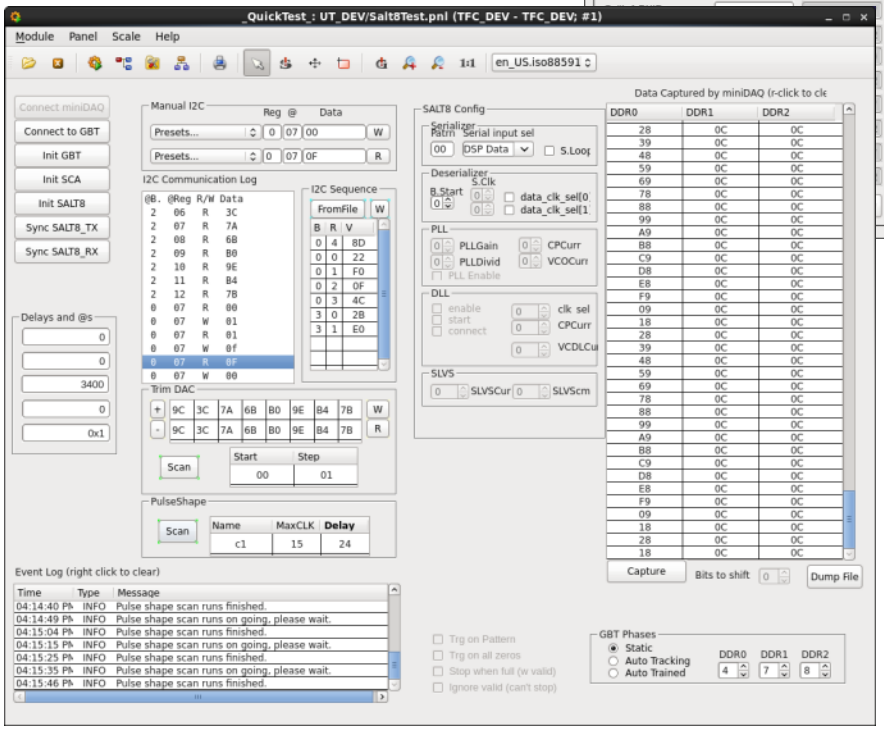
- The Linux PC
  - PVSS control panels sends out configuration data to CCPC via an 1 Gbps Ethernet cable.
  - A process running on PC reads event data in MEP from AMC40 via a 10 Gbps optical line, saves data in files for further analysis, or has real time analysis to avoid huge data files.
  - Quartus loads firmware to AMC40 FPGA via a USB-to-jtag connection.
  - Configures GBTx on VLDB via USB-to-I^2C adapter.
- CCPC on the MiniDAQ system
  - Access register of FPGA on AMC40, write or read back register values of configuration.
- AMC40 on the MiniDAQ system
  - A special firmware is implemented to combine TFC/ECS & event data in 1 pair of optical fibers, to & from VLDB separately.
  - The GBT frame to VLDB consists of GBTx config (IC), SALT8 config (EC), & TFC.
  - The GBT frame from VLDB contains data from all input e-ports on VLDB & IC/EC read back.
  - AMC40 generates MEP from VLDB GBT frame data and sends to PC via a 10 Gbps optical.
- On VLDB
  - GBTx is configured from the USB-to-I^2C adapter, or from IC data.
  - GBT-SCA communicates to GBTx of EC data & relay in I^2C protocol with SALT8.
  - E-ports operate at 320 Mbps, send TFC/CLK to SALT8, & receive event packets.

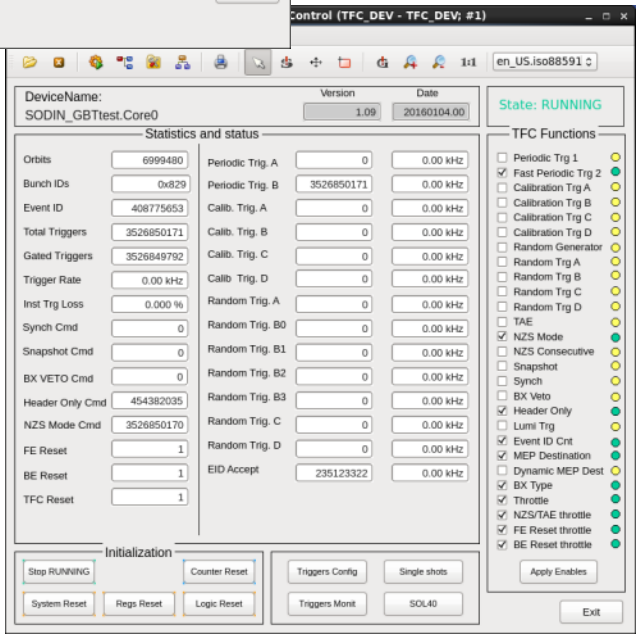
PVSS Control Panels

8-bit TFC for UT

Calib, Synch, Snapshot, BxVeto, NZS, HeaderOnly, FEReset, BXReset







TFC control panels by Federico Alessio

SALT8 test control panel started by Carlos Abellan

Measure System Performance

- Besides of validating the readout chain, we also want to measure the system performance in analog domain and digital domain.

- Static measurements of LV voltage drop & power consumption.
- Noise of individual channels & common mode for high frequency effects. Some effects may also show up in the coupling of adjacent channels.

- We can measure bit error rate (BER) of the digital signal to check the quality of overall communication.
- We can also measure eye diagrams in individual components.

Requirements of BER Measurement Method

- The bit error rate (BER) measurement program runs on the Linux PC. It has following requirements:
- The program analyzes the MEP data at real time to avoid saving huge files, as the data rate per ASIC is ~ 0.12 GByte/s. We need to run in hours to measure the very small BER value.
- The analysis algorithm has to be simple & fast, since events come in at 40 MHz rate. For a 3.2 GHz CPU, there is only 80 cycles per event.
- It needs an accurate determination on whether or not the data received at the end of readout chain is exactly what was sent out from the head.

Bit Error Rate Measurement

- In a first attempt we configure SALT8b to send out Synch package for every clock cycle, and check only Bxid[3:0].

Eport 0 (8-bit)		Eport 1 (8-bit)	Eport 2 (8-bit)		
12-bit BXID			Synch pattern		
Bxid[11:8]	Bxid[7:4]	Bxid[3:0]	Patt[11:8]	Patt[7:4]	Patt[3:0]

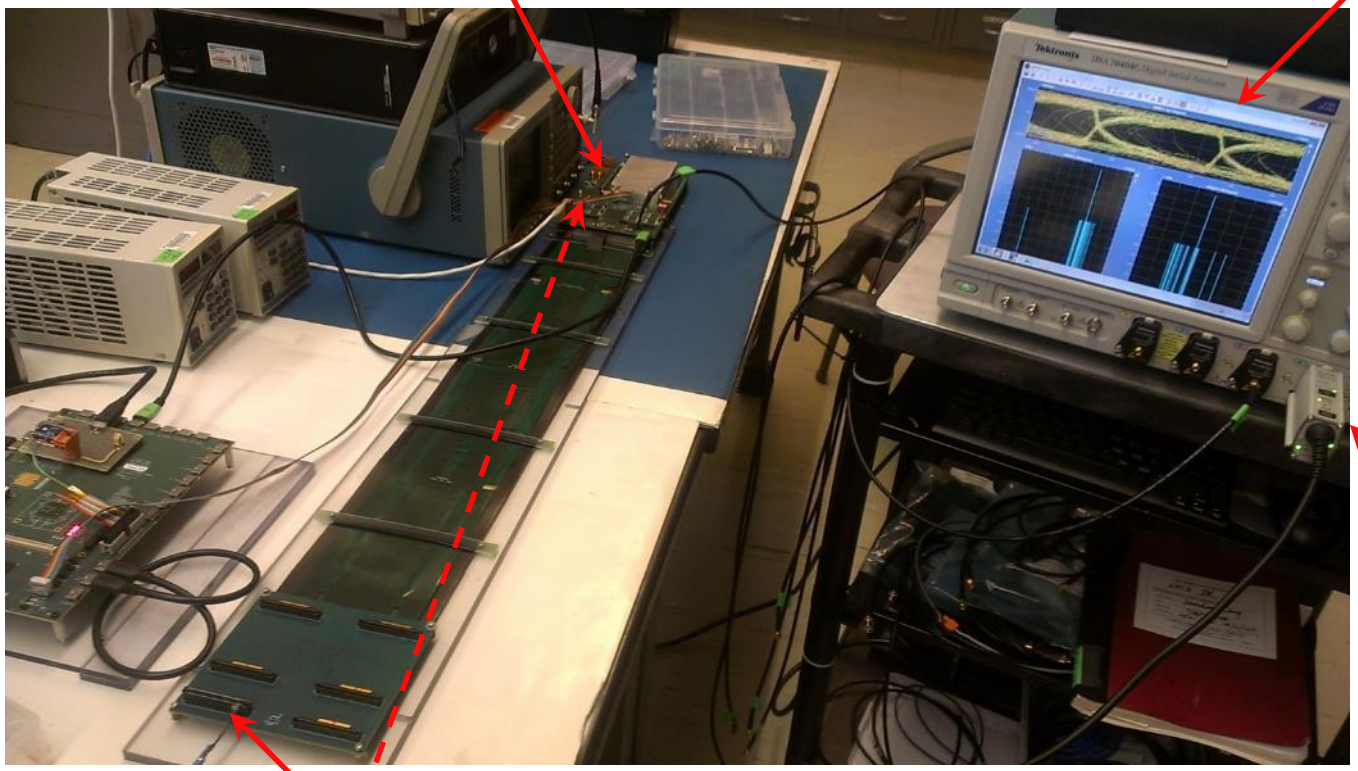
- The BER is expected to be very small. So from previous events we determine what Bxid[3:0] should be in the current event.
- Bxid[3:0] signal may be affected by Bxid[11:8], Patt[11], Patt[8], & Patt[7:4].
- Bxid[11:8] can have all different values, independent of Bxid[3:0] value. We can set Patt[11], Patt[8], & Patt[7:4] to different values in different runs.
- Thus we can measure the true BER, check bits at a rate of 5.76×10^{11} bits per hour.

- In a slice system without flex cable, with timing optimized, we measured the BER of the system to be 0.

Eye Diagram Setup

SALT8b Testboard modified
for eye diagram test

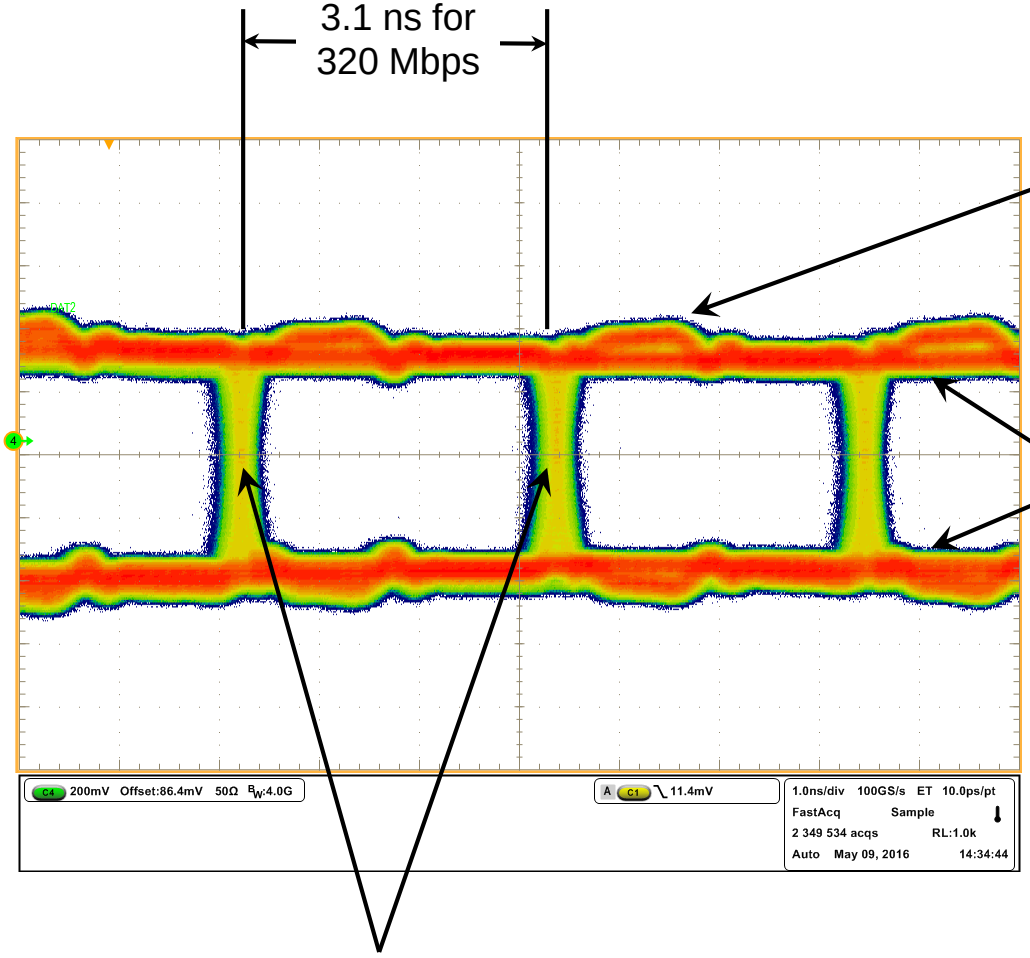
Tektronix
DSA 70404C



Tektronix P7504
LVDS probe

A ERM8 connector with a
modified micro-coax soldering tip

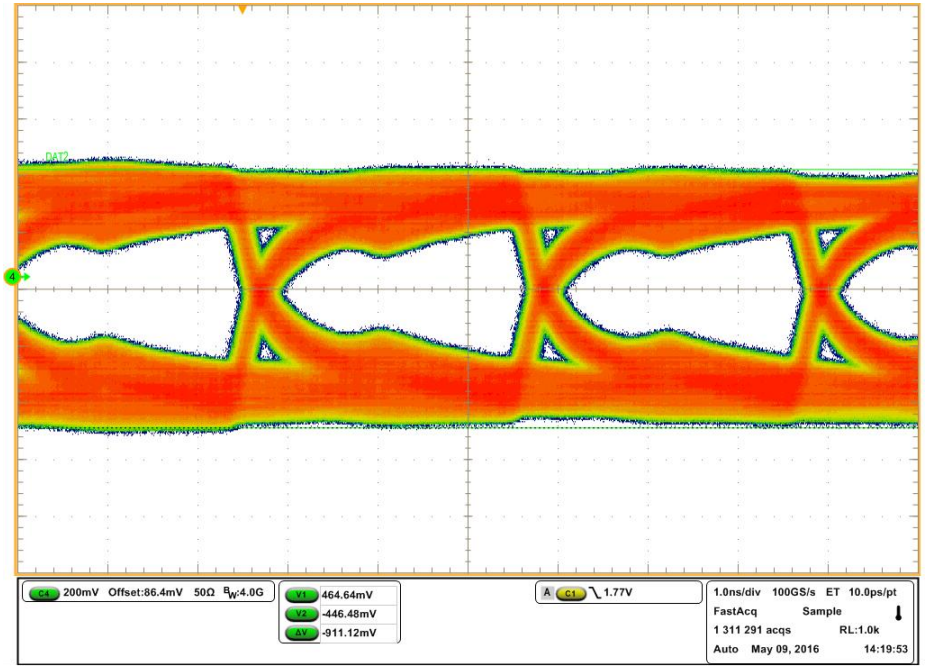
Eye Diagram @ SALT8b TB (I)



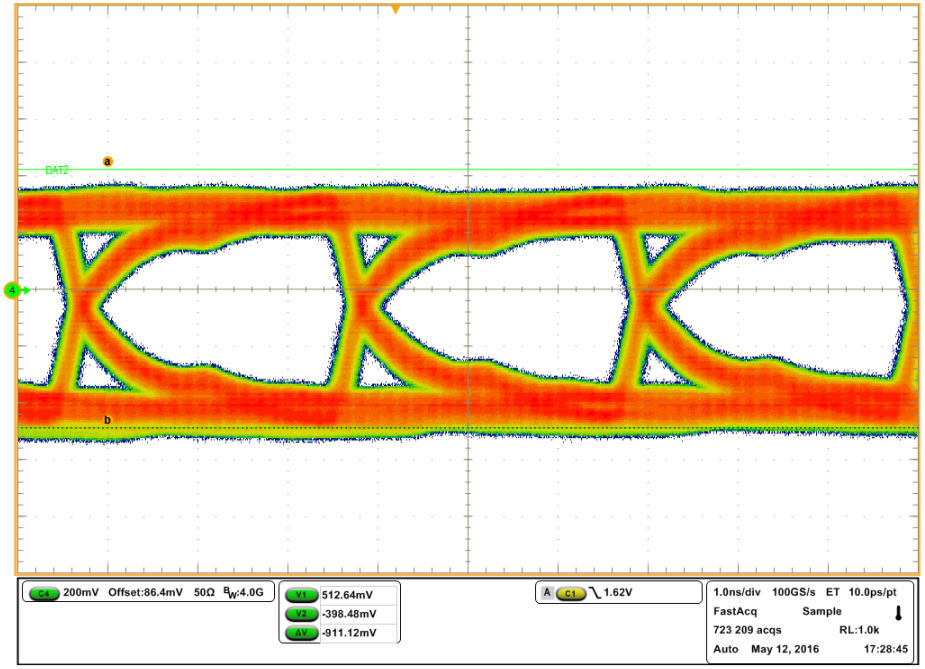
Eye Diagram At The End of Flex Cable

Plots taken by Nathan Jurik

Rev2 flex cable



Rev1 flex cable



Rev2 seems worse than rev1, maybe due to the impedance issue in the new Flex cable.

Summary

- We have staged slice test plans to validate the read out chain and optimize individual components.
- The system setup depends strongly on the available components.
- We plan to study the noise performance, bit error rate, eye diagrams to provide quantitative & qualitative measurements of the readout system.
- Phase I test that was aiming for this workshop is behind plan. We hope phase I & phase II tests can be ready for the electronics review on July 1st at Syracuse.