# UMD Interface Status Update

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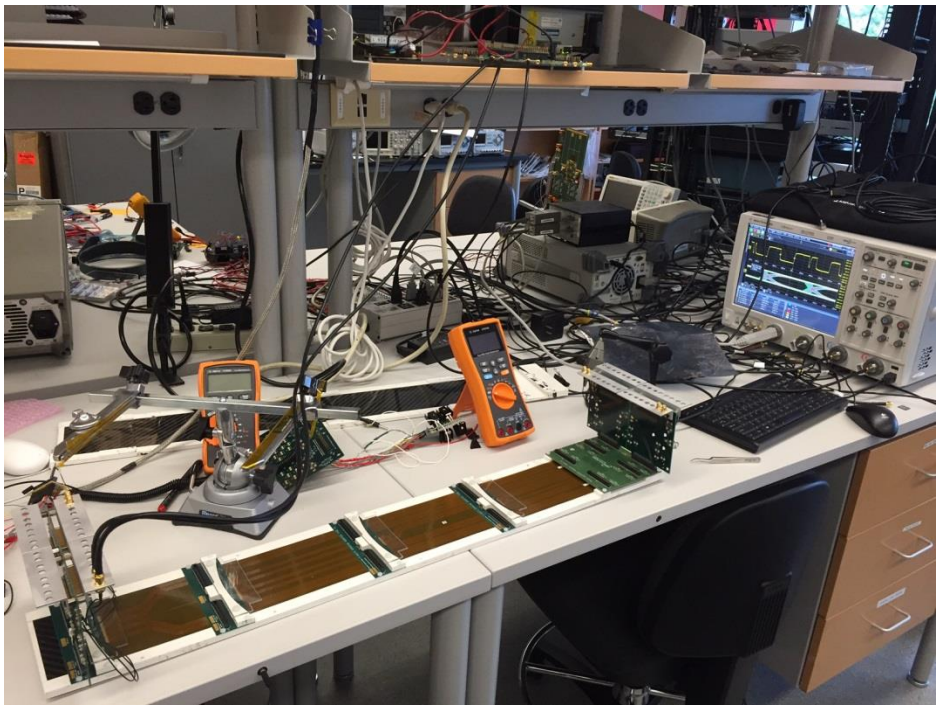
# Flex power lines

- 1.44 Amps on digital source line P1 West (longest run)
- 110 mΩ on source, 86 mΩ on return (117 mΩ spec)
- No working voltage sense pairs in longest two runs
- 12 working signal pairs in longest run (out of 48)
- Includes one e-link, but not TFC



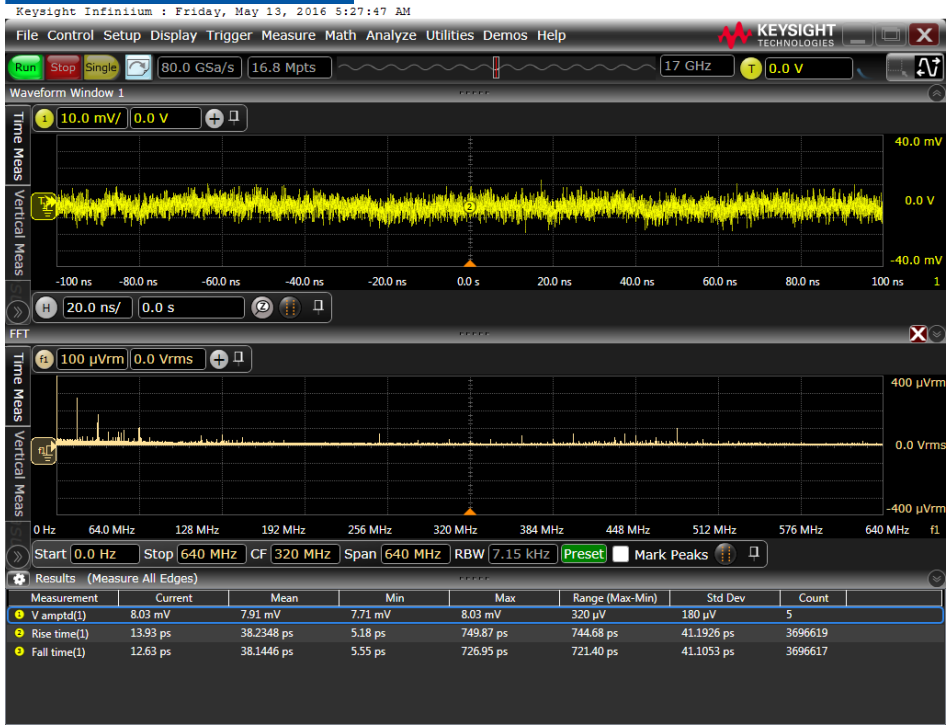
# Flex Cable: Gen 1 vs Gen 2

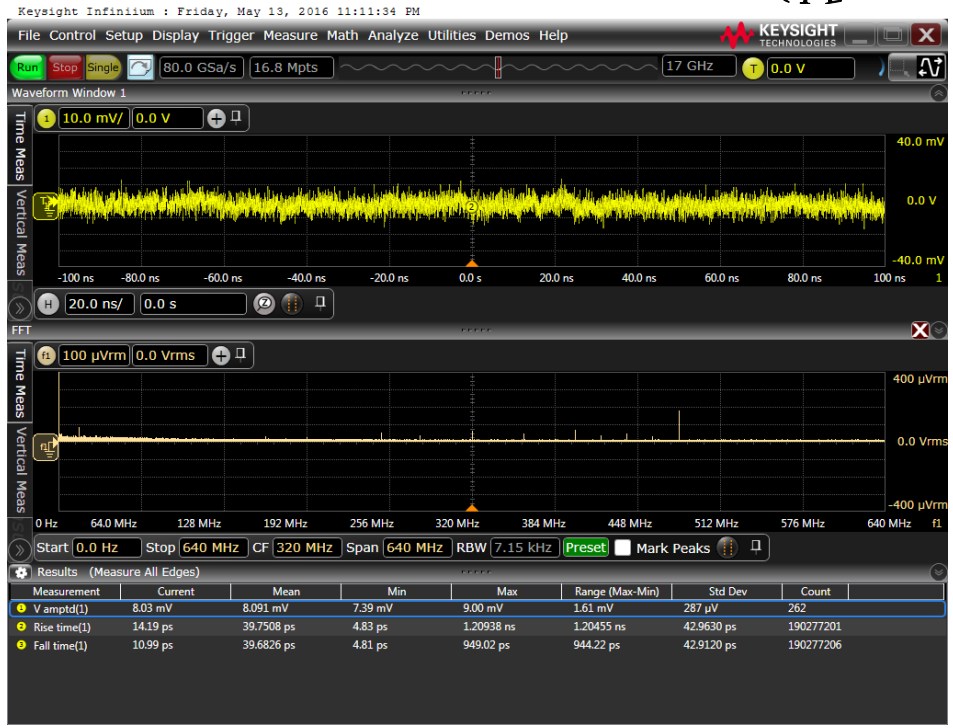

Serializer, Gen 1 Flex


Serializer, Gen 2 Flex

- Eye diagrams over longest flex run using serializer board to generate signal, passive probe board to receive and terminate
- 400mV, 320 Mb/s, fixed pattern
- Consistent performance between generations, 2nd very slightly better

# Crosstalk: Gen 1 vs Gen 2




Serializer, Gen 1 Flex

Serializer, Gen 2 Flex

- Very preliminary crosstalk test
- Single signal source (previous slide)
- Measure crosstalk in adjacent channel, terminated at both ends
- Improved in gen 2, minimal in either case
- Further tests needed

# Flex Cable: Serializer vs. SALT


Serializer, Gen 1 Flex


SALT8, Gen 1 Flex

- Still need to look at SALT8 through flex gen 2
- Plan to remove short-causing pin as per Nadim's instructions
- So far cable performance is very similar

# Flex test plans

- Broken TFC line limits test options
- Repeat measurements with SALT as signal source replacing serializer
  - Try different SLVS drive current, common mode
- Power SALT8 through flex cable, re-evaluate signal quality
- Validate SALT8 communication over gen2 flex cable
- Fill the Gen2 STAVE Flex cable with system mix of 40 MHz and 320 Mbps differential signals using 4 COMET boards

# COMET Status

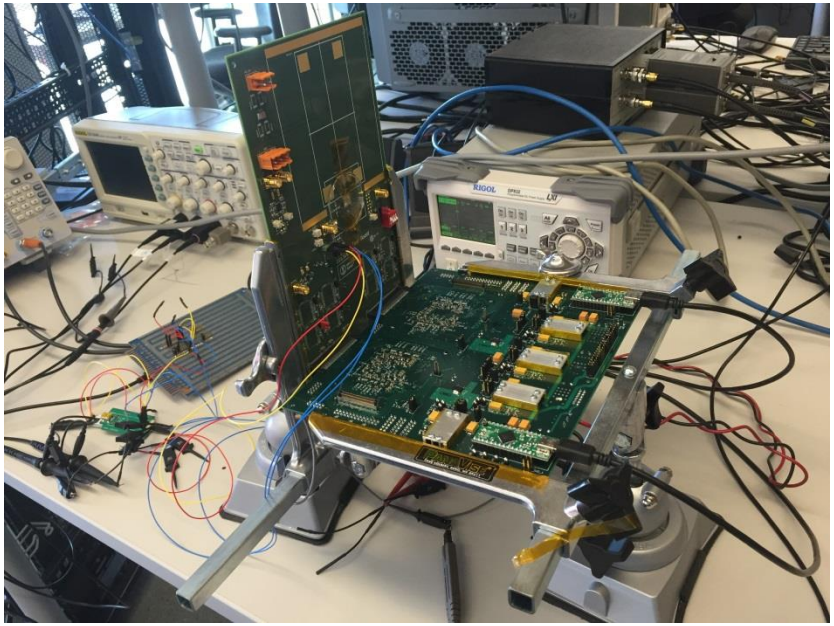
- 9 COMETs assembled and functioning – 3 fully reworked
  - One board for CERN here to demonstrate functionality
  - Will ship additional boards to Syracuse, Milano
- Features implemented:
  - USB interface
  - TFC
  - Single e-link
  - SALT8 communication
  - COMET-COMET communication
- **Gateware plan: send and interpret 3 e-links, then 5, then send 20**
  - Milano test plans? What stage is useful?

# COMET Operation

- Power: 5V
- Program FPGA: Microsemi FlashPro 4
- FPGA directly controlled via CSV files
  - nBytes (9 or 256)
  - Start header
  - Transfer type
  - Control/TFC/e-link data
  - Checksum (not functional)
  - Stop header
- Three functions for USB interface
  - FT_Open (USB module)
  - FT_Write (USB module, csv file)
  - FT_Read (USB module, read config csv file, nBytes)
- FTDI USB module requires Windows OS

```
9
10101010
00000001
00000010
00000000
11111111
00000000
11111111
00000000
01010101
```

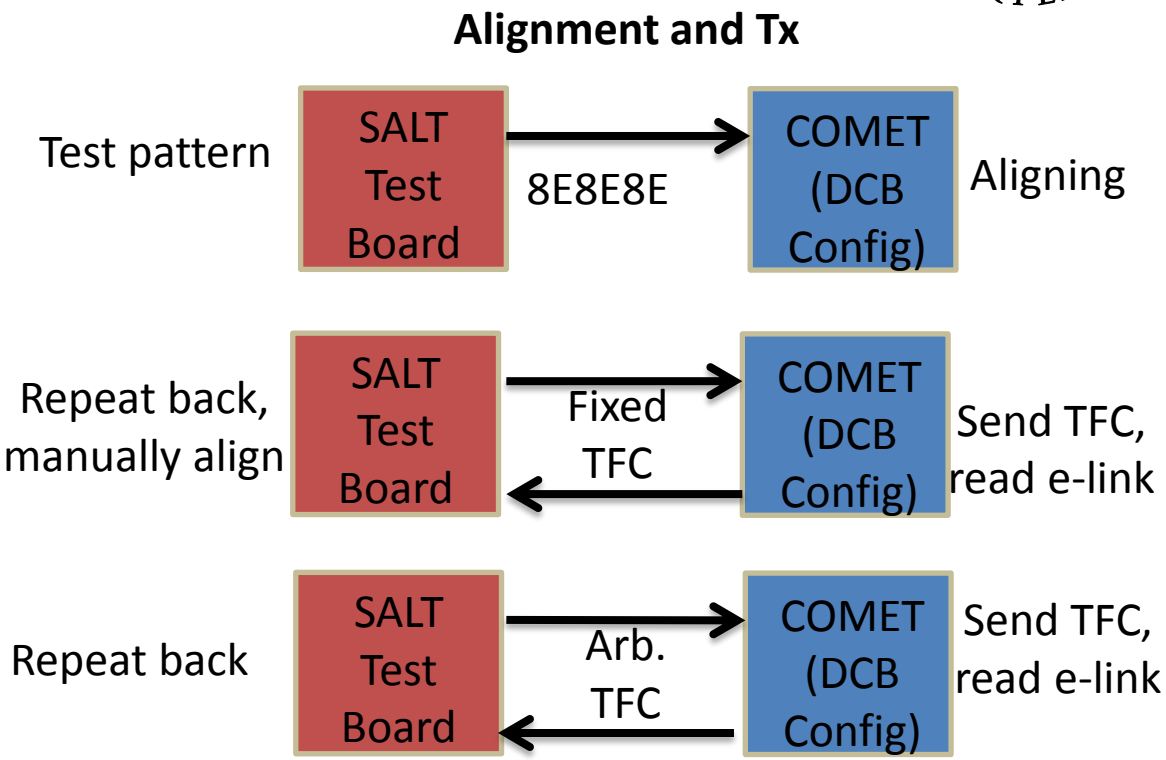
# COMET Operation

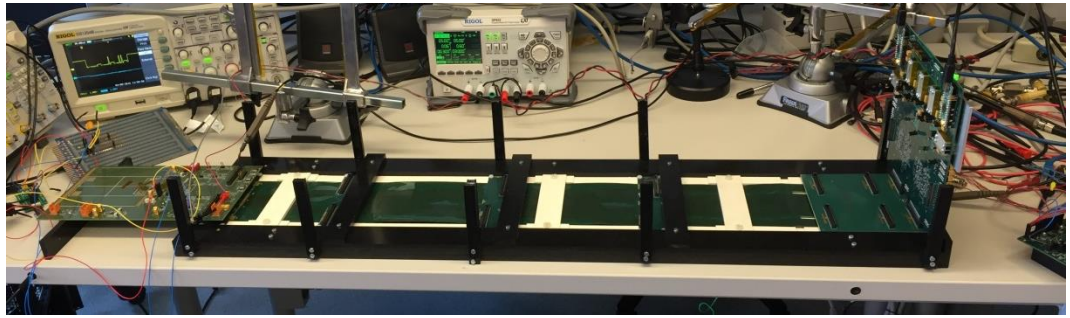


- Prepared BAT files:
- n01_Align_COMET.bat
  - Open FTDI module
  - Start alignment
  - Stop alignment
- n02_TxRx_COMET.bat
  - Open FTDI module
  - Fill TFC registers from PC
  - Write out TFC registers (repeatedly)
  - Read out e-link (once)
  - Write e-link registers to PC
  - Optional: Check registers for ascending sequence

# COMET-SALT Communication

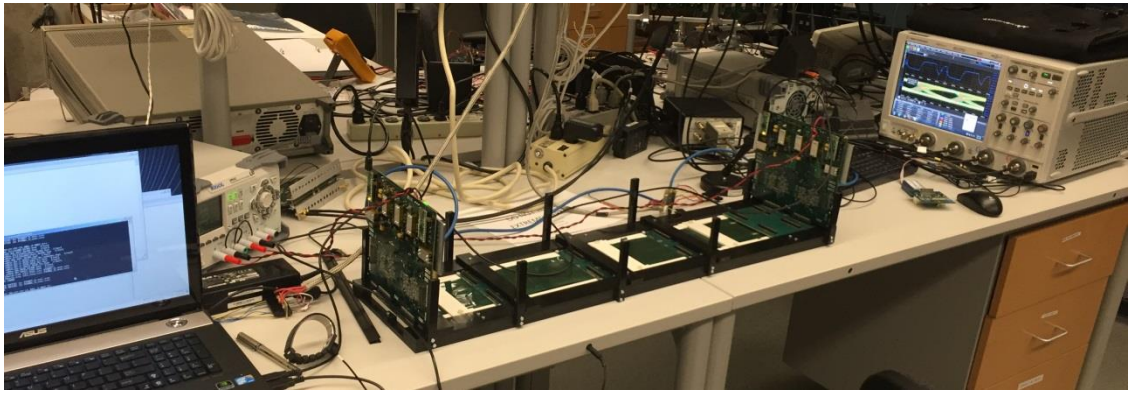
- Set SALT8 to repeat test register 8E
- Run n01_Align_COMET.bat
- Set SALT8 to repeat TFC register
- Send fixed pattern w/ n02_TxRx_COMET.bat
- Adjust SALT8 register (0,2) to align to TFC
- Can now send and receive arbitrary sequences

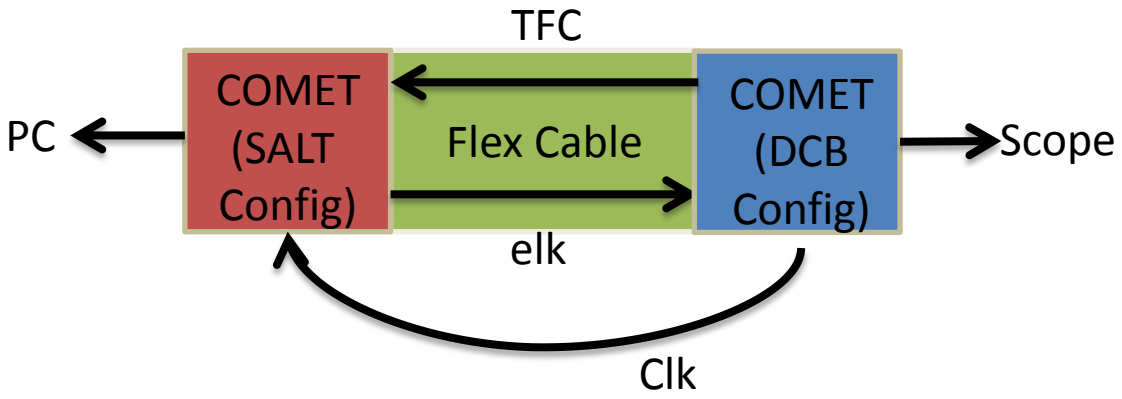


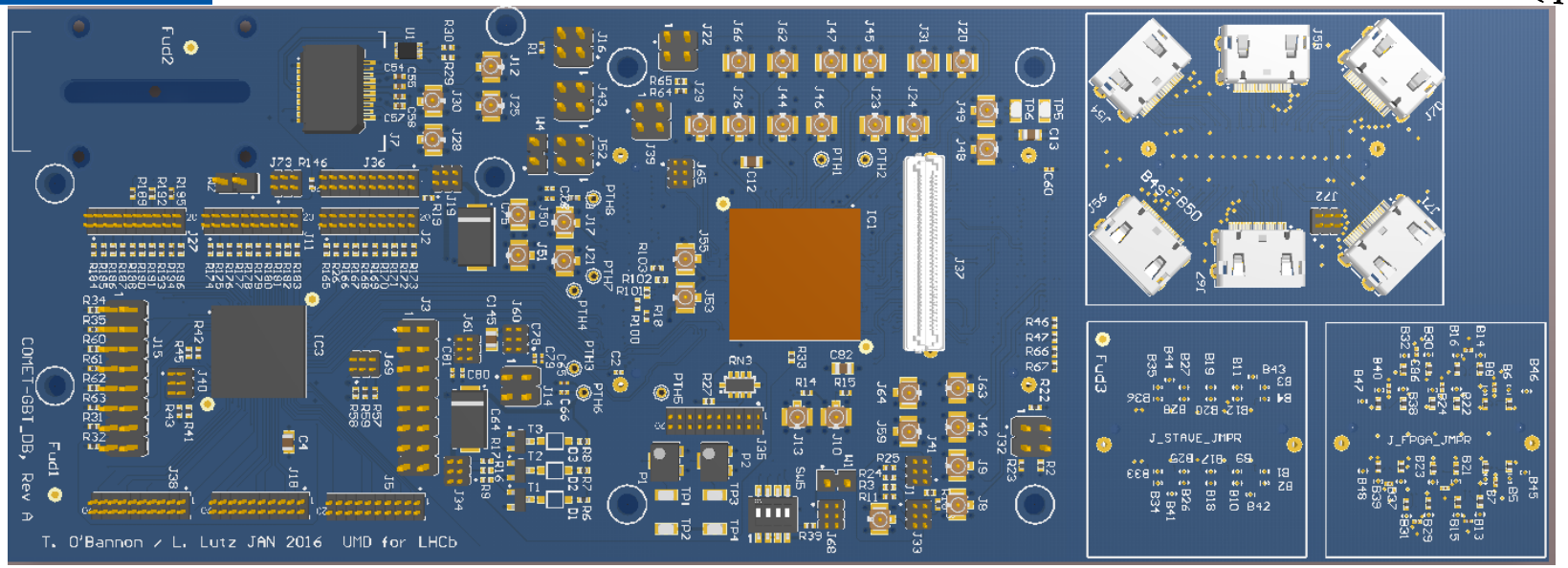
# COMET-COMET Communication

- Bug in COMET-COMET communication fixed
- Clocks power up in deterministic phase
- No bit errors observed at the level of 1 in 10^7
- Work ongoing to instantiate additional e-links
  - FPGA more restricted than expected
- Operation: As above, but requires both COMETs to send and align to 8E test pattern simultaneously





# COMET GBT DB (DCB SubCircuit prototype)




- Power provided from COMET regulators (plugs in replacing passive DB)
- Set registers via CERN I2C dongle (wire harness needed)
- Each board incorporates 1 GBTx, 1 GBT-SCA
- SFP+ connector accommodates VTTx/VTRx or commercial equivalent
  - Requires different polarity and pull-up voltage configured by jumpers
- Separate jumper boards connect GBTx inputs to STAVE e-links, FPGA output pins
- Additional jumper board for HDMI connectors
- Additional configuration via U.FL cables
- Clock/TFC lines, refclk i/o, test outputs, etc.

# GBT DB Status

- COMET GBT DB assembly in progress
- 2 boards with GBTx oscillator (1 UMD, 1 Syracuse), 1 without (UMD)
- Have components for 2 more (limiting component GBT-SCA)
- Expected delivery date: June 3rd
- I2C configuration developed through CERN GBTx webpage
  - XOSC, Widebus, automatic phase aligner tracking (initially)
- Plan: immediately begin verifying functionality, then send to Syracuse for slice test
  - Initial test:
    - Power on, write/read I2C registers
    - Set test clock output to reference clock
      - **Register 319[4:0] =0, Register 283[6:0] =1**
    - Check refclk0 on flex cable

# GBTx loopback test

- Connect GBTx_1 rfclk out to GBTx_2 rfclk in
- Connect GBTx_1 Tx to GBTx_2 Rx
  - Directly via U.FL cables
  - Incorporate copper SFP+ connector
  - Incorporate VTRx/SFP+ and optical fibers
- Write data to GBTx_1 elk from COMET FPGA
- Read data out from GBTx_2
  - via COMET FPGA (requires moving pins in COMET gateware)
  - via Tx to logic analyzer (more difficult to validate output, requires internal loopback in GBTx_2)

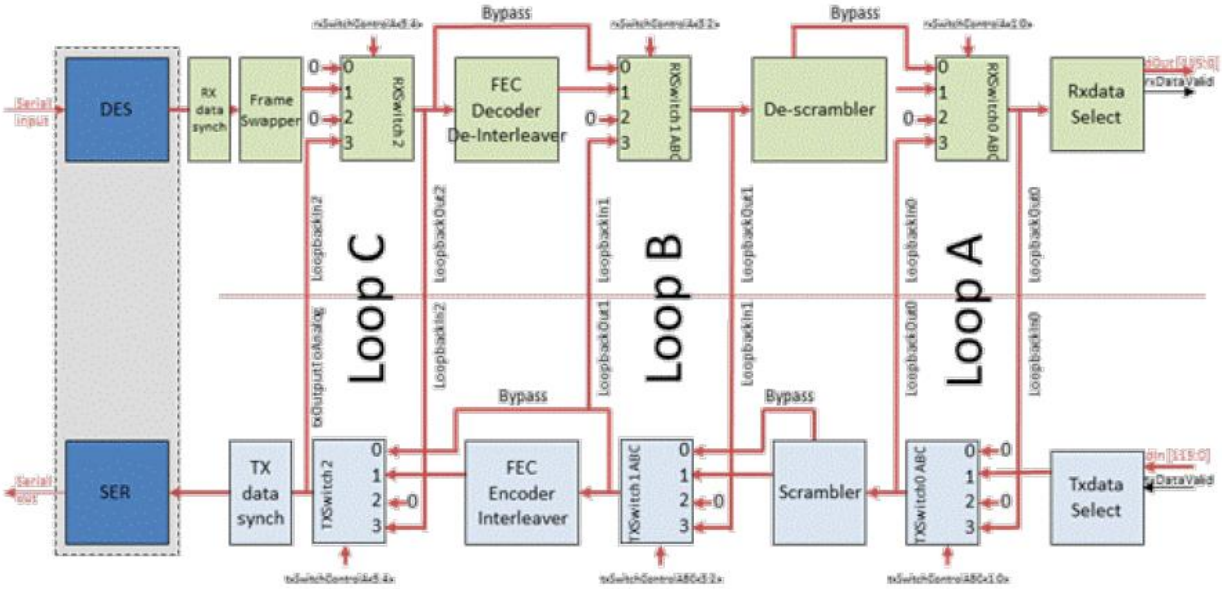



Figure 17 GBTX data path block diagram

- **Any additional validation before sending board to Syracuse?**
- Next steps:
  - Interface with SALT8
  - Program I2C from COMET

# DCB EDR Objectives

- Evaluate SALT communication via STAVE Flex cable interconnections
  - SALT8 using COMET configured with the Passive DB for 3 e-links, 1 TFC, and 1 ref clock
  - Implemented except for 2 e-links, need working signal lines to evaluate in gen 2 flex
- Evaluate STAVE Flex cable interconnections with full capacity signal environment
  - Fill the Gen2 STAVE Flex cable with system mix of 40 MHz and 320 Mbps differential signals using 4 COMET boards
  - Specifically evaluate the effects of crosstalk and i2C interface margins
- Complete PCB layout study for backplane, DCB, and master-control boards designs
  - Complete design trade of crosstalk versus differential pair spacing within planned PCB stackups
  - Validate crosstalk performance with test PCB
- Complete the COMET GBT daughter board design, layout, and build.
  - Assembly in progress, will start tests immediately with plans to complete all evaluations well before the DCB pre-production readiness review (~Nov 2016)