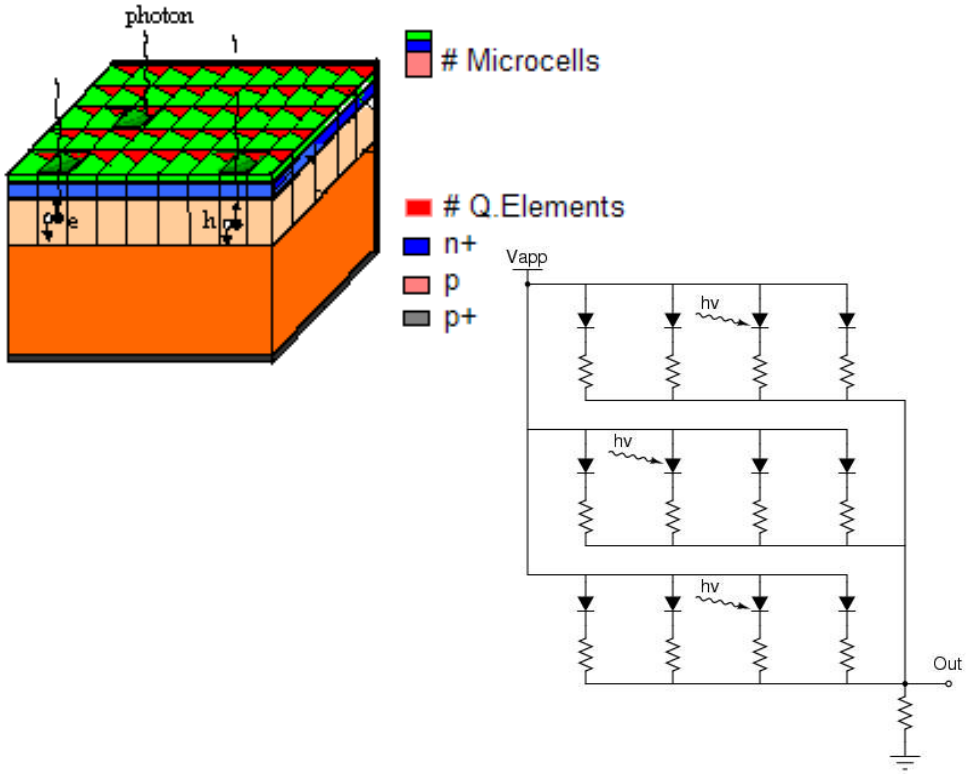
# Design and Test of Silicon Photomultiplier (SiPM) Structures in MPW CMOS Technology

N.D'Ascenzo
Huazhong University of Science and Technology
Wuhan, China

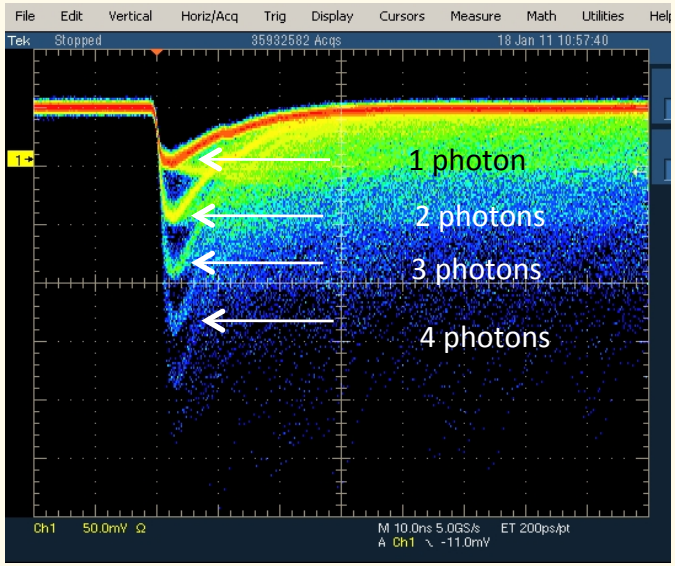
# Modern Silicon Photomultiplier Structure

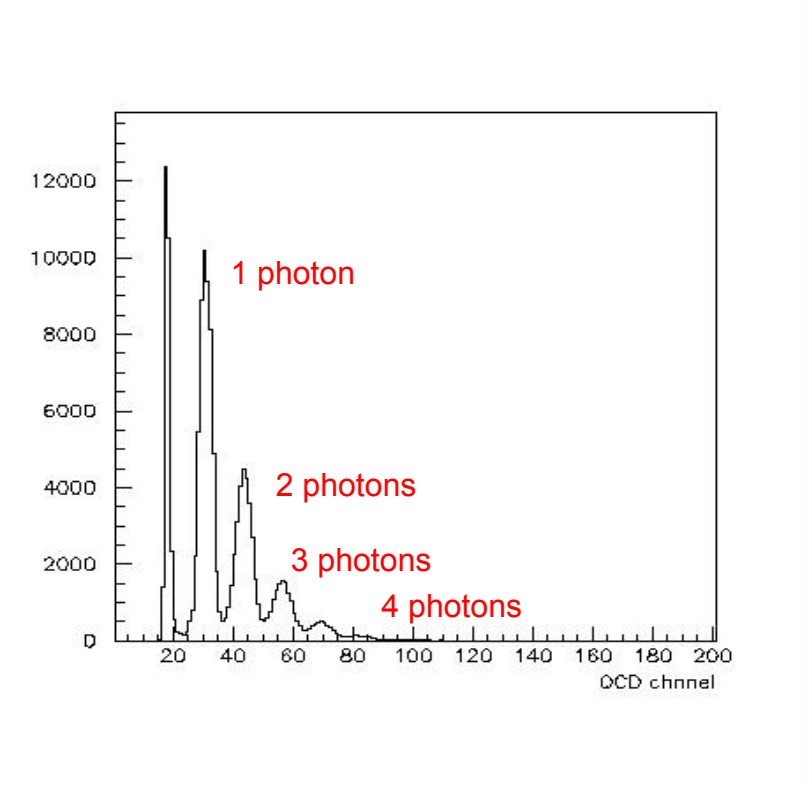



- Silicon Fine Micro Cells Structure (*p/n* junctions) on Common Substrate (few thousands)
- Breakdown Mode Operation of Micro Cells
- Integrated Quenching Elements for every Micro Cell
- Common Output
- Trenches for optic crosstalk suppression

- All microcells are independent and identical (give binary signals)
- Output is sum of the standard binary signals of microcells fired by photons

# Silicon Photomultiplier – Fundamental Limit Response

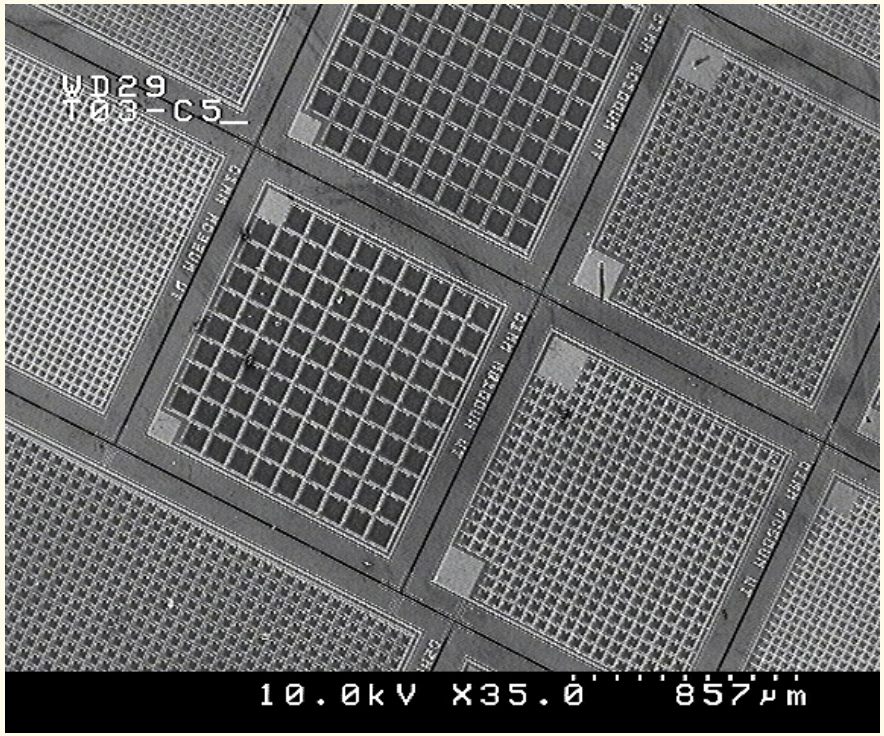


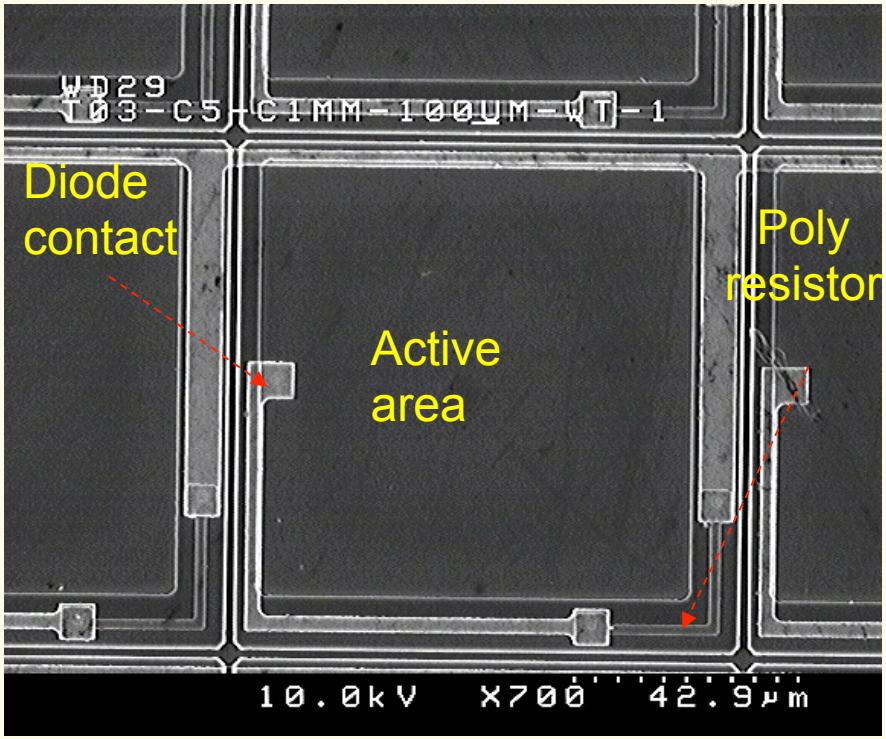




Theoretical Limit on Sensitivity - Single Photon Detection is the basic principle of operation with practically unlimited resolution

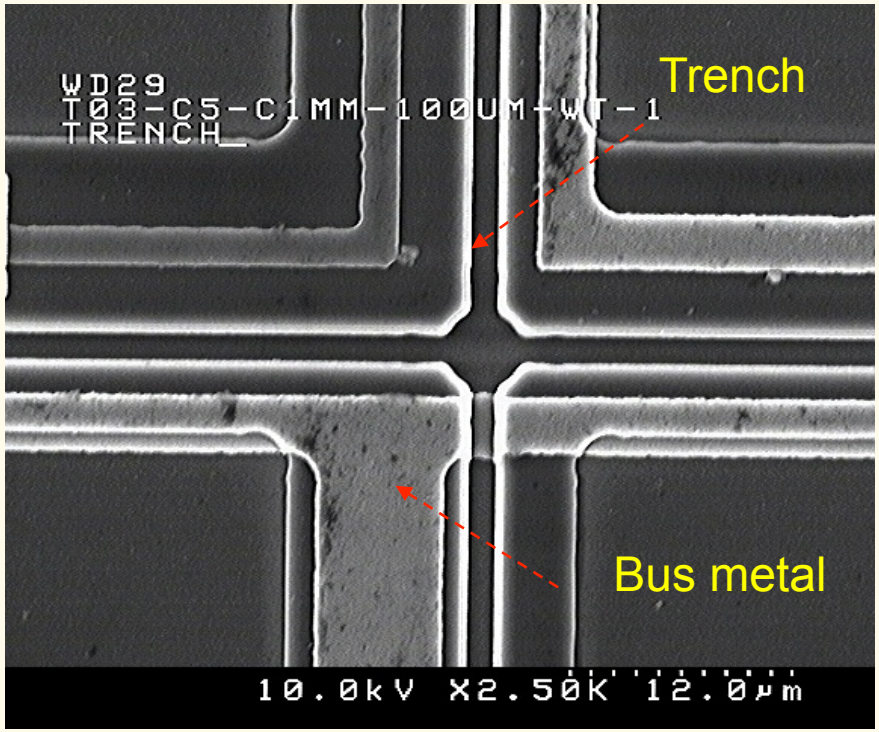
# Technology of SiPM Structures

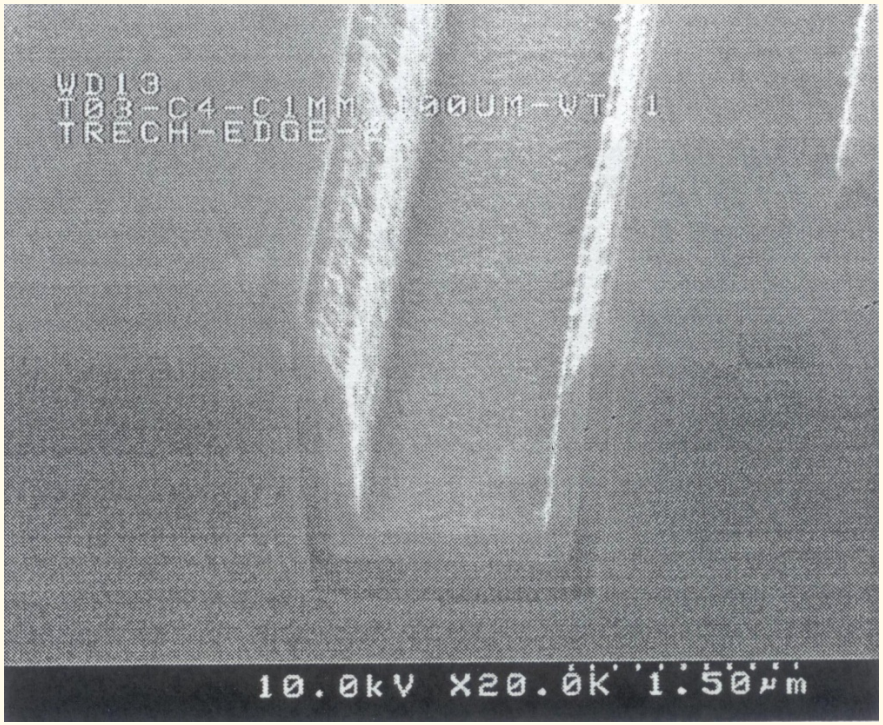
- General view of Silicon Photomultiplier
- Common Electrode Layout
- Microcells with Quenching Elements and Trenches



# Technology of SiPM Structures

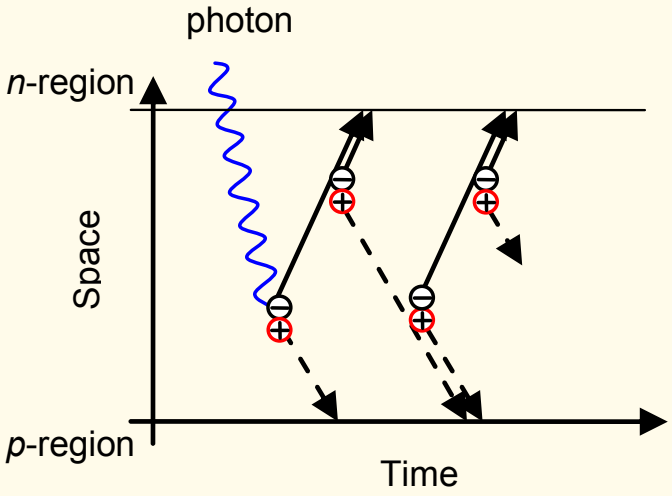



Trench Technology for preventing Optic Crosstalk

# Avalanche Breakdown pn-Junction

# Breakdown Mode Operation in Semiconductor

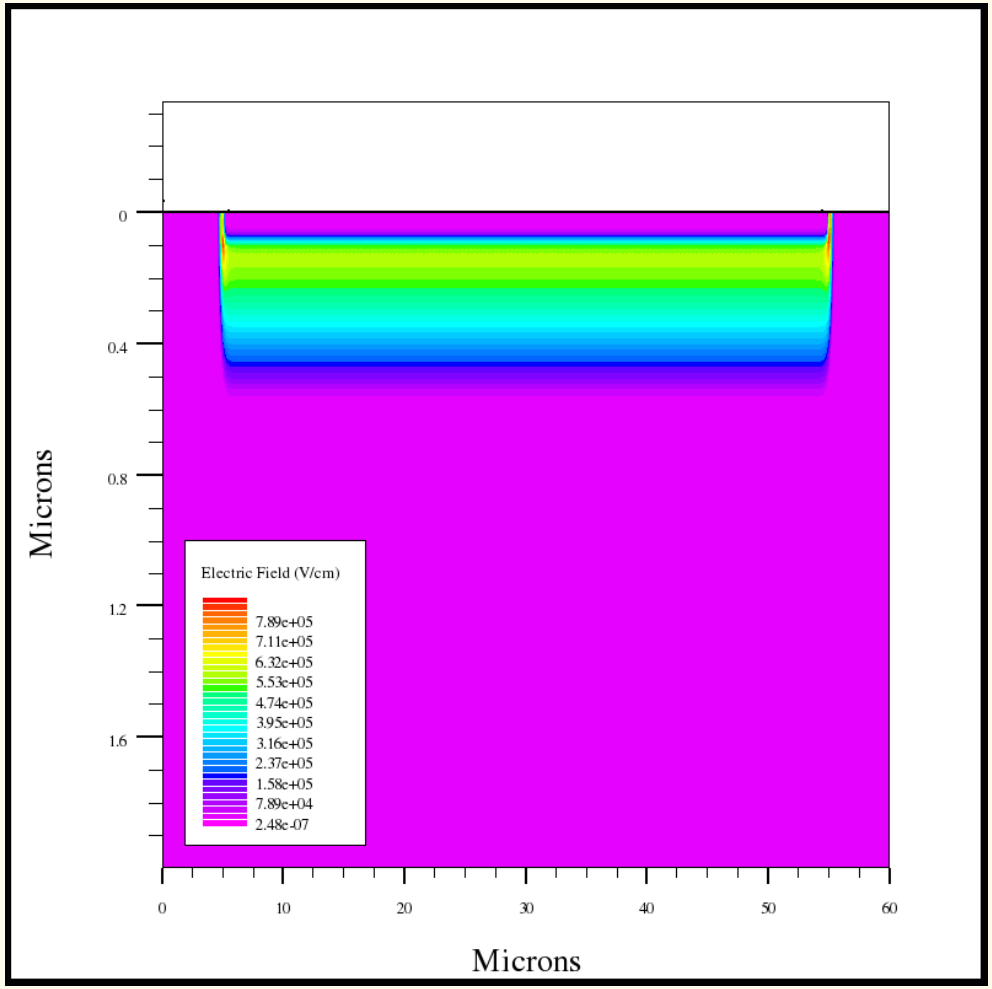



In the Avalanche Breakdown mode, the pn junction is biased above its breakdown voltage for operation;

- Electrons and holes are accelerated in the extremely High Electric Field and reach the condition of the "~ equivalent" secondary ionization for *e* and *h*;

The "Amplification Gain" is infinity, required quenching mechanism

# Avalanche Breakdown *pn*-junction in CMOS

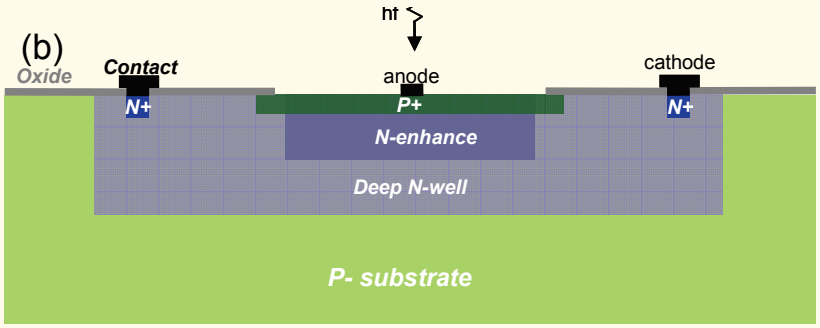


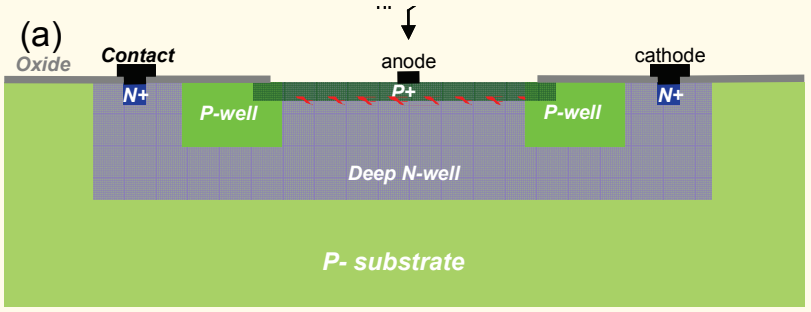

Standard CMOS pn-junction:

- The Electric Field is Not Uniform

Required the Special Design for Uniform of the Electric Field

# Avalanche Breakdown pn-junction Technology



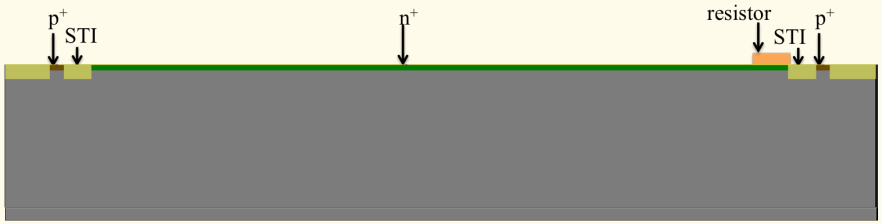



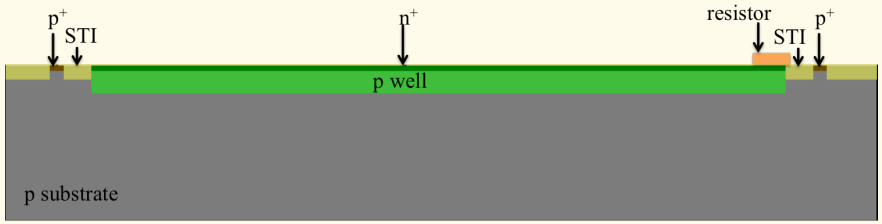

## Guard Ring

- Special Structures to avoid the Non Uniformity of the electric field

Unfortunately such Structures is not following the Standard CMOS Technology Rules

# CMOS Avalanche Breakdown pn-junction Technology



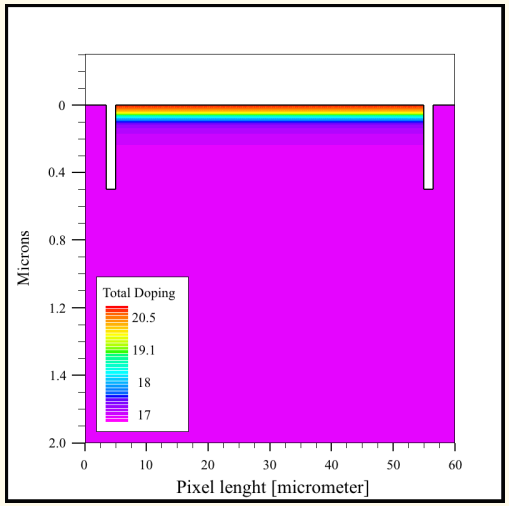



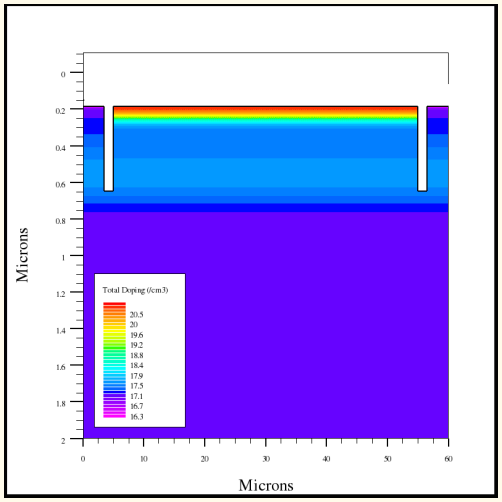

The Goal was Test of the Avalanche Breakdown *pn*-junction just use the MPW without violations of the CMOS rules.

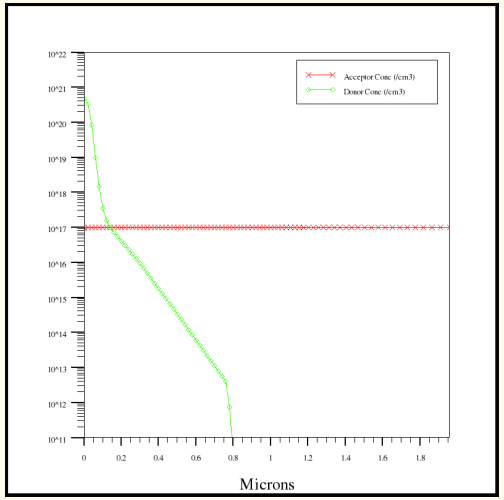
Guard Ring:

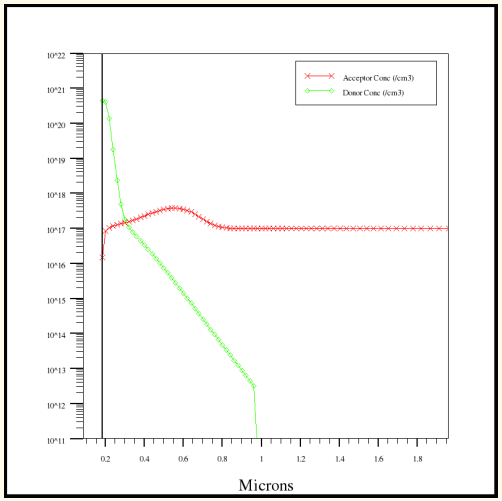
- CMOS Technology gives the possibility to realize only Guard Ring to use the STI (Shallow Trench Isolation) – even produce them by definition…

# CMOS Avalanche Breakdown *pn*-junction Technology



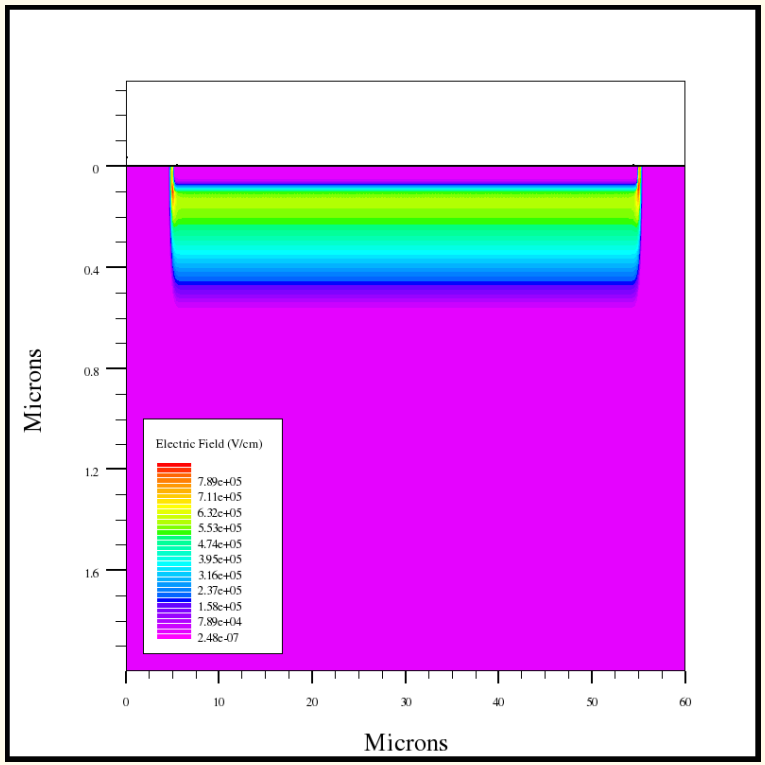



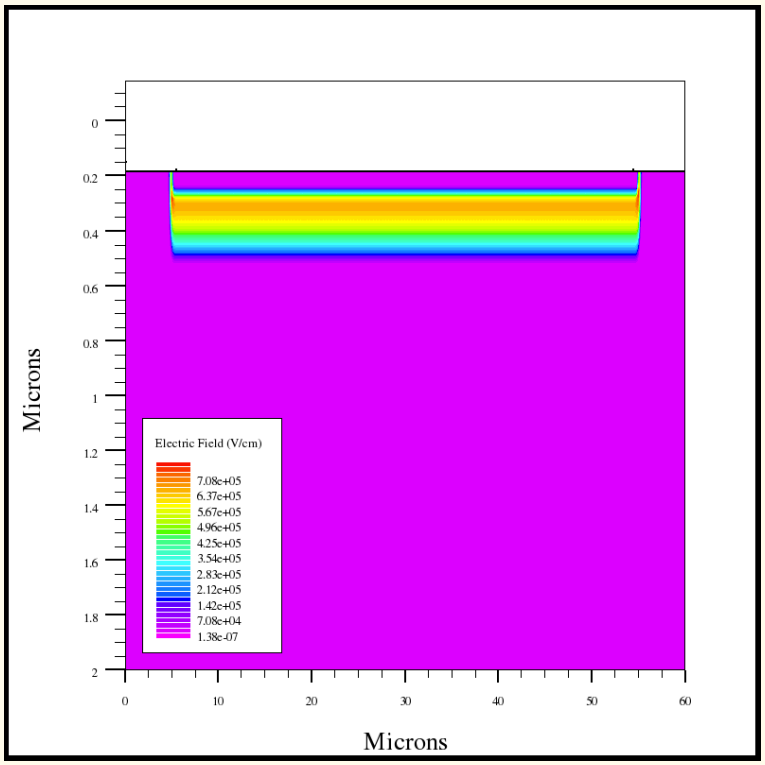




TCAD SILVACO Simulation – Concentrations: native *pn* junction and *p/nwell*

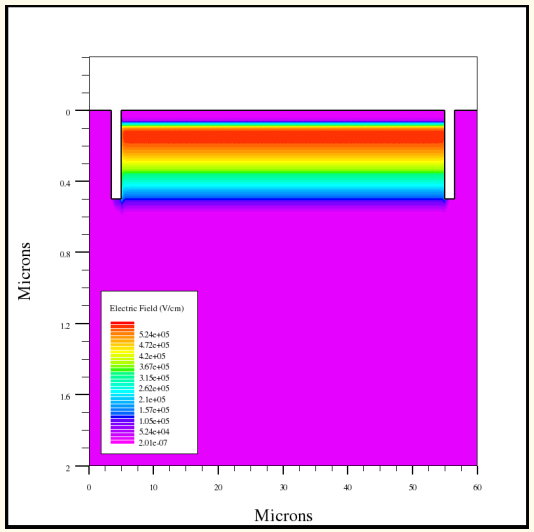
# CMOS Avalanche Breakdown pn-junction Technology

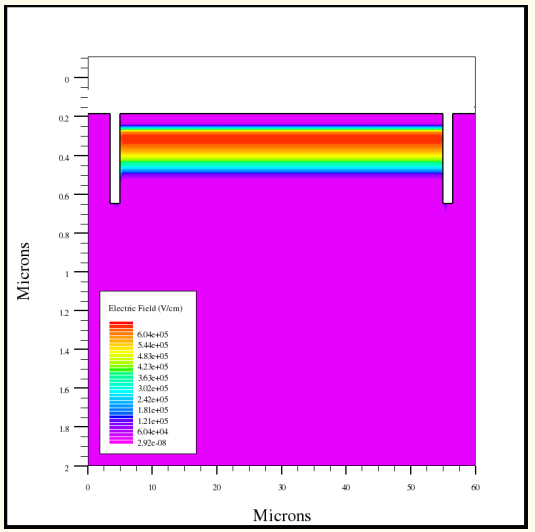


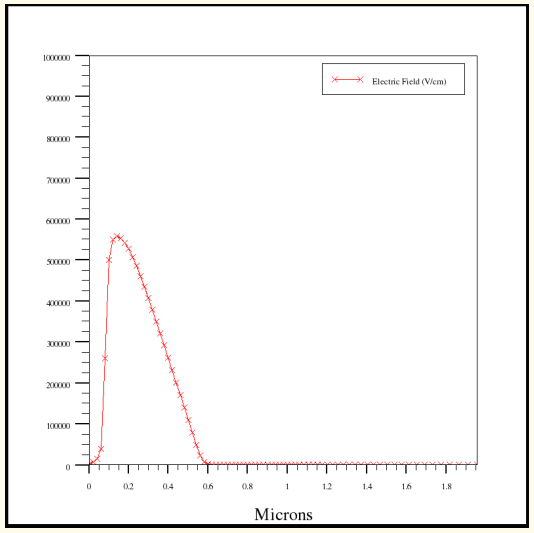



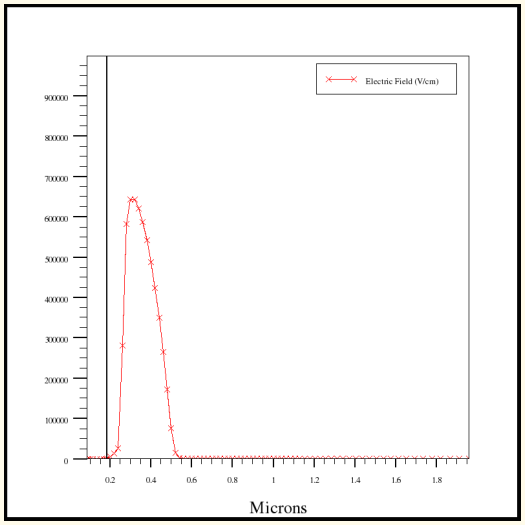

TCAD Silvaco Simulation gives some good results – Electric field with Initial Conditions for CMOS Processess

# CMOS Avalanche Breakdown pn-junction Technology



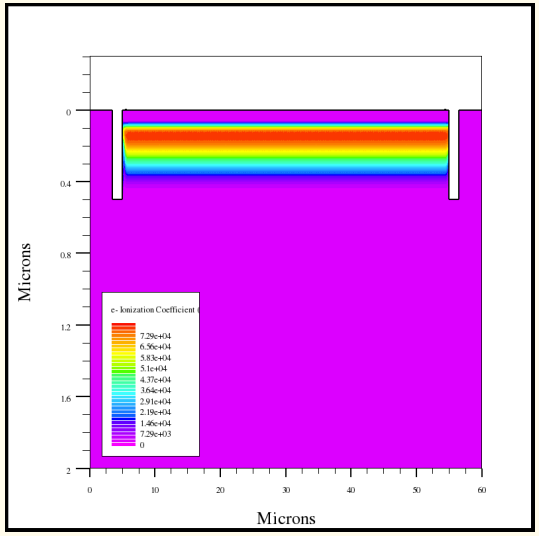



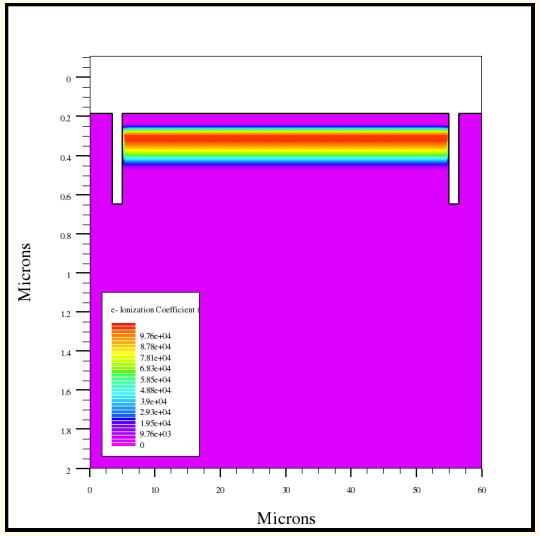



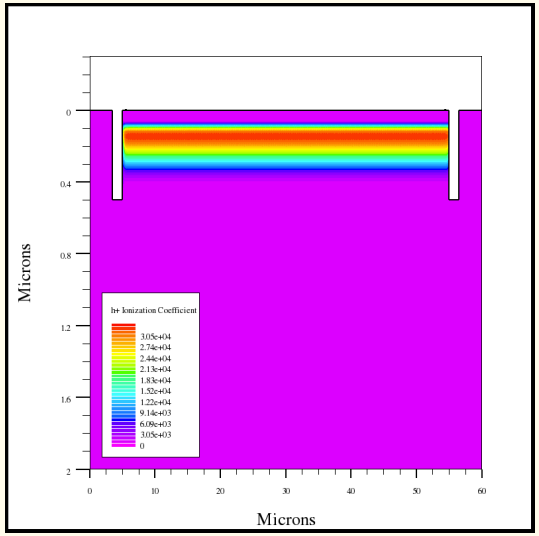



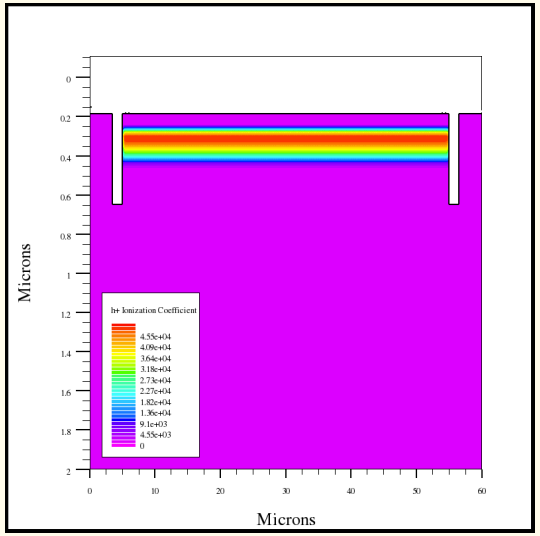

TCAD SILVACO Simulation: Electric Field with STI

# CMOS Avalanche Breakdown pn-junction Technology



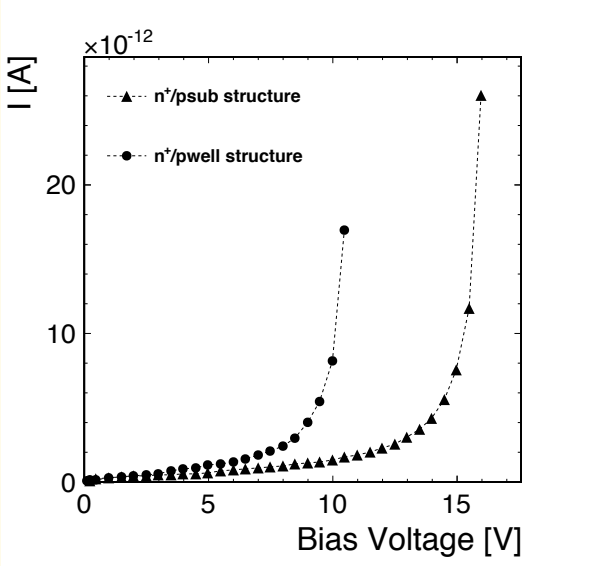



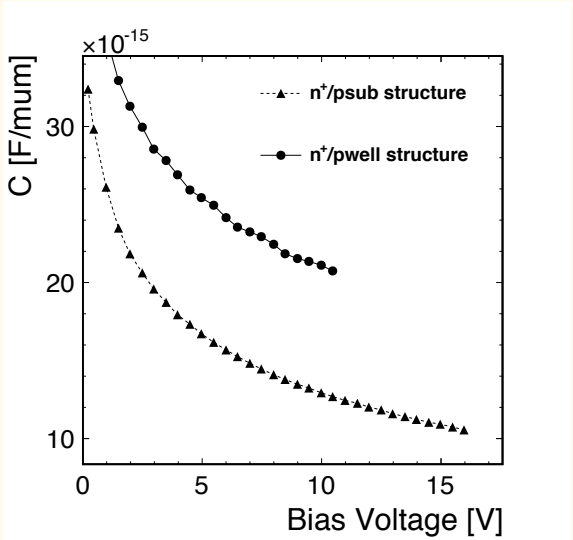



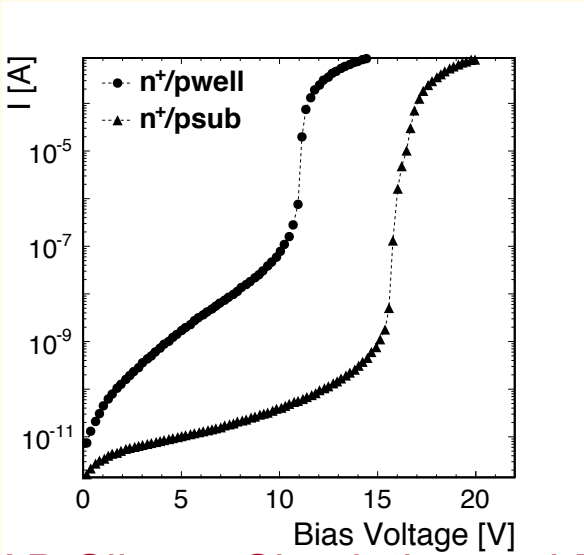



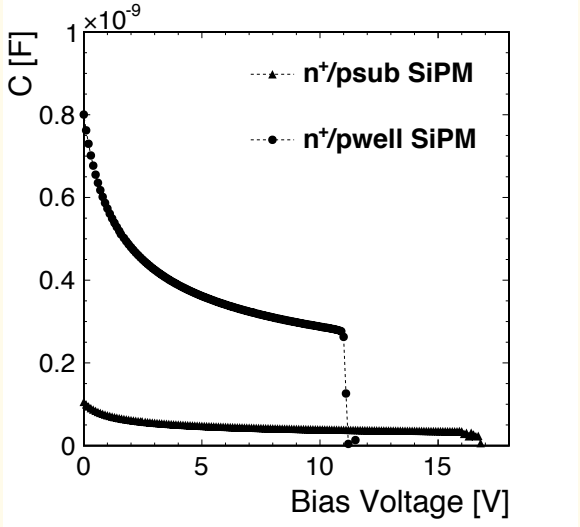

TCAD Silvaco Simulation – Ionisation Factor

# CMOS Avalanche Breakdown pn-junction Technology



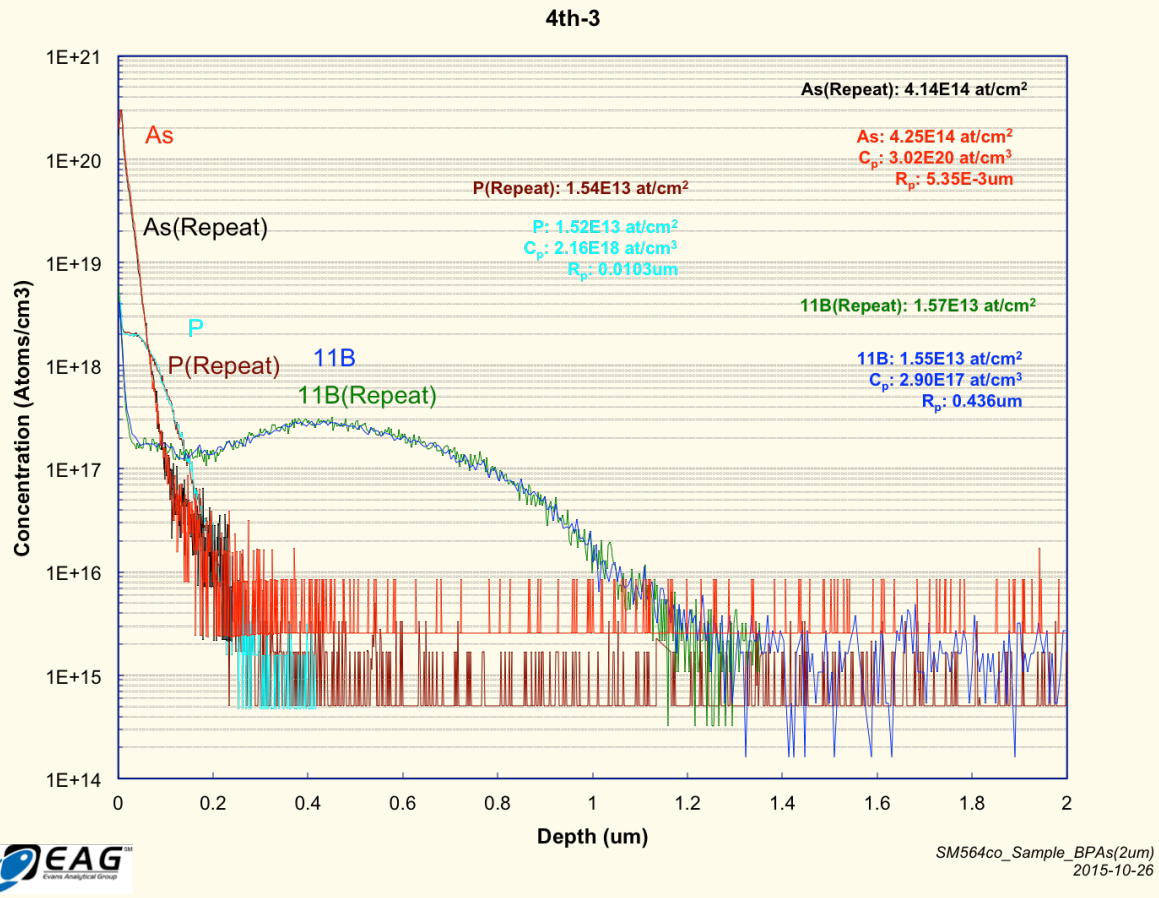




TCAD Silvaco Simulation and Experimental Results – Reverse IV and IC

# CMOS Avalanche Breakdown pn-junction Technology




TCAD Silvaco Simulation and Experimental Results – Reverse IV and IC

# Summary

- The Development and Design of Avalanche Breakdown Mode p/n Silicon Structures was performed on the basis of CMOS Multi Project Wafer (MPW).
- The results of the experimental tests show the good progress of the implementation of the SiPM in standard CMOS technology without modification of the standard technology processes
- The goal is implementation of the electronic components in the same technological stream