Update on fullbeam DAQ board on PET system

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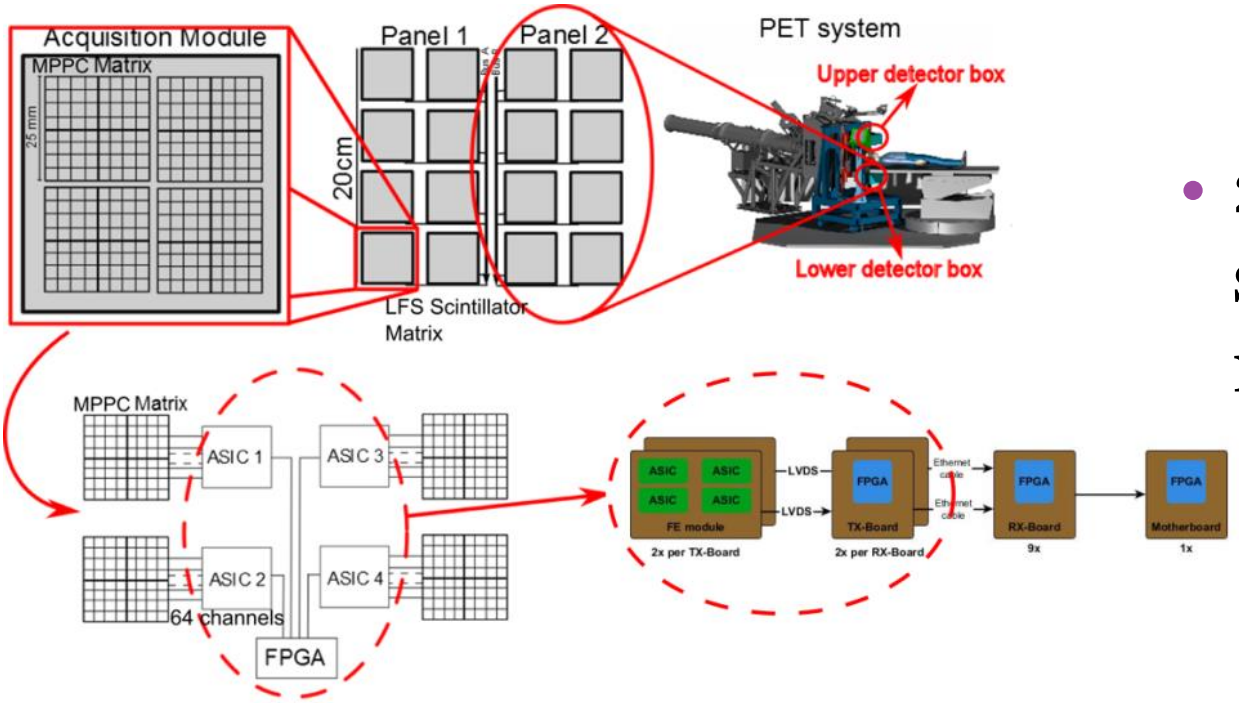
What is about?

- INSIDE project and PET prototype
  - INnovative Solutions for In-beam DosimEtry in hadron therapy

The INSIDE project is funded by the MIUR (Ministero dell'Istruzione, dell'Università e della Richerca) of the Italian government under the program PRIN 2010-2011 project nr. 2010P98A75.

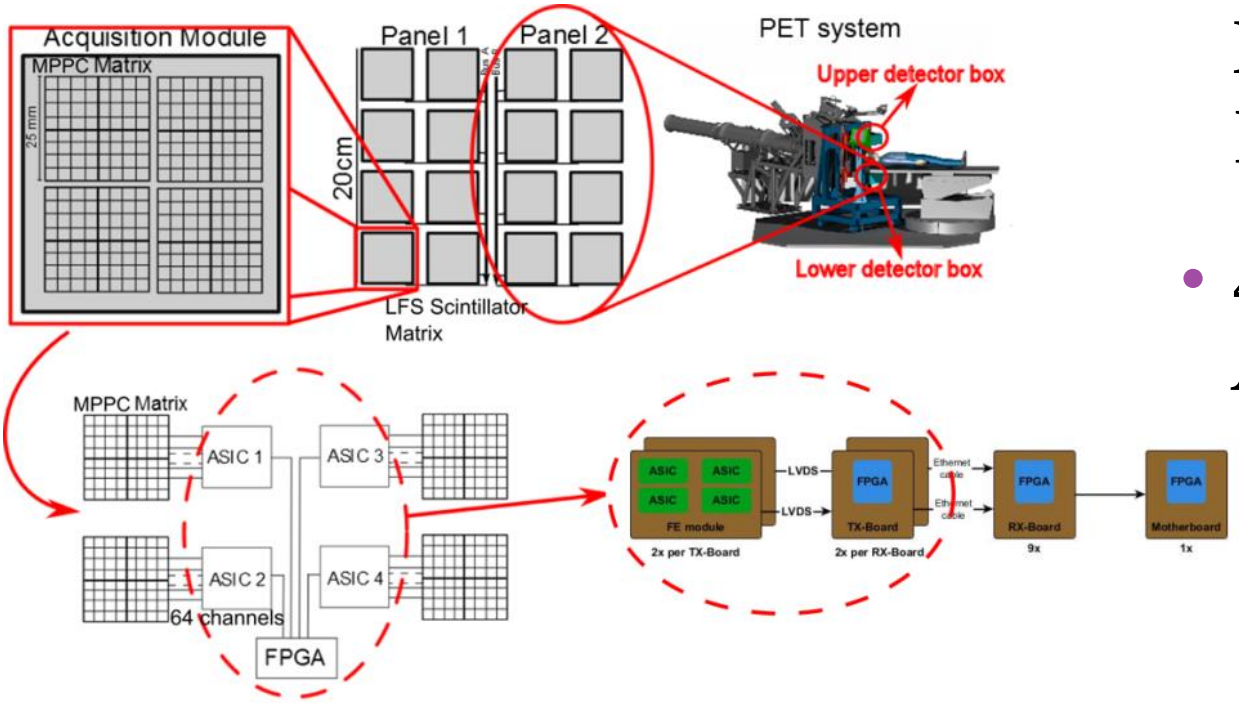
- Two Coincidence Sorter Architectures
- Software Development of a control system for HV/LV power supplies
  - Secondment at CAEN, Viareggio, Italy 10/2015-12/2015

PET Prototype(1/4)



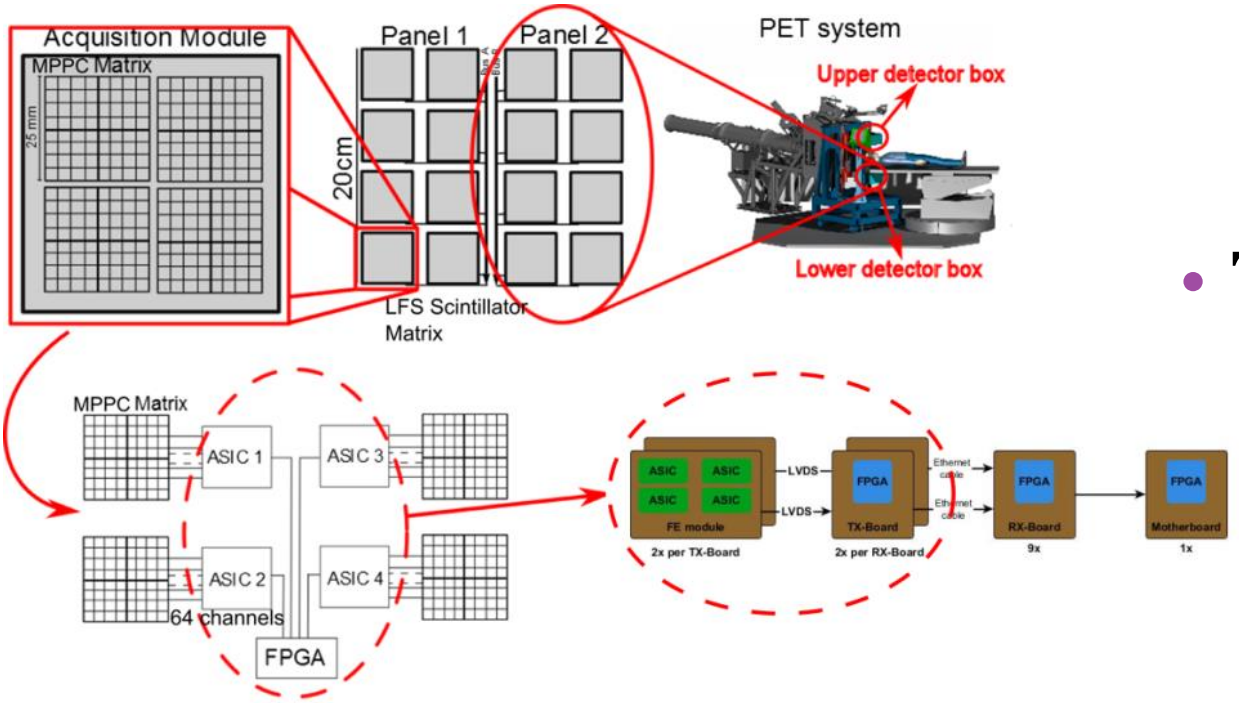
- 2 planar panels
  - 10cm x 20cm
- 2 x 4 pixelated LFS scintillator matrices
  - 5cm x 5cm
  - 3mm x 3mm x 20mm crystals

PET Prototype(2/4)



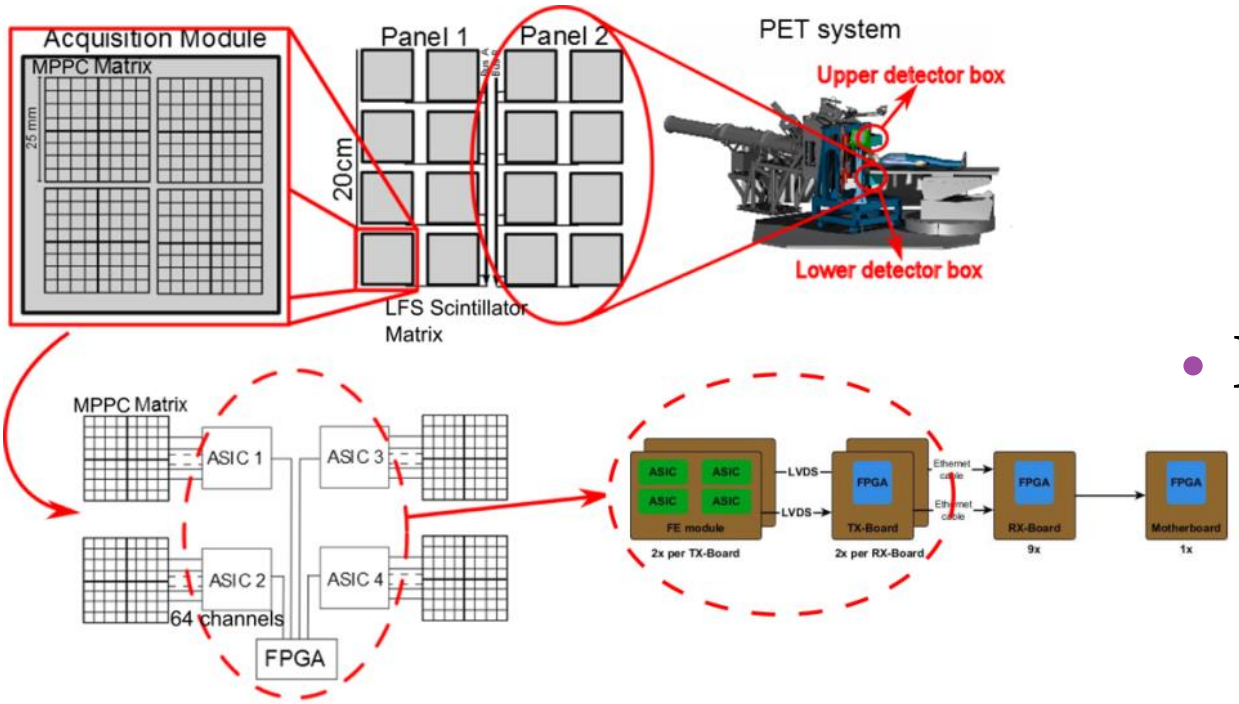
- 4 matrices of 8 x 8 MPPC from Hamamatsu
- 4 x 64-channel ASICs
  - On-chip multiplexing
  - TDC
  - 0.18um CMOS technology

PET Prototype(3/4)



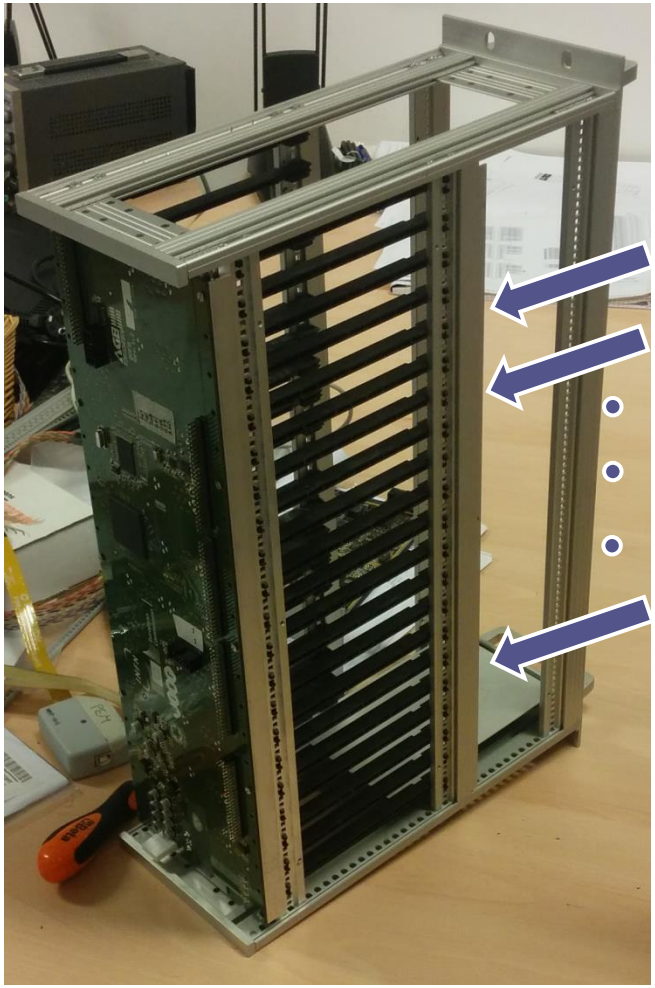
- FE Boards
  - 4 ASICs
  - FPGA
- TX Board
  - Small low-cost FPGA
  - Packet building

PET Prototype(4/4)



- RX Board
  - Fiber-optic receiver
  - Data concentrator
- Motherboard
  - Data acquisition board
  - Up to 9 RX-boards

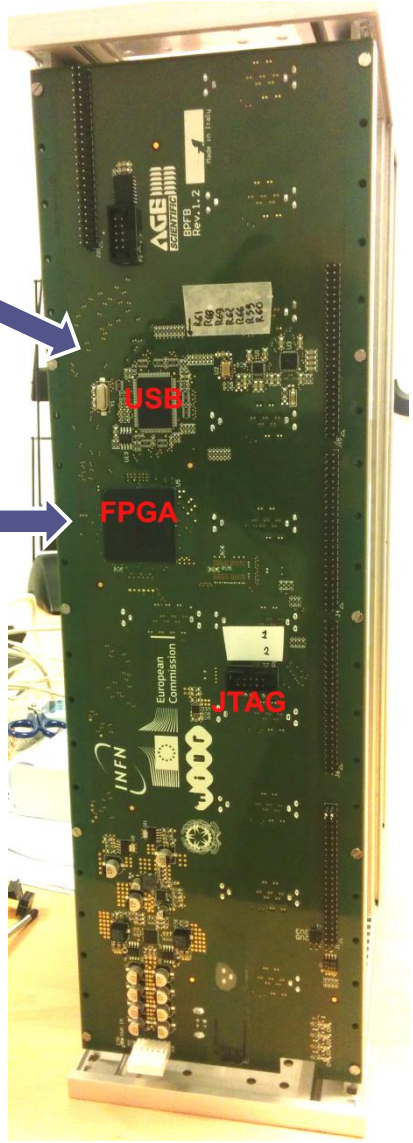
DAQ Motherboard



9 RX Boards

Cypress EZ-USB FX2LP (CY7C68013A)

Cyclone V



Data stream

- Encoded information about the detected photons

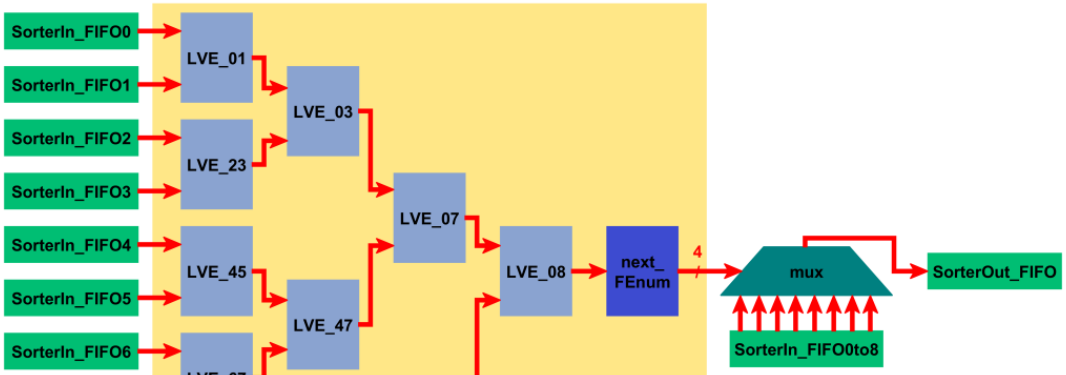
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
W0	F15	F14	F13	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	F0
W1	Detector ID						Crystal ID									
W2	E3	E2	E1	E0	Energy											
W3	Timestamp MSB															
W4	Timestamp LSB															
W5	Energy ID								Timestamp Fraction							

Coincidence Detection

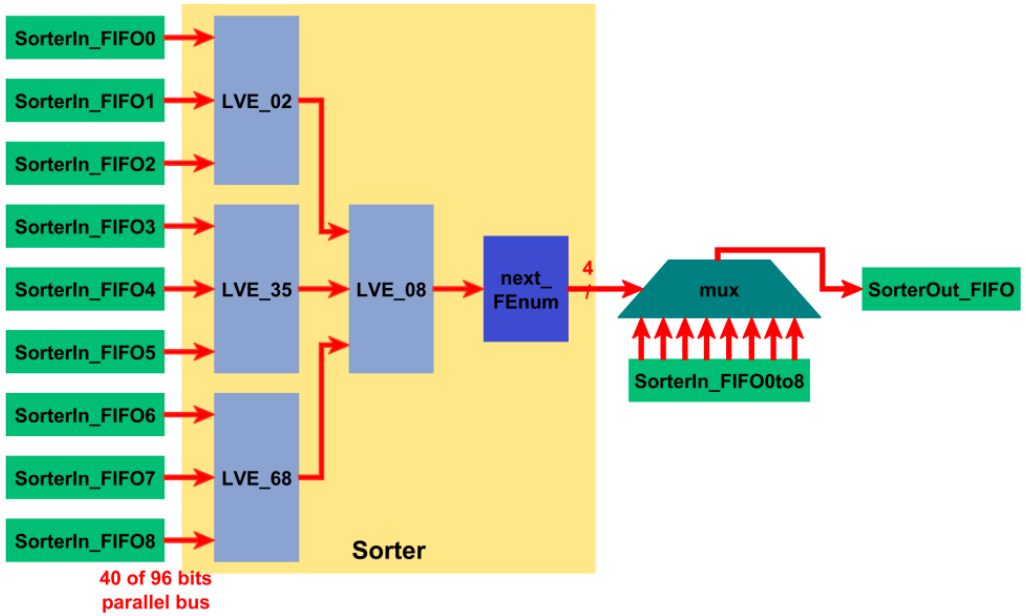
- Pairing of the detected single gammas
- The timestamp of the events must differ less than a Coincidence Window
- Necessary to merge and sort the events by timestamp → Development of Coincidence Sorter

Coincidence Sorter Architecture (1/3)

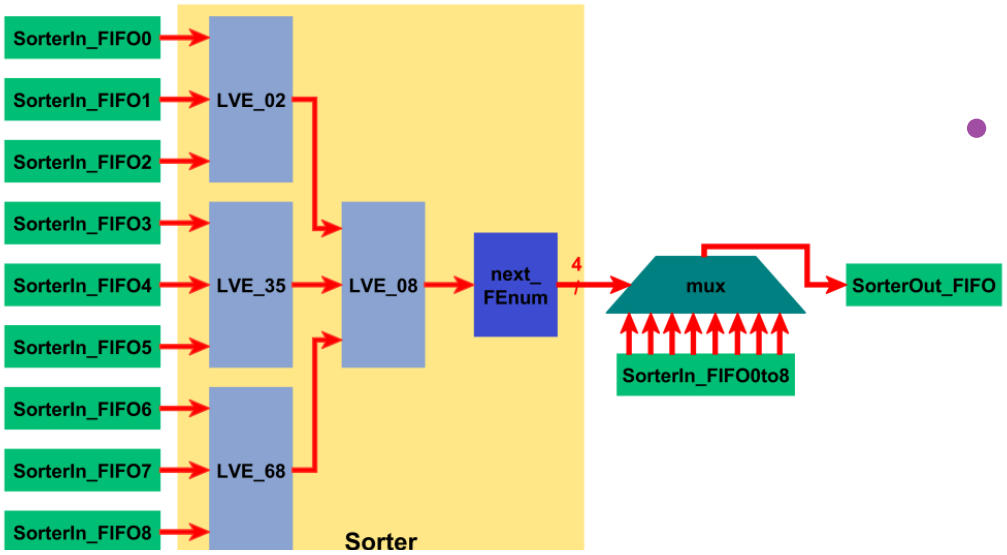
Architecture with
2-input comparators



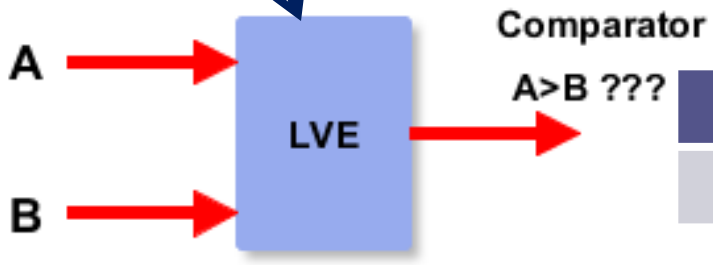
Architecture with
3-input comparators



Coincidence Sorter Architecture (2/3)

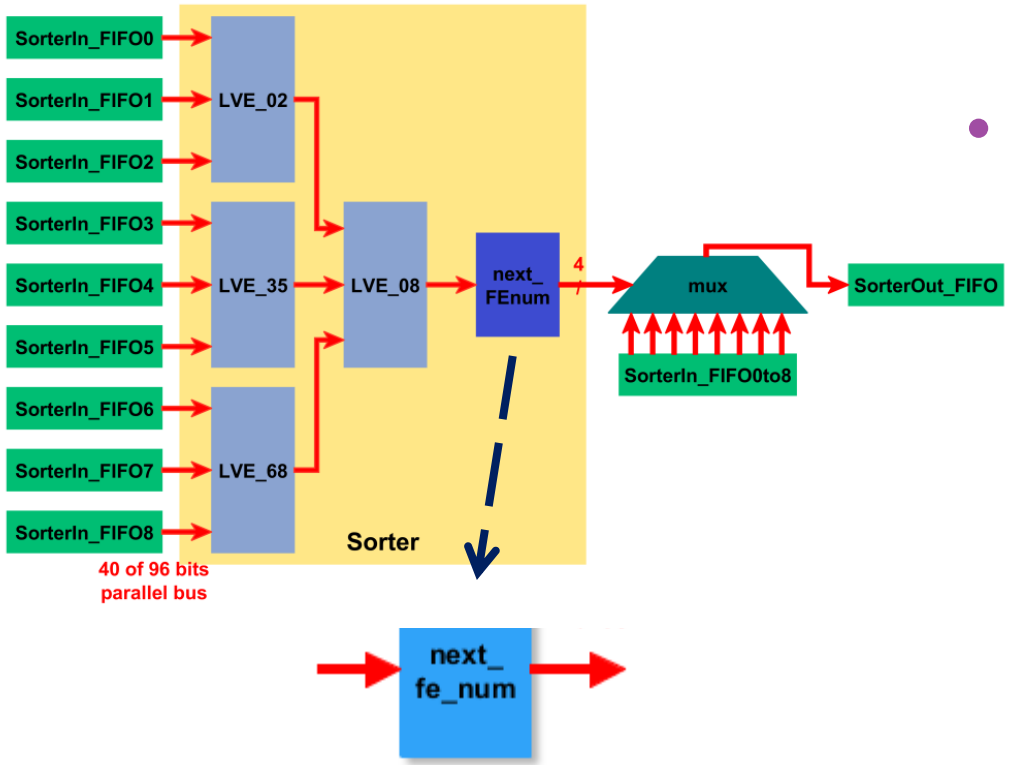


- LVE
  - Compares timestamps
  - Outputs the earliest timestamp
  - Outputs 5 additional bits



1 bit	4 bits	40 bits
Valid Data	FIFO number	Timestamp

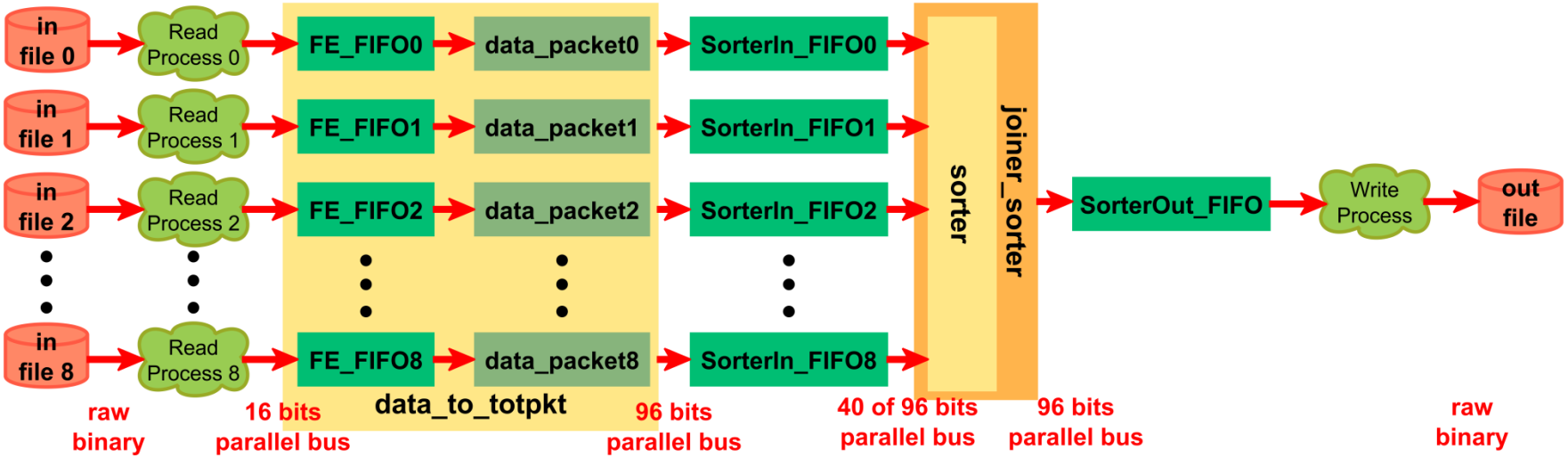
Coincidence Sorter Architecture (3/3)



- next_FEnum stage
  - Outputs the 4 bits
  - Restarts the process
  - Multiplexer
    - Recovers the data packet from the input FIFO

1 bit	4 bits	40 bits
Valid Data	FIFO number	Timestamp

Coincidence Sorter Testbench



- Simulation on ModelSim
  - Functionality verification → comparison of the simulation results with these from the python script
  - Goal of 20MHz minimum throughput rate
    - Achievement: → 28 MHz for 2-input-comparators Sorter
      → 40 MHz for 3-input comparators Sorter
    - The sorter can sort up to 40 million data packets per second.

CAEN
Tools for Discovery

Secondment at CAEN (10/2015 - 12/2015)

- Software development of a control system for HV/LV power supplies
  - Windows form application of the Microsoft Visual Studio 2010
  - HV Wrapper library provided by CAEN
- Implementation of ramp-up and ramp-down procedure and current/voltage monitoring for the HV power supply
- Current/voltage monitoring for the LV power supplies

Thank you!!!

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