Fig. 5: Scanning Electron Microscopy images (TOP view, 3D view, Zoomed View) of the 3D assembly including all metal levels of the BSI imager structure. (dashed line shows bonding interface)
AGENDA

• Leti brief overview

• CMOS Image sensor evolution with 3D technologies

• Current developments running at Leti
  ▪ Image sensor for visible light
  ▪ Image sensor for high energy particles

• Current 3D technology development at Leti

• Conclusion
LETI AT A GLANCE

- Bio medical platform
- Chemical & material platform
- Photonic platform
- Embedded systems
- Micro & Nanoelectronic platform
- Nanocharacterisation platform
IMAGING @ LETI – A GLOBAL OFFER

→ From material to system
→ From photon to decision

Component

Detection materials

Technologies

ROIC design

Modeling - simulation

Integration - packaging

Optics

Characterization

System

Image processing

Continuous transfer

From material to system
From photon to decision
3D INTEGRATION FOR IMAGE SENSOR

- How 3D improve image sensor:
  - Form factor decrease:
    - No WB, Buttable sensors for large array
    - X & Y axis reduction
    - Z axis by thinning
  - Performances improvement
    - Decrease R, C, signal delay
    - Increase device bandwidth
    - Decrease power consumption
  - Vertical integration of logic with sensor
    - Local signal treatment at pixel level
    - Fast acquisition
    - Reduction of SNR
3D IMAGE SENSOR APPLICATIONS

- **Visible light**
  - Cmos Image Sensors for consumers

- **X-rays / Elementary particles**
  - CERN: Medipix/timepix experiment
  - CERN: ATLAS experiment
3D EVOLUTION: FRONT SIDE CIS WITH CO-PROCESSOR DIE ON THE BACK

CMOS images sensor 3D demonstration at Leti (2012)

- 3D stack of 2 partitioned dies
- 65nm processor reported below a 130nm image sensor

From, P. Coudrain et al. ECTC 2013
BACK SIDE VS FRONT SIDE CIS PERFORMANCES

![Graph showing resolution vs pixel size and metal levels effect]

- Pixel size race decrease $1.4 \rightarrow 1.1 \rightarrow 0.9 \, \mu m$ for consumer ($5 \rightarrow 16 \rightarrow 24 \, Mp$)
- Photodiode efficiency challenge increases as pixel size decreases

Courtesy of Yole development
BSI is a key enabling technology to go to 3D integration because pads of the read-out layer are located on the same side of the image sensor processing chip (DSP). That configuration makes the integration easier by having direct access to each pixel site.

With FSI sensors, the 3D integration would be very difficult because TSVs should cross through the whole active pixel array.

End of 2012, Sony released the first stacked image sensor (see right picture).

In the future, 3D stacking will become more used as more functionalities will be required.
FROM 2D TO 3D CMOS IMAGE SENSOR

"All in one" integration
- Cost-effective for low-end image sensors
- Large chip size & low performance for midrange to high-end applications

Increased photodiode area by dissociation of image sensor and circuit read-out chip:
- Chip size can be reduced and more than 80% of the surface can be pixel array
- More processing can be integrated directly in the sensor
- Manufacturing process is optimized for the photodiode array and the readout circuit which gives better imaging performance

Courtesy of Yole development
3D STACKING IMPROVES IMAGER FILL FACTOR

<table>
<thead>
<tr>
<th>Phone Ref. (Year)</th>
<th>CIS Manufacturer</th>
<th>Resolution/Techno</th>
<th>Pixel size</th>
<th>Pixel Array Area</th>
<th>CIS Area</th>
<th>Dies per wafer (12-inch)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Motorola Razor (2011)</td>
<td>Omnivision</td>
<td>8Mp/BSI</td>
<td>1.4μm</td>
<td>16mm²</td>
<td>43mm²</td>
<td>1,500</td>
</tr>
<tr>
<td>Apple iPhone 4S (2011)</td>
<td>Sony</td>
<td>8Mp/BSI</td>
<td>1.4μm</td>
<td>16mm²</td>
<td>35.4mm²</td>
<td>1,816</td>
</tr>
<tr>
<td>Samsung Galaxy SII (2011)</td>
<td>Samsung</td>
<td>8Mp/BSI</td>
<td>1.4μm</td>
<td>16mm²</td>
<td>34.2mm²</td>
<td>1,884</td>
</tr>
<tr>
<td>Apple iPhone 5S (2013)</td>
<td>Sony</td>
<td>8Mp/BSI</td>
<td>1.5μm</td>
<td>18mm²</td>
<td>28.5mm²</td>
<td>2,268</td>
</tr>
</tbody>
</table>

Source: Yole

Hybrid sensor
Sony stacked CMOS imager with:
- Wafer-to-wafer bonding (oxide to oxide)
- TSV-last from front side
- Wire bonding for connection to substrate

Source: Sony, 2013
• 3D integration will first enable better pixel performance, but also enable a smaller die size and faster on-chip processing.
IMAGE SENSOR 3D HYBRID STACK TECHNOLOGY
STM – LETI

3D stacking
• Fine pitch interco thanks to Hybrid Bonding technology
• Top die optimized for pixel – keep only pixel layers

courtesy of J. CHOSSAT - STMicroelectronics - Imaging Division
Integration specs

- **Wafer**: 200mm
- **CMOS tech**: 0.13µm
- **Copper tech**: Double Damascene
- **Back End levels**: 12 (2x6)
- **Pitch**: 5µm - 24µm
- **Connections types**
  - lines [5µm x 10mm]
  - pads [5x5µm]
- **Alignment (x,y)** <500nm

System details

- **Visible RETINA 1000fps**
  - **BSI Sensor [Back Side Imager]**
    - Photodiodes for rolling shutter capture
    - Primary reading circuit
  - **Control logic unit [Memory + Individual Pixel Processing]**
    - Analog-to-digital converter
    - Massively parallel processing
    - SIMD components
  - **FPGA [Field-Programmable Gate Array]**
    - Baseband and large scale parallel signal processing

Operation

- **32 connections / Macropixel**
- **2 Modes**
  - High speed
  - High resolution
LETI HYBRID TECHNOLOGY HIGHLIGHTS

- Excellent wafer to wafer bonding (except outer ring)
- Exploration of design rule vs process
- Surface planarization with ultra low topology (low/wide scale)

- 6+6 BEOL metal levels bonded
- Ultra thin backside grinding (down to 5µm)
COOLCUBE™, POTENTIAL FUTURE 3D STACKED IMAGERS

- **Innovative miniaturized 4T pixels with backside illumination (BSI)**
  - Bottom layer: pinned photodiode + Transfer Gate
  - Top layer with 3 transistors

Multiple benefits:
- BSI integration → high quantum efficiency
- Photodiode area +35% for 1.4μm pitch pixel
- Only CoolCube can address these dimensions

*Coudrain et al., Towards a Three-Dimensional Back-Illuminated Miniaturized CMOS Pixel Technology using 100nm Inter-Layer Contacts, IEDM 2008*
3D IMAGE SENSOR APPLICATIONS

• Visible light
  • Cmos Image Sensors for consumers

• X-rays / Elementary particles
  • CERN: Medipix/timepix experiment
  • CERN: ATLAS experiment
**BUTTABLE DETECTORS ON ROIC**

**CERN – LETI project summary 2011 -2016**

- Product: hybrid pixel detector for medical applications
- TSV-last made in Medipix3 - Medipix RX – timepix3 wafers (IBM 130nm)
- Suppression of lateral wire bonding
- Buttable sensors assembly: no dead zone between sensor

**Medipix specifications**

- Wafer diameter: 200mm
- Wafer thickness: ~725um
- IC Technology: 130 nm / IBM
- Top Surface: Al + Nitride
- Chip size: 14100 x 17300 µm
- TSV per chip: ~100
- TSV aspect ratio:
  - H120:D60 µm (MEDIPIX RX)
  - H50: D40 µm (timepix3)
TECHNOLOGY ILLUSTRATION AND RESULTS

TSV Medipix3/RX results – 2012-2015

TSV Medipix3/RX results – 2012-2015

6 lots run at LETI

Technology

Back side UBM

Medipix wafer after front side UBM

Accoustic image of the bonding interface

TSV:

RDL Cu 7 µm

60µm x120µm

Thin wafer debonded on tape

Electrical Tests

P01-Resistance cumulée Chaine de 2 TSV (VSS)

2 TSV chain resistance

TSV Last for Hybrid Pixel Detectors: Application to Particle Physics and Imaging Experiments

D. Henry(1), J. Alozy(2), A. Berthelot(1), R. Cuchet(1), C. Chantre(1), M. Campbell(2) ECTC 2013

Functionnal tests on ASICS
MEDIPIX3 FUNCTIONAL RESULTS (2013-2014)

Using the same test program as Wafer probing, generating the same classification. (Readout interface is a Fitpix USB device)
2 Wafers tested chip by chip (1 day of measurement per wafer)
→ No yield loss due to TSV technology except on wafer edge due to process edge exclusion

One TSV processed wafer was sent to ADVACAM company for:
- Dicing of thinned wafer and selection of “good” chip candidates
- Sn-Pb solder spheres were processed on Edgeless Sensor

BGA pads on the back side redistribution layer have been prepared with low temperature solder spheres
Assembly has been done manually for several chip and the obtained “BGA” components could be mounted using standard equipment but with some care due to its fragility

First image obtained with a TSV processed hybrid pixel detector (flat field corrected)
Sensor 500\( \mu \text{m} \) (edgeless)

Chip thinned to 120\( \mu \text{m} \)

Sensor 200\( \mu \text{m} \)

Chip 750\( \mu \text{m} \)

Wirebonds for sensor HV bias

ASIC wire bonds

TSV: CEA-Leti, FR
Flip chip: Advacam, FI

Wire bond for sensor HV bias
TIMEPIX3 (SI AT 50 MICRONS) WITH TSV-LAST FUNCTIONAL RESULTS (2015)

- Under bump Metallurgy (TiNiAu) on pixel pads
- Wafer bonding on temporary carrier (SAM inspection showing good bonding)
- Wafer thickness profile after thinning to 50 µm (53 +/- 2 µm)
- TSV etching to bottom oxide (diameter = 40 µm)
- Daisy chain TSV resistance mapping
  Yield = 88%
- 50 µm Thinned timepix wafer diced on tape
- Timepix die from back side showing redistribution of I/O signal on BGA pads

G. Pares CEA-leti - INFIERI WS Lisbon | 23
Particle detectors for ATLAS experiment (CERN)

- Realization of 60 µm fine pitch Cu pillars
- Stress management of ultra large & thin ASIC Read-out IC
- TSV-last on going

- Develop an alternative wafer level back-side process, called Stress Layer Compensation (SLC), that compensates for the CTE mismatch of the ROIC CMOS front-side stack
- Compensation effect needs to be dynamically effective with temperature ranging from ambient to solder reflow (260°C)
Wafer level technology modules processed on FEI4 ROIC wafers

FEI4b deformation during temperature excursion corresponding to solder reflow

Simulation with 4 µm of SiN = Ideal results

SLC = SiN C 1µm/AlSi 4 µm

⇒ Already 4X reduction of bow amplitude with SCL
RECENT STRESS LAYER COMPENSATION RESULTS

Deposition at die level
With film delamination

Over compensation (Al film too thick)

Need to add static compensation to be close to 0 line

Best dynamic compensation

Deposition at wafer level
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Micro-bumps DRM & schematic

- Wafer size: **300 - 200 mm**
- Micro-bumps material: **Cu post / SnAg 305 solder**
- Minimum pitch: **40 µm**
- Minimum micro-bumps diameter: **20 µm**
- Micro-bumps thickness (typical): **Cu 10µm / SnAg 10µm**

Micro-bumps Morphological illustrations

Micro-bumps before reflow  
Micro-bumps after reflow

Micro-bumps on **C65**  
D = 25 µm

Micro-bumps on **FDSOI28**  
D = 18 µm
µbump pitch available at 20 µm on 300 mm wafers @LETI

From C. Ribière CEA-Leti 2015
<table>
<thead>
<tr>
<th>TSV diameter</th>
<th>30 µm</th>
<th>40 µm</th>
<th>50 µm</th>
<th>60 µm</th>
<th>80 µm</th>
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<tr>
<td>AR 1:1 &amp; 1.5:1</td>
<td><img src="1" alt="Image" /></td>
<td><img src="2" alt="Image" /></td>
<td><img src="3" alt="Image" /></td>
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<tr>
<td>AR 2:1</td>
<td><img src="6" alt="Image" /></td>
<td><img src="7" alt="Image" /></td>
<td><img src="8" alt="Image" /></td>
<td><img src="9" alt="Image" /></td>
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<tr>
<td>AR 3:1</td>
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<tr>
<td>AR 5:1</td>
<td><img src="16" alt="Image" /></td>
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<td><img src="18" alt="Image" /></td>
<td><img src="19" alt="Image" /></td>
<td><img src="20" alt="Image" /></td>
</tr>
</tbody>
</table>
TSV Last : high reliability driven
- Increased Si thickness with High AR TSV -> 3 to 5
- TSV mineral passivation (harsh environment)
- TSV polymer filling

TSV mid : high density driven
- Increased Si thickness with High AR TSV -> 10 -> 15 -> 20
- Alternative technology AR20 (development 2015)

Temporary bonding
- Zone bond 200 & 300mm
- Low temperature (200°C)
- High temperature (400°C) ongoing development on disruptive technology
OPEN3D PLATFORM PARTNERING WITH CMP WORK FLOW OFFER

- **Wafer fabrication in foundry**
- **Wafer reception at LETI**
- **Design & Layout & DRC**
- **Dicing & Packaging**
- **CMP MPW wafer service**
  - Customer interface
  - 3D modules identification
  - Order form
- **3D Electrical Tests**
- **LETI 3D Technology implementation**
  - Interconnections
  - TSV
  - Metallization
  - Components stacking

G. Pares CEA-leti - INFIERI WS Lisbon
• Image sensor has long been a key driver for 3D and will continue to be particularly with the hybrid wafer-to-wafer stacking of sensor with logic/memory

• Continuous developments in 3D technology field involve:
  • High density and fine pitch interconnections
  • Fine pitch TSV interco
  • Hybrid copper bonding
  • Reliability for critical applications (automotive, aerospace, medical)
  • Thermo-mechanical constraints, stress management

• CEA-Leti can provide a broad and mature 3D technology portfolio:
  • µbumping and solder interface CMOS post-processing
  • Flip chip stacking D2D and D2W
  • TSV-last
  • Cu-Cu wafer to wafer bonding
  • MPW is available for 3D technologies provided by CMP/Leti
THANK YOU FOR YOUR ATTENTION

QUESTIONS ?