Data Transmission Developments for LHC Experiments

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Overview

At Nikhef, we work on several lines of research for data transmission in the LHC (ALICE, ATLAS, LHCb) experiments

(and beyond, *e.g. the deep-sea networks of KM3NET, a complex systems of electro-optical cables and optical fibre components providing connection between the sensors in the deep sea and the control room in the shore stations*)

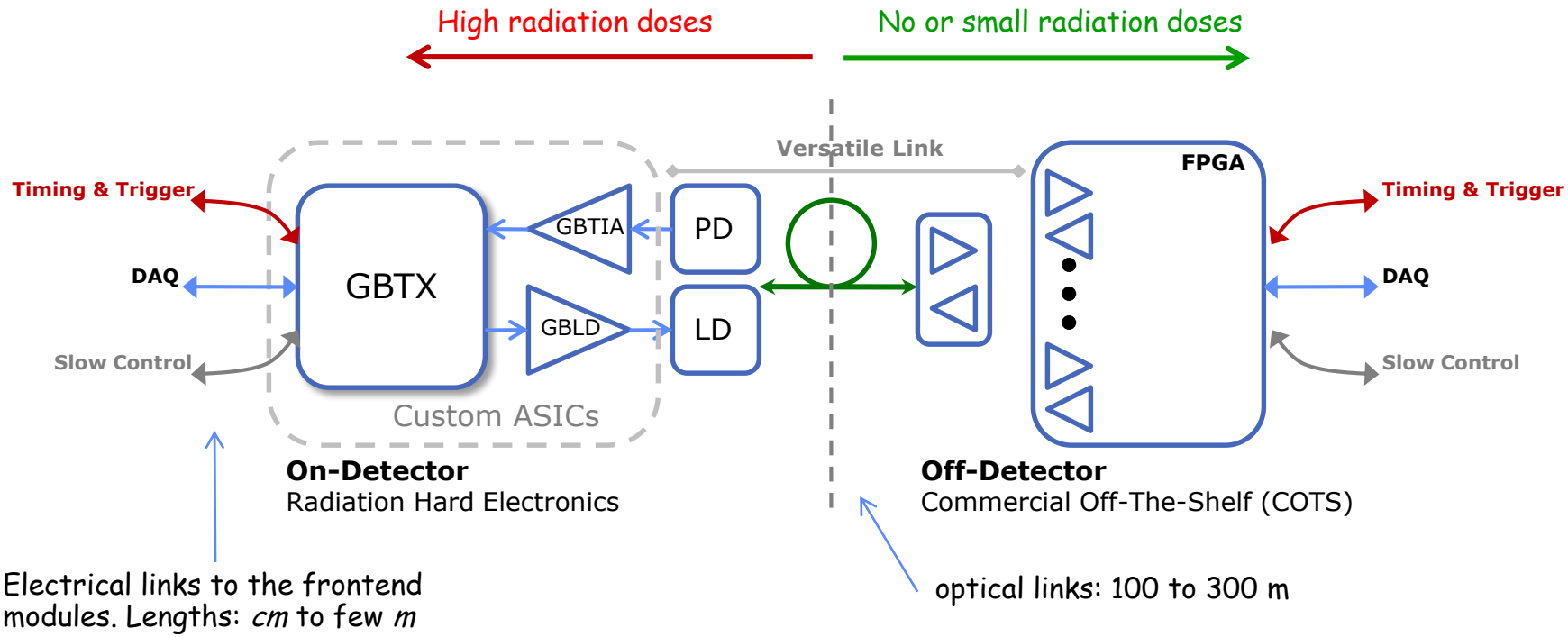
We can group these under two main lines:

- low-power ASIC readout
  - e.g. serializater and wireline driver (GWT) for VELOpix
  - *see Elena's talk*

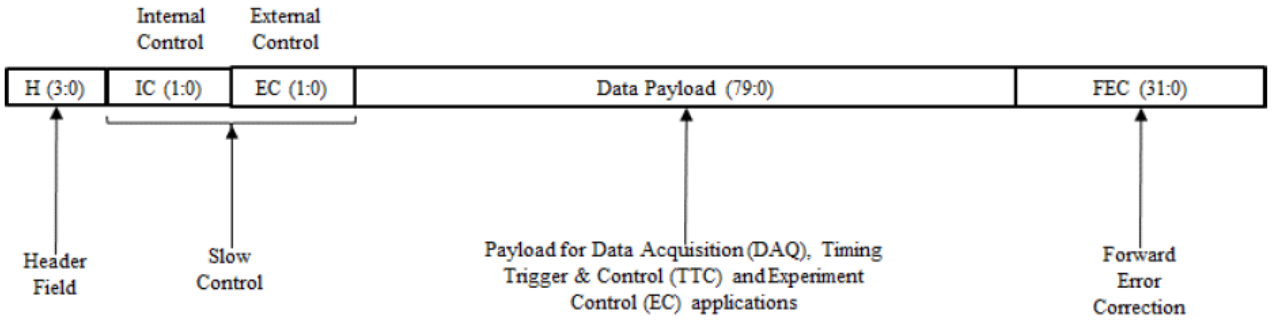
- GBT and FPGA-based serialization protocols
  - architecture based on GBT serializer
  - usage of flash-based FPGAs on detector
  - will say a bit in this talk on prototypes and test systems

GBT Architecture

Data transmission architecture adopted by LHC experiments for their forthcoming upgrades is based on the GigaBit Transceiver (GBT)



Data frames usable both for DAQ and Control



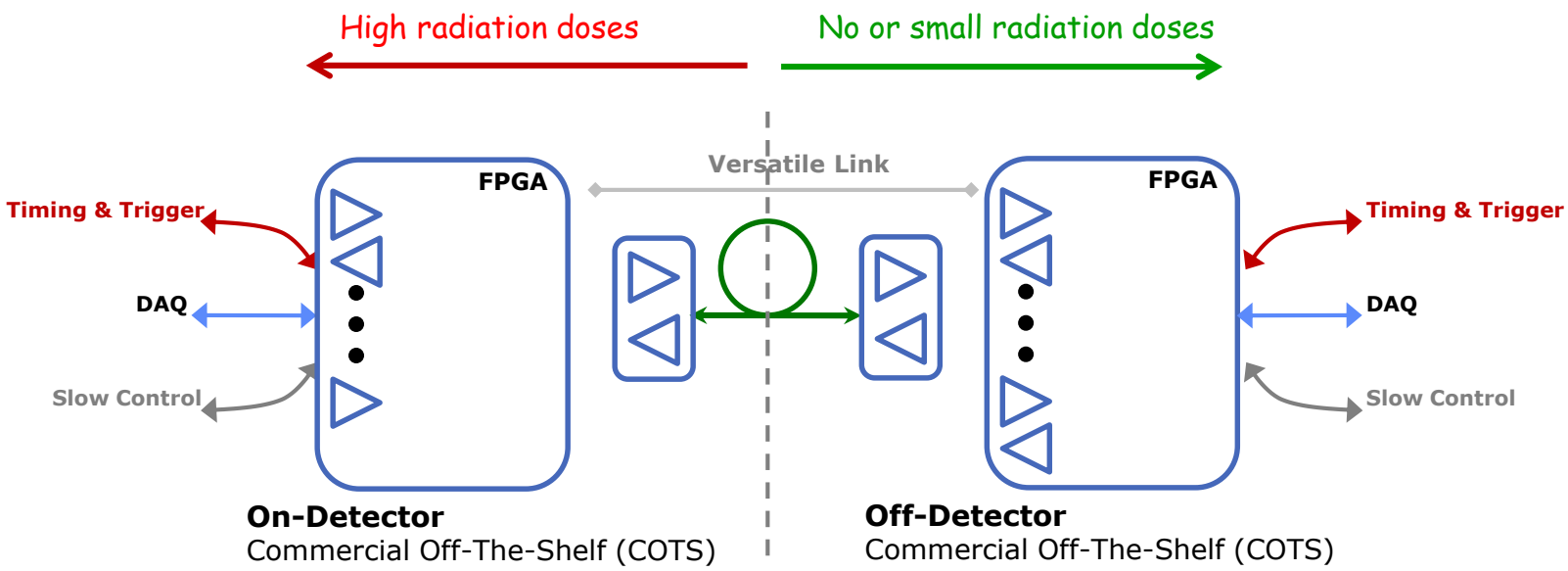
Plan of the talk

I will focus on activities in which Nikhef is involved (my institute)

In particular related to LHCb (my experiment)

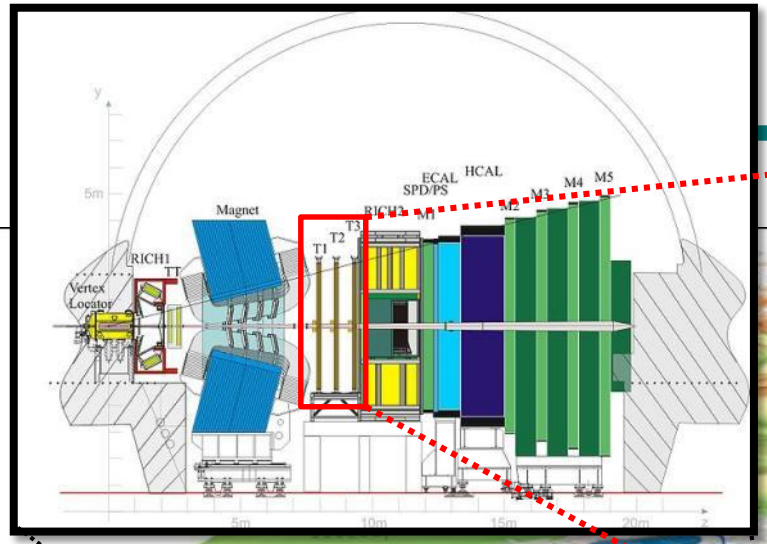
In particular using the GBT ASIC (my detector)

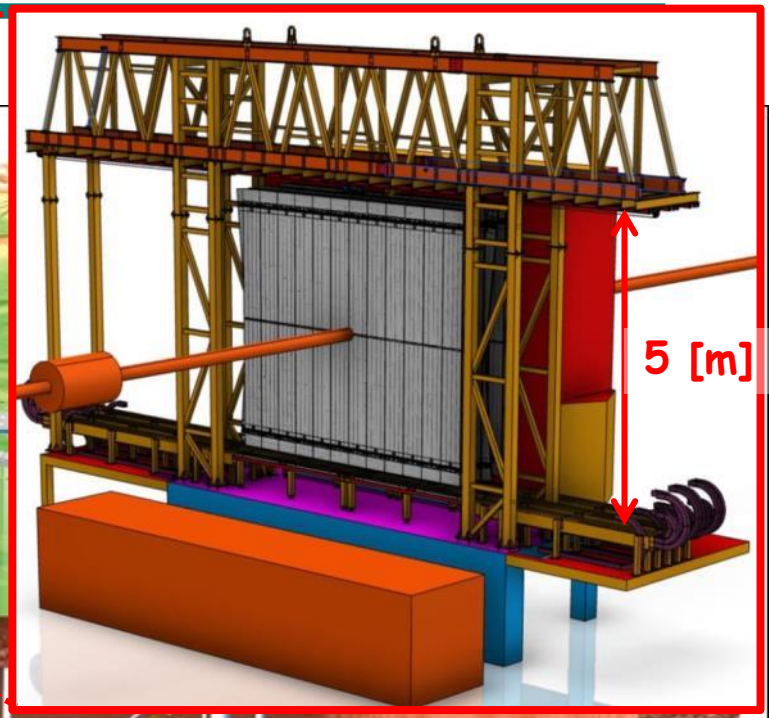
But please keep in mind that this is also a possible solution…



… e.g. we tested transceivers on board of flash-based FPGAs

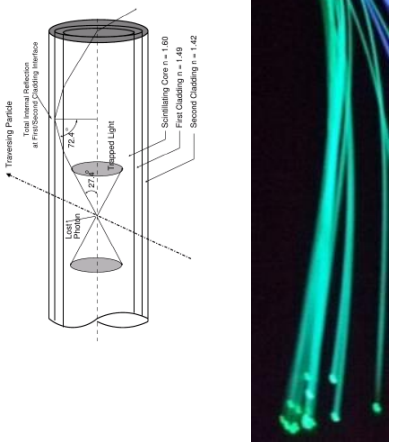
LHCb SciFi Tracker



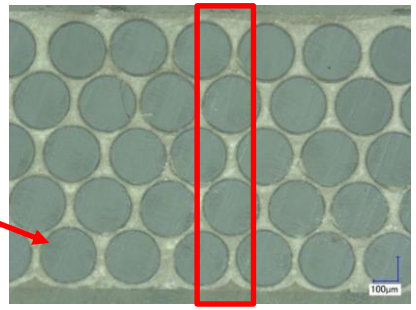


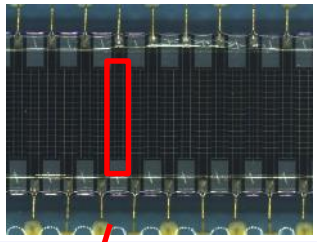
Overview

2.5 m × 250μm Fibres



Fibre mats 2.5m ×13cm

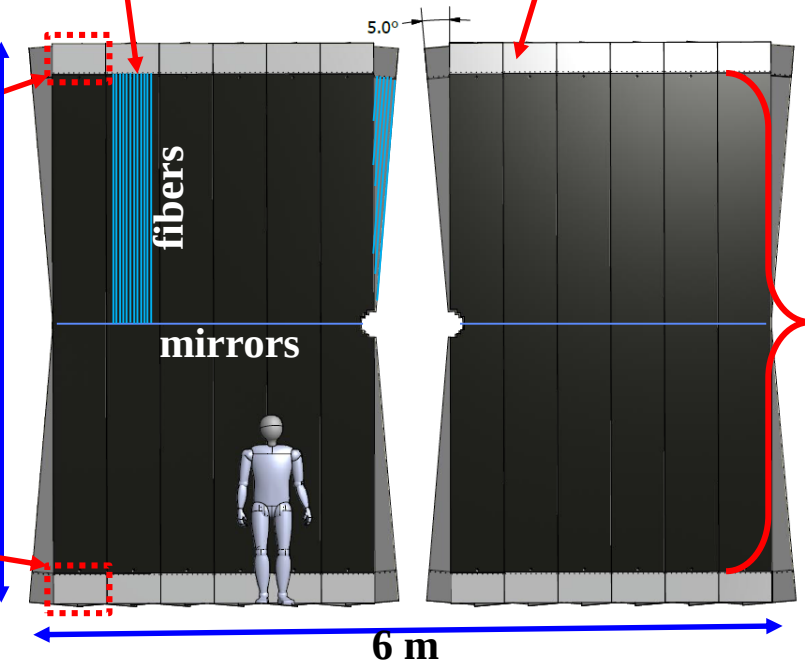




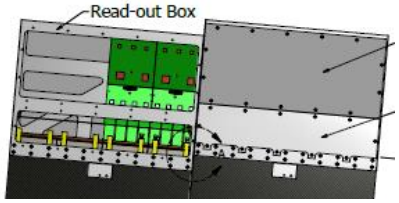
Silicon PM (SiPM) array: 128 × 250μm

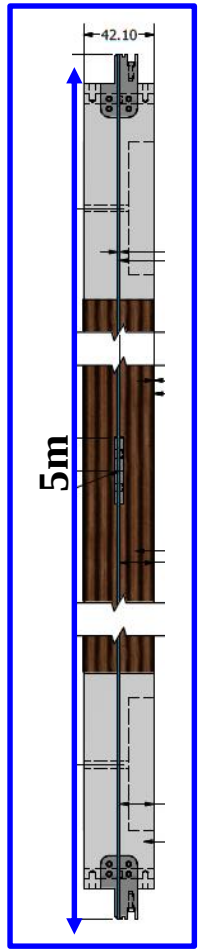
Modules = Supporting panels + mats

3 * X-U-V-X

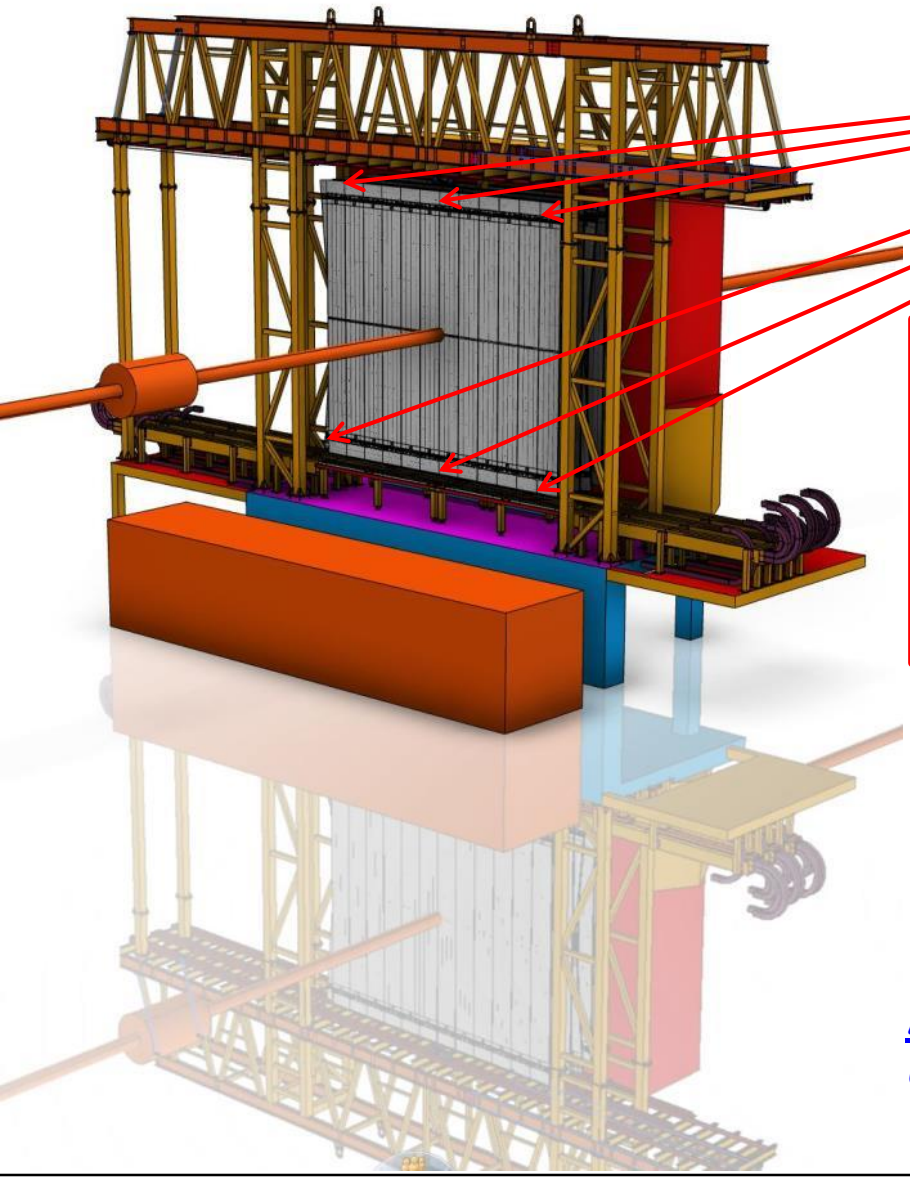


Readout box (ROB)
SiPMs (-40°C)
and FE boards



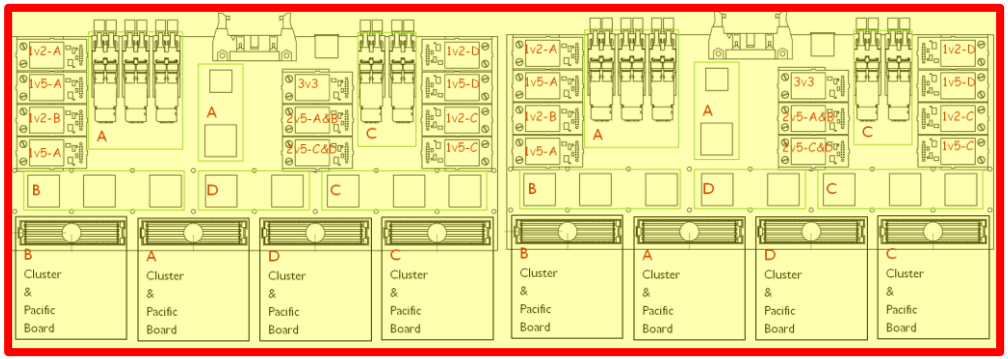


SciFi Data



24 ROBs per layer

16 data links (GBT) per ROB
4 ctrl links (GBT) per ROB



288 ROBs in total

4608 data links @4.48 Gbps

1152 data links @3.20 Gbps

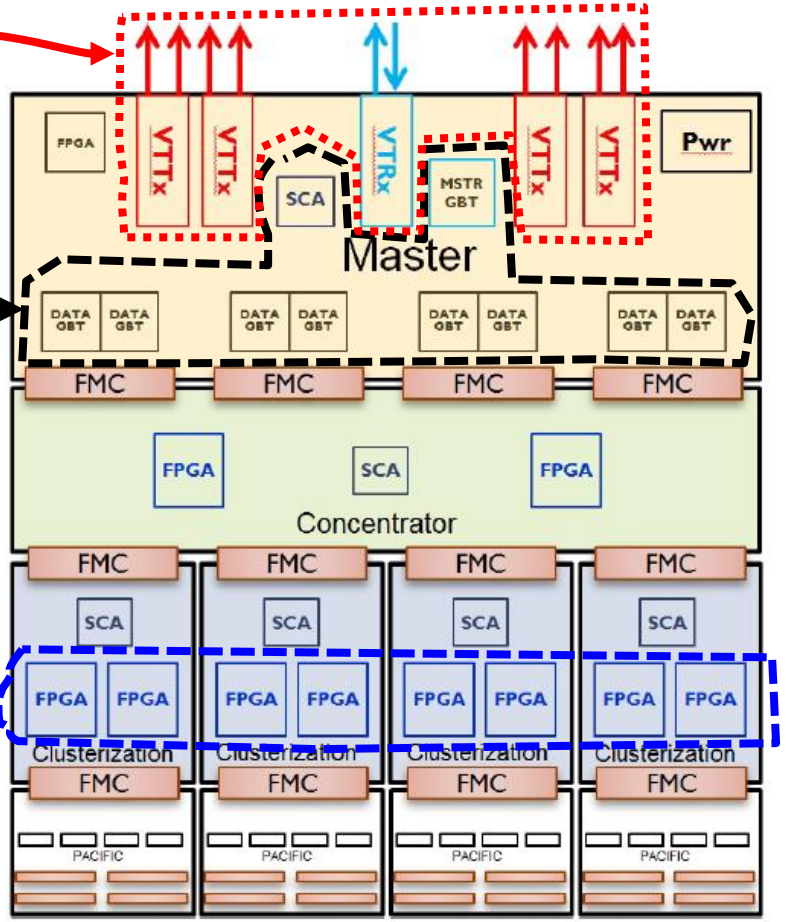
N.B. LHCb will operate a trigger-less FE architecture, all FE data will be "passed" to the event-builder CPU farm

Building Blocks

Versatile Links

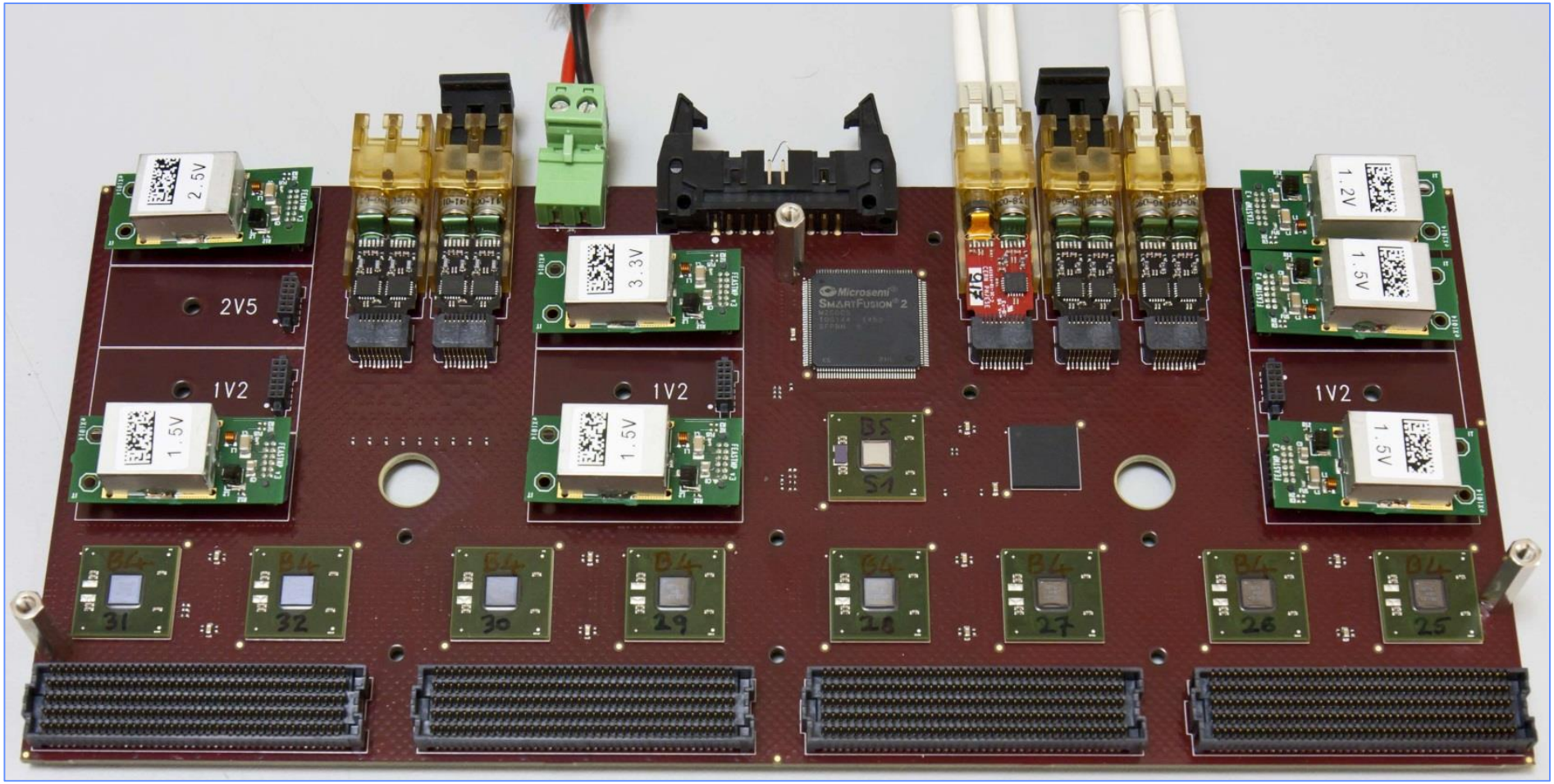
GBT chip set

Flash-based FPGAs (Microsemi)



1st "Complete" SciFi Front-End

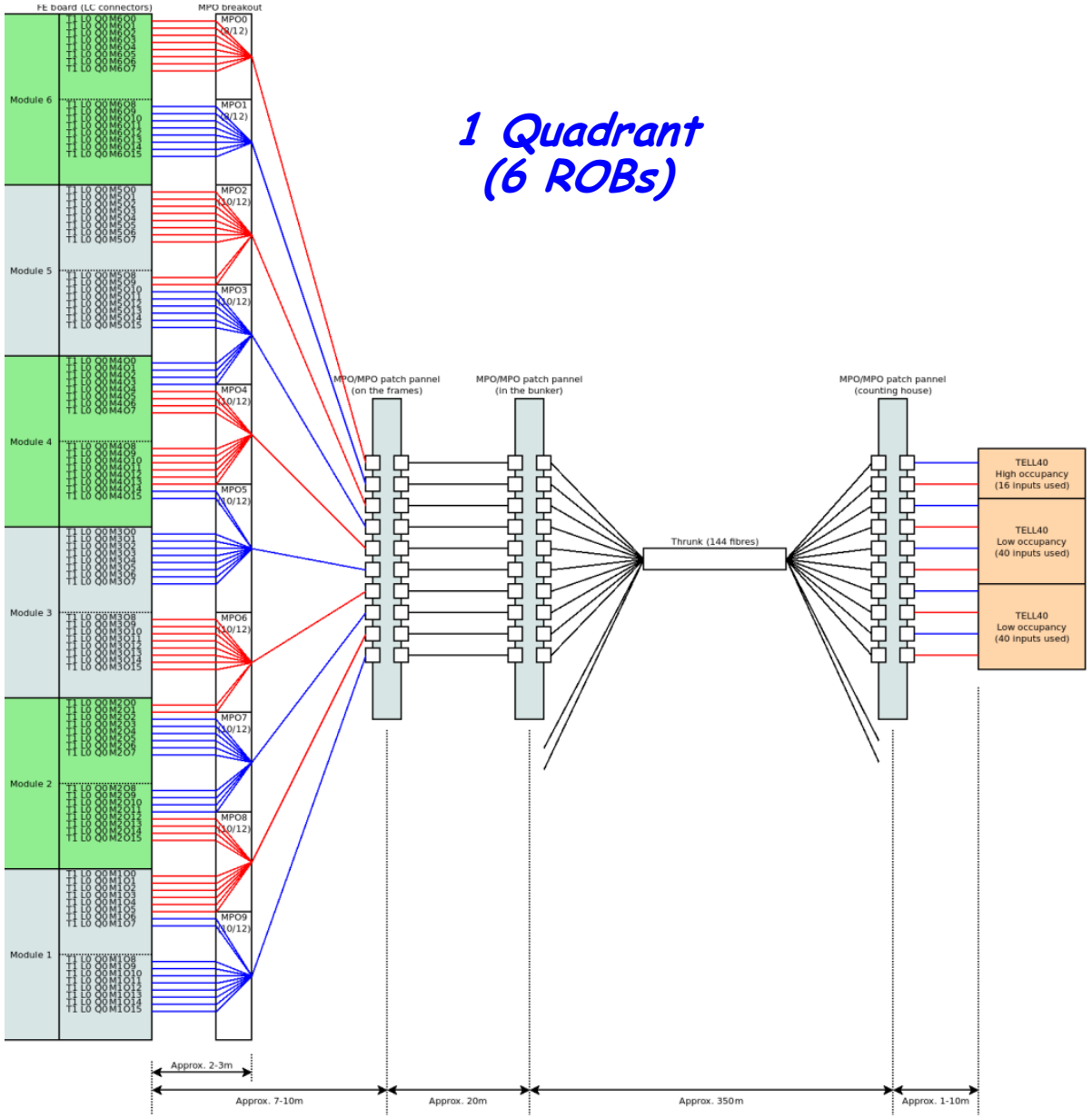
Master Board



- 2 (bidirectional) GBT links for control
- 8 GBT links for data sending

• published on "Bits & Chips (NL)"

Optical Network



1 Quadrant (6 ROBs)

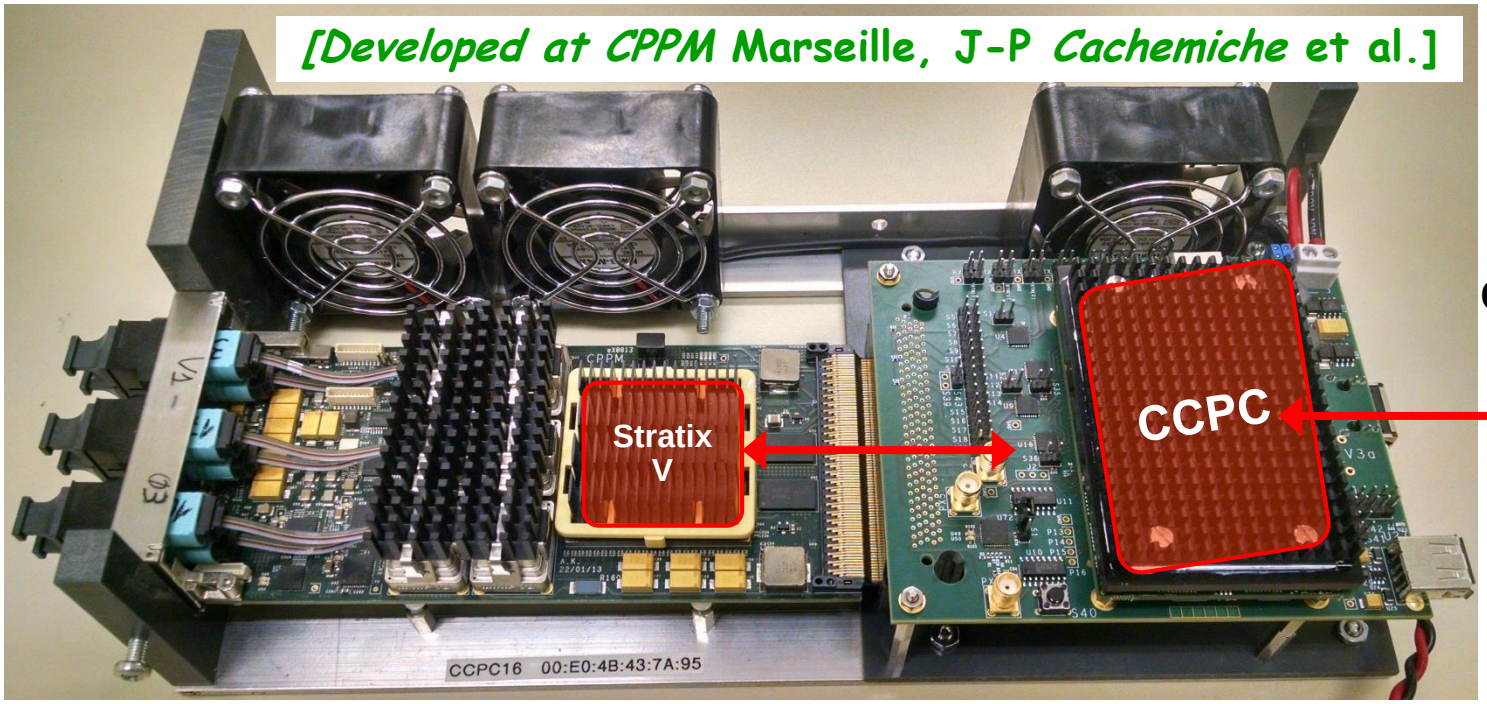
48 "trunks"
576 ribbons
6912 fibers

16 inputs

40 inputs

40 inputs

Prototype of Back-End Electronics



DATA
(GBT+10GBe)

CONTROL
(1GBe)

AMC40

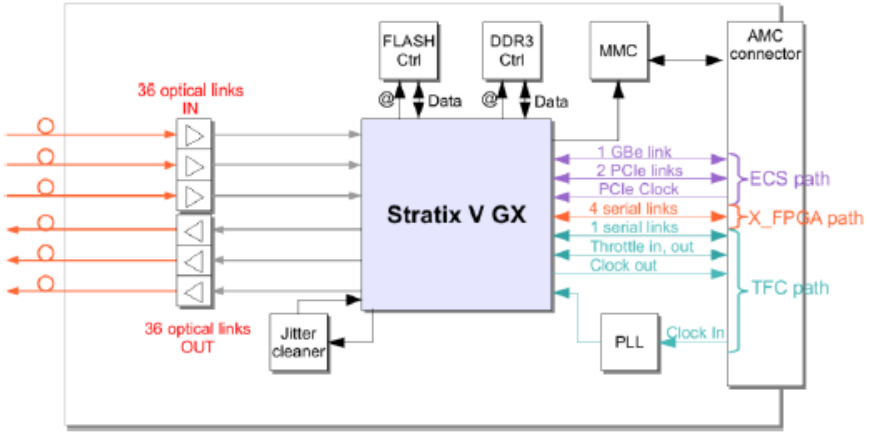
AMC_TP with a CCPC

General-purpose readout and control system based on optical links, Stratix V FPGA and GbE

PCIe-40 Back-End

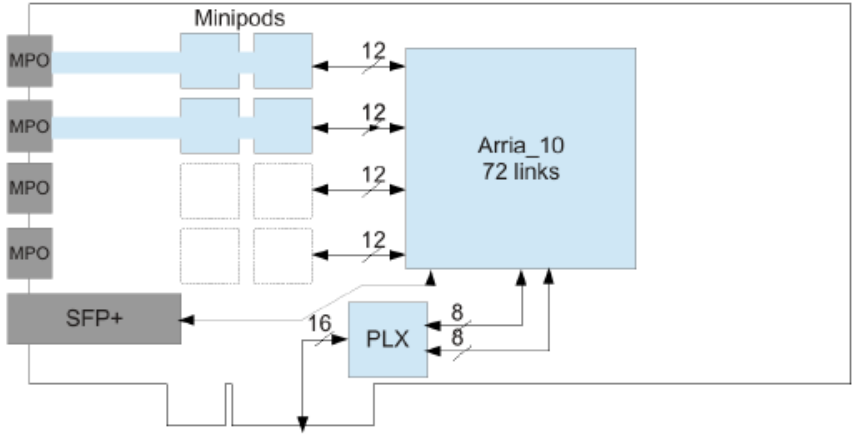
Presently moving to PCIe-based architecture

AMC40



- Stratix V
- x36 optical links
  - x24 GBT
  - x12 10GBASE-R
- ~10Gbps x 12

PCIe40

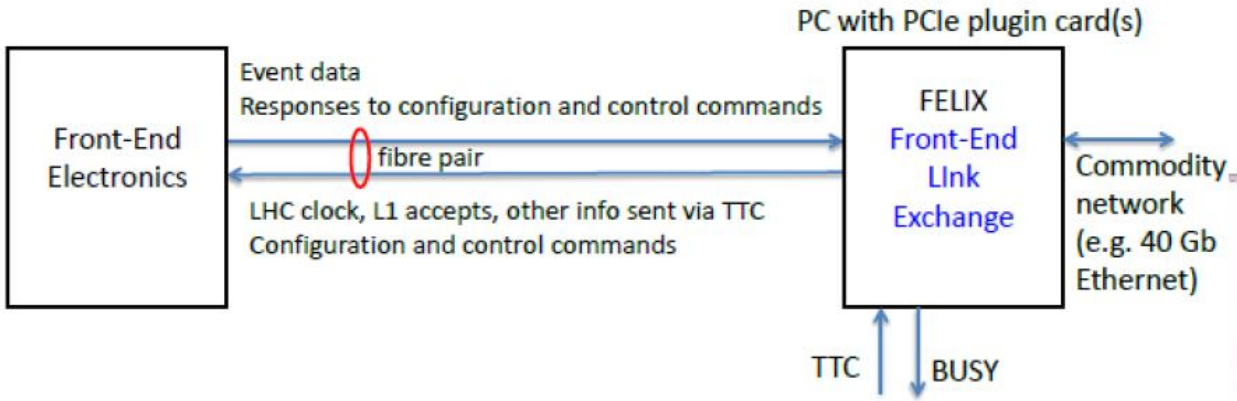


- Arria X
- (Up to) 48 optical links
- x2 PCIe Gen3x8 → Switch → x16
- ~55 Gbps x 2

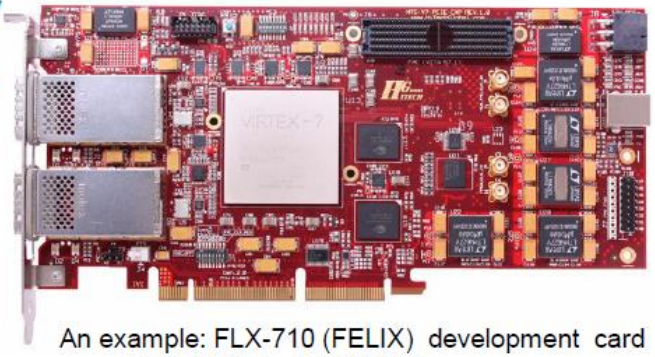
Intermezzo - FELIX

- Nikhef most important Phase-1 hardware upgrade project (intention to contribute to FELIX also for Phase-2)
- FELIX – FrontEnd LInk eXchange
- A new approach for interfacing the Front-End electronics in Phase-1 for the New Small Wheel muon detectors and new first-level trigger electronics making use of data of the LAr calorimeter
- Interfacing for the DAQ and DCS for the NSW detectors and the LAr L1 and L1Calo systems

Nikhef people involved:
- Frans Schreuder
- Andrea Borga
- Henk Boterenbrood
- Jos Vermeulen
- Mark Donszelmann

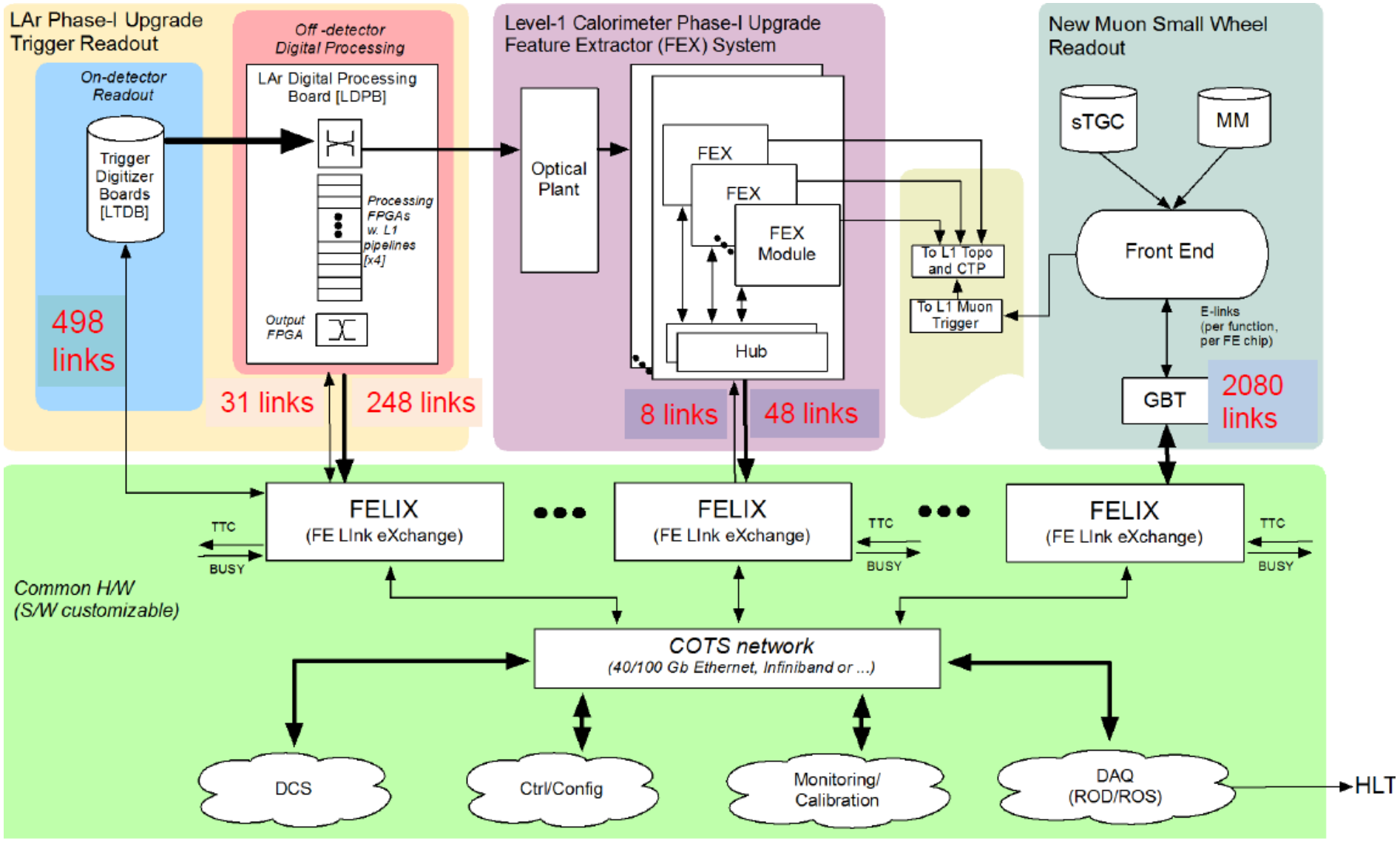


- FELIX acts as intelligent switch: server PCs connected to commodity network send and receive data via FELIX -> functionality implemented currently in firmware implemented in software: better maintainability, no dependence on firmware developers, software running on COTS hardware
- FELIX for Phase-1: COTS server PCs with PCIe cards
- Fibre pairs transfer different types of information for which currently separate connections are used

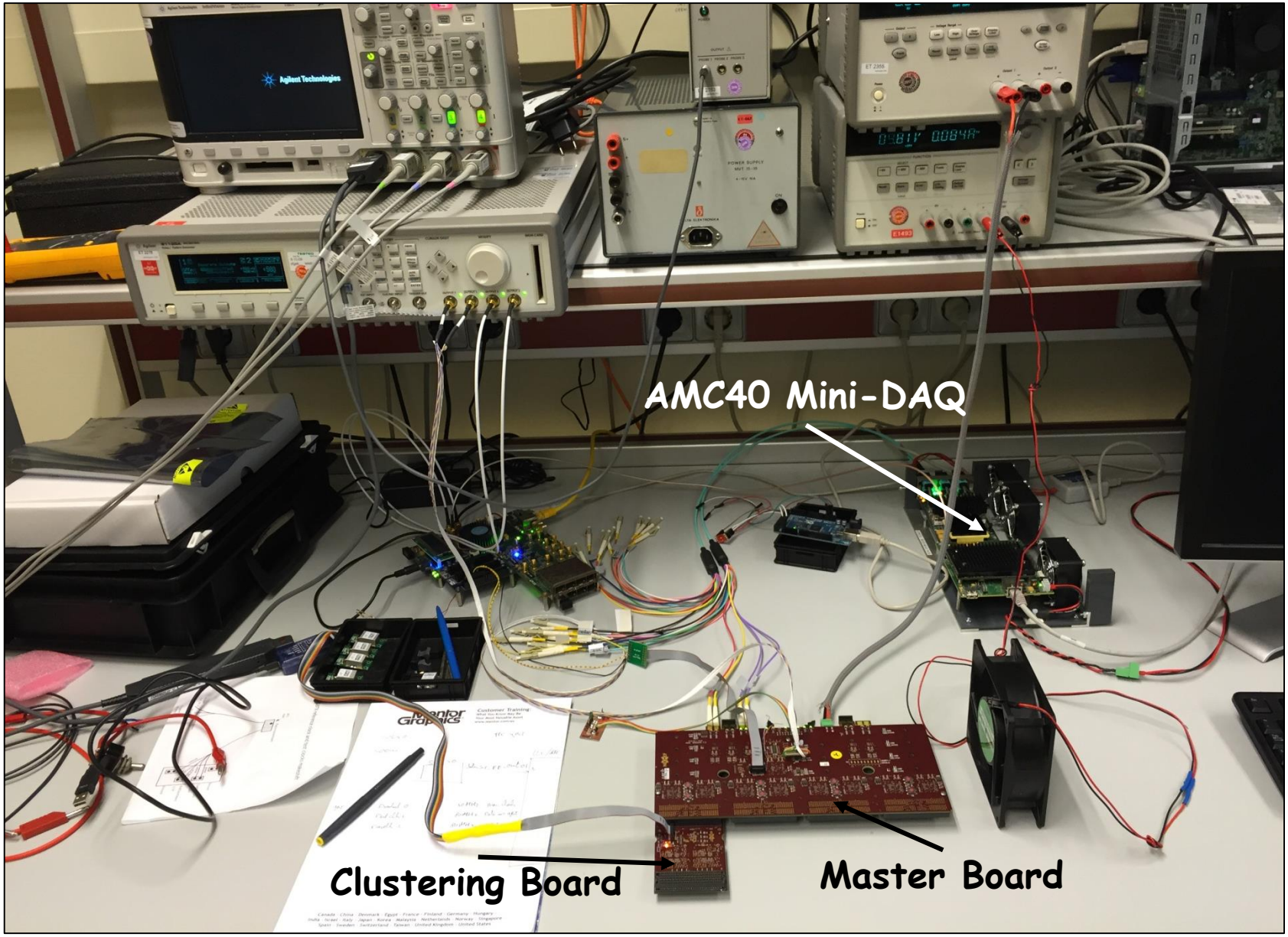


An example: FLX-710 (FELIX) development card
- HiTech Global HTG-710
- Virtex-7 X690T
- PCIe Gen 3 x 8 lanes
- 2x12 bidir CXP connectors
- FMC connector

Intermezzo – FELIX (cont'd)

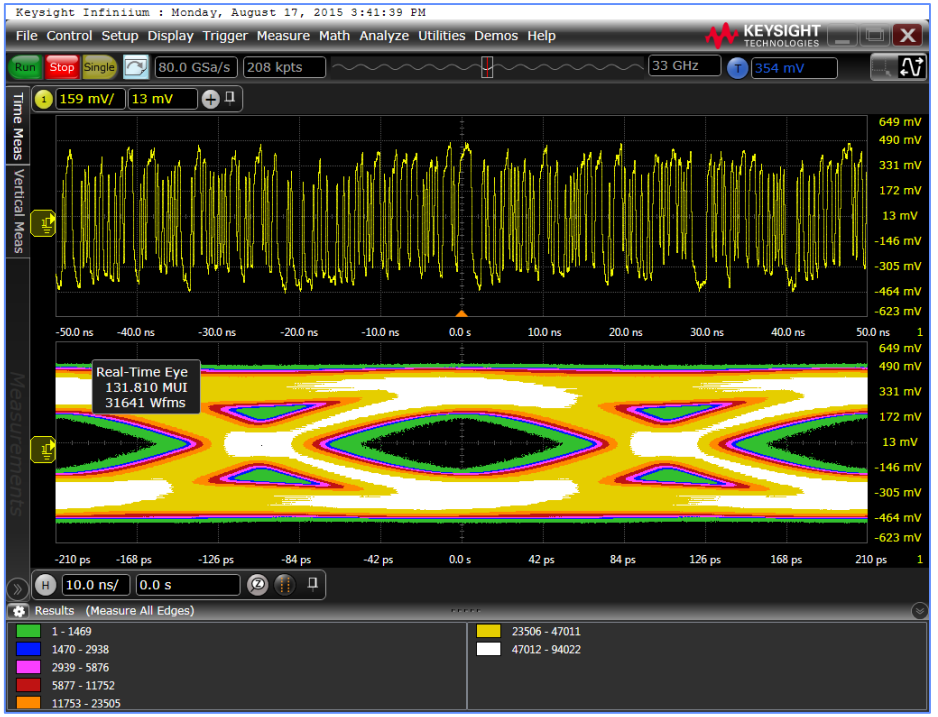


Test System Completed

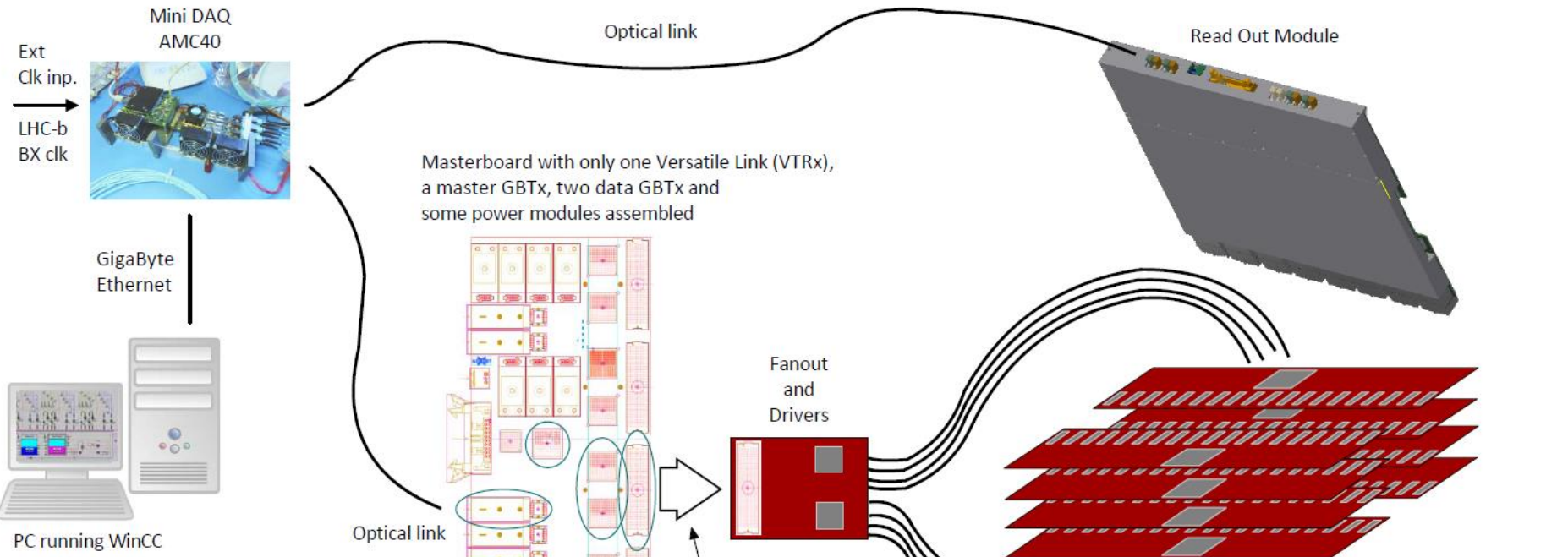


Data Transmission Tests

- SciFi uses GBT wide bus protocol (112bits @40 MHz)
- AMC40 contains also slow and fast control firmware ("SOL40") as well as DAQ firmware
- Eye pattern measurement at the input of the Versatile link VTTx
  - Eye opening of 354 mV
- Data link stable in the AMC40 mini-DAQ receiver
  - Send data from GBT in test mode to AMC40
  - Send data from clustering FPGA to GBT to AMC40
- Basically validated SciFi data transmission scheme

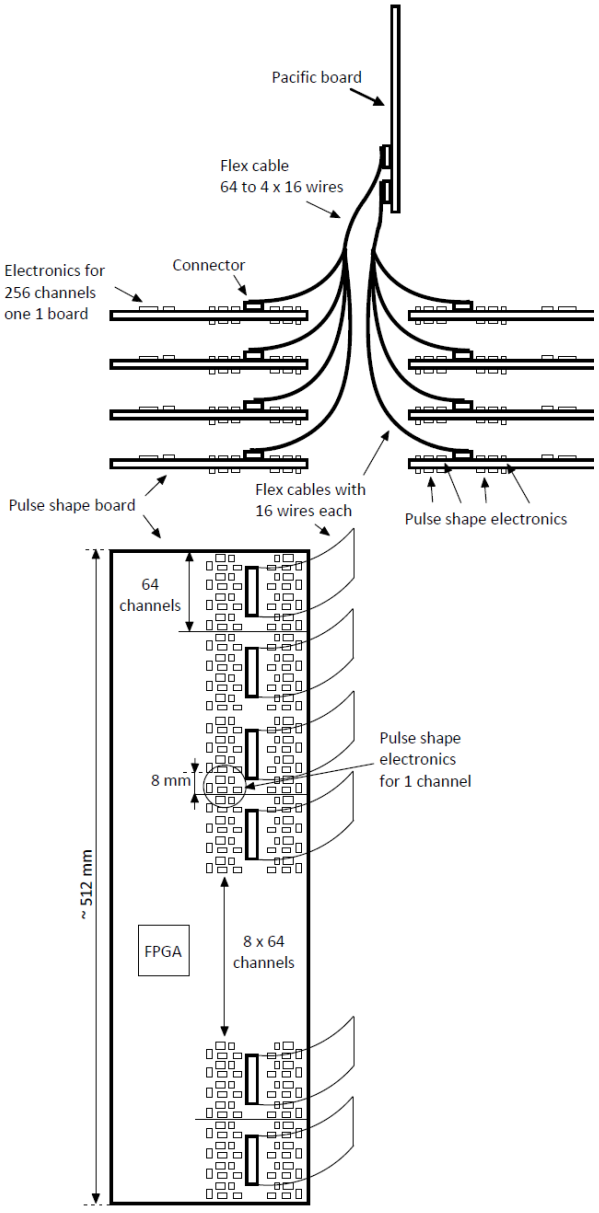


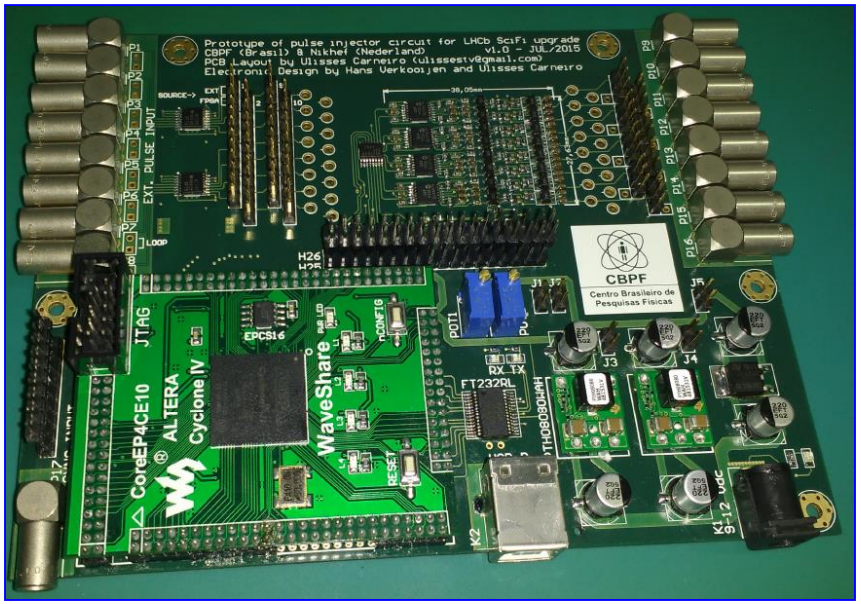
Building an automatic test-system

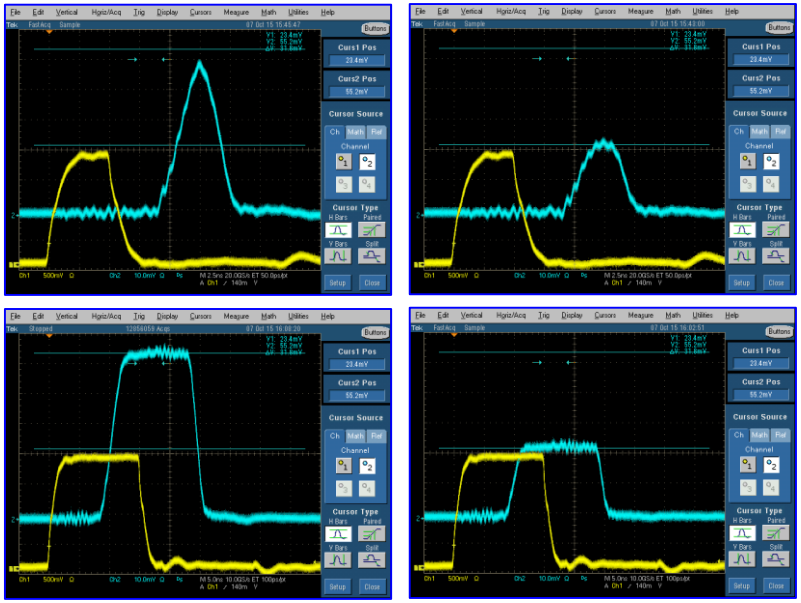


The control bus transmission protocol is based on the HDLC standard.
Each printed circuit board with pulse forming networks has 256 channels
Data to one of those boards contain
8 bits for channels address
1 bit to switch the channel on or off
5 bits to delay a channel pulse from 0 to 12.5ns in steps of 390ps relative to the calibration pulse
5 bits to adjust the channel pulse width with a delta time of 12.5ns in steps of 390ps
8 bits to adjust the amplitude of the channel pulse +/- 25% of its nominal value. 1 LSB equals 0.2%

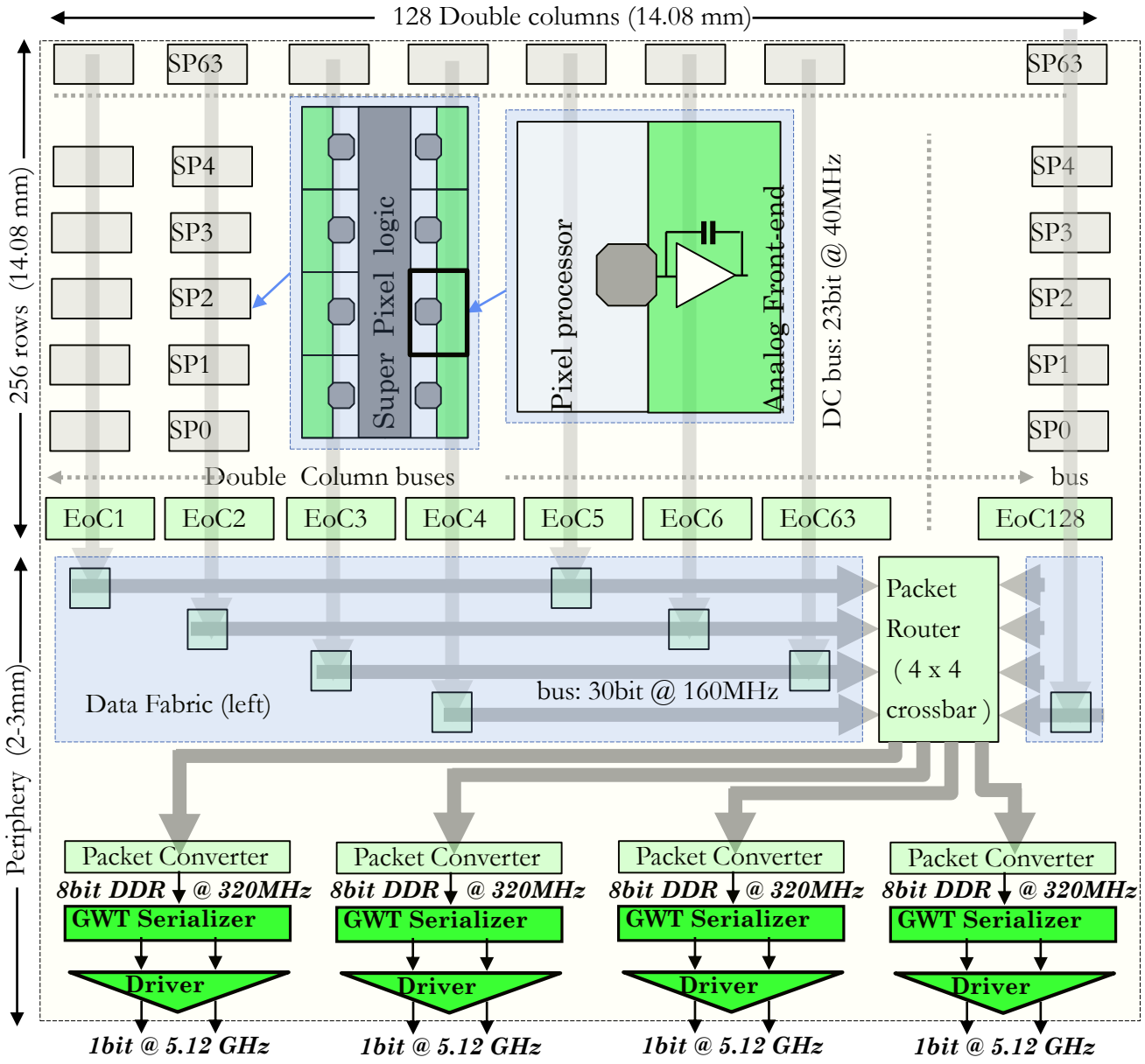
Test-system Prototype







Velopix

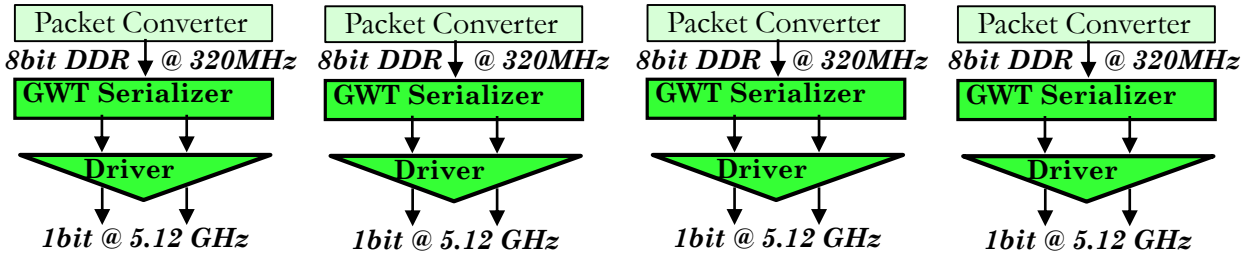


You will hear about VELO and VeloPix in Elena's talk

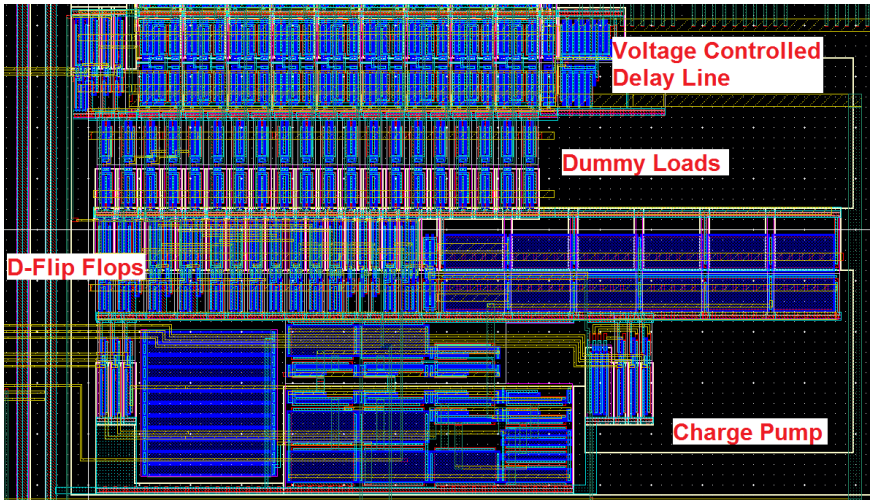
here I just want to give a short update on the GWT serializer, that is being ported to 65nm TSMC

And report shortly on some signal integration checks we performed at Nikhef

GWT Serializer

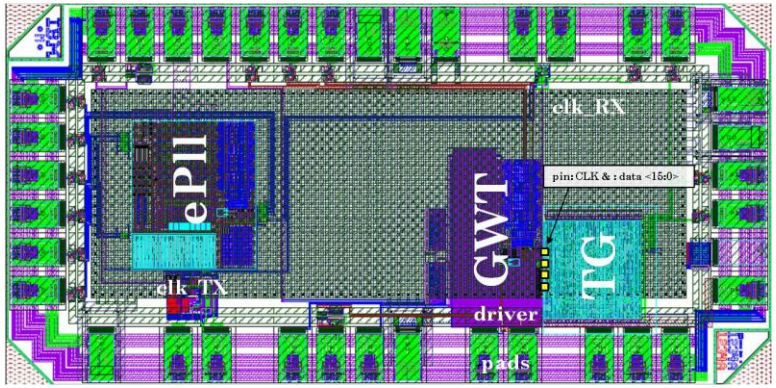


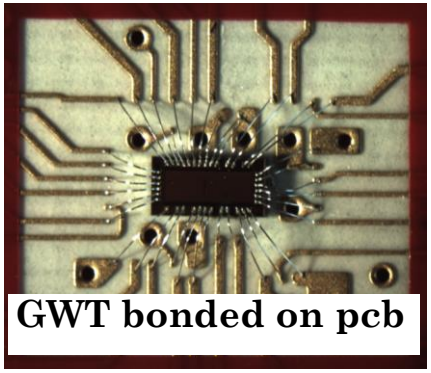
- In parallel to the VeloPix production in 130nm TSMC technology (taking place this year, see Elena's talk), we migrated the present 5.12Gbps circuit from 130nm TSMC to 65nm TSMC
  - Mangleshwar Srivastava is submitting the design in May in the framework of the RD53 collaboration (ATLAS-CMS pixel readout chip for SLHC)
  - in parallel, we are working on the design (Nina Beschoor Plug) of a 10.24Gbps version in 65nm TSMC (e.g. for MediPix-4 and TimePix-4)



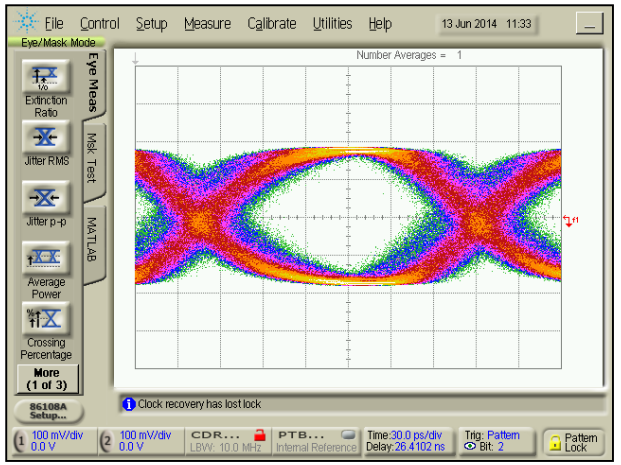
Prototype in IBM 130nm

- Test chip produced on IBM 130nm MPW run to evaluate GWT design




GWT bonded on pcb

- evaluation tests performed with dedicated setup
  - phase mismatch ok : 50ps p-p (25% UI)
  - eye diagram opening ok : ~ 60ps @ ±200mV (30% UI)
  - low internal phase noise
  - jitter on ref. clock (ePll-generated)
  - comfortable bandwidth and voltage operational limits



- main activity now around redesign in 130nm TSMC technology

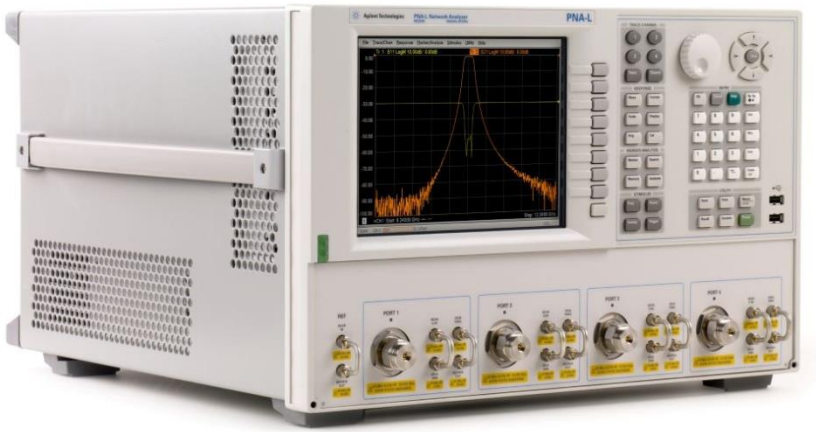
Signal Integrity

If you work at high-speed data transmission, you have to worry about signal integrity *(clean and fast transitions, stable logic levels, no transients, accurate timing, etc.)*

If you have tried to build setups to test your design prototypes, you are aware of the challenges posed by rising bandwidth (transmission line effects, cross-talks, EMI, clock distribution, …)

At Nikhef, we took the challenge seriously and equipped ourselves with

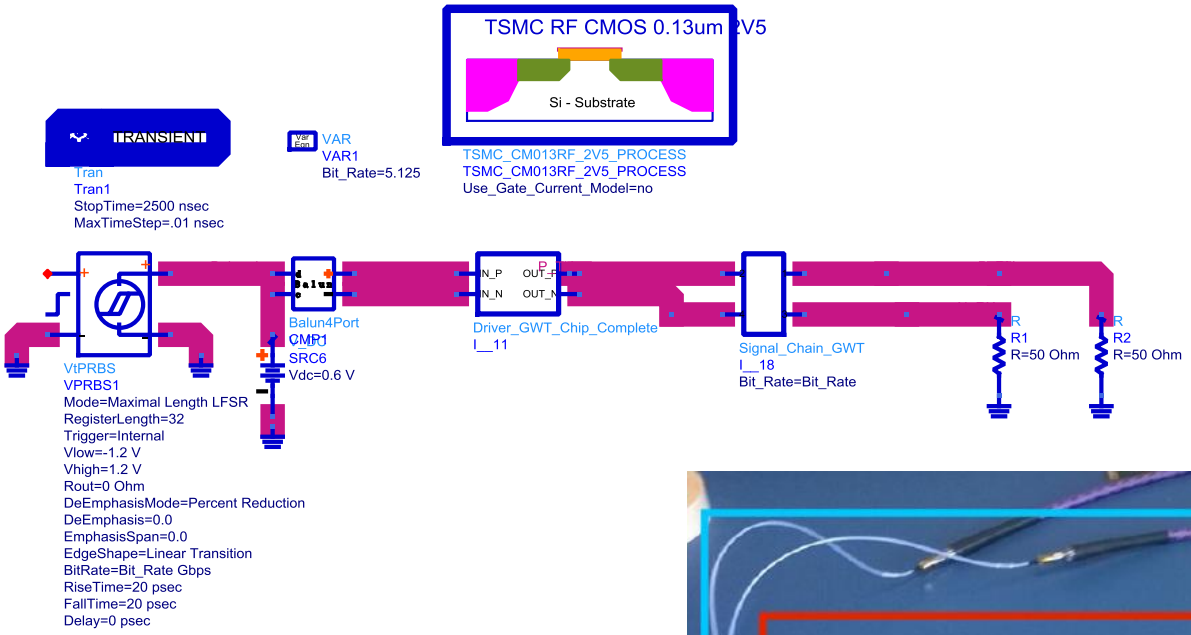
- simulation software (ADS by Keysight EEsof EDA)
- 4 port Vector Network Analyser (Agilent VNA N5230C, up to 20Ghz)
- 35 GHz Sample Scope

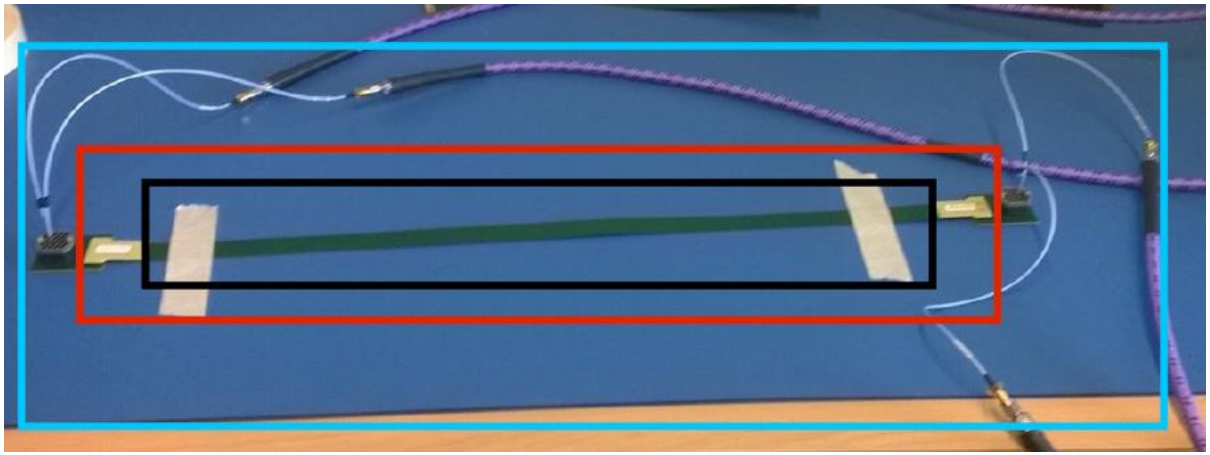


GWT Signal Integrity Test Setup

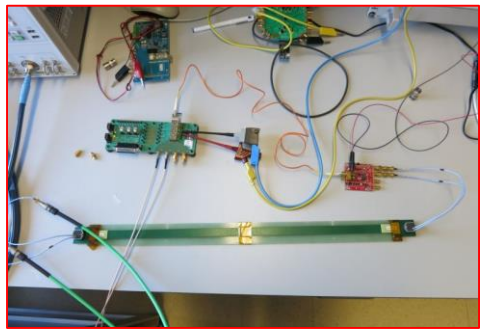
Output driver of GWT TSMC 130nm

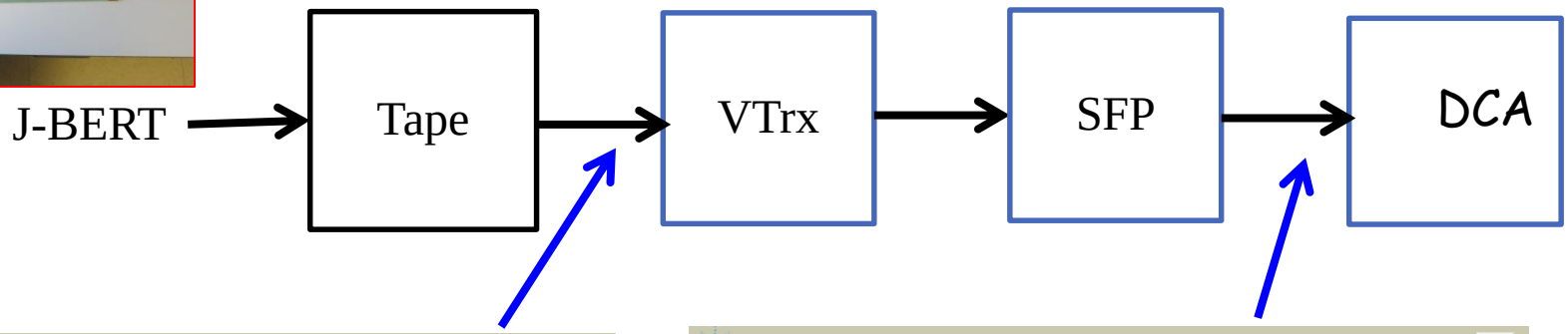
- **Cable model**
- **Measurement with a cable similar to those that will actually be used**

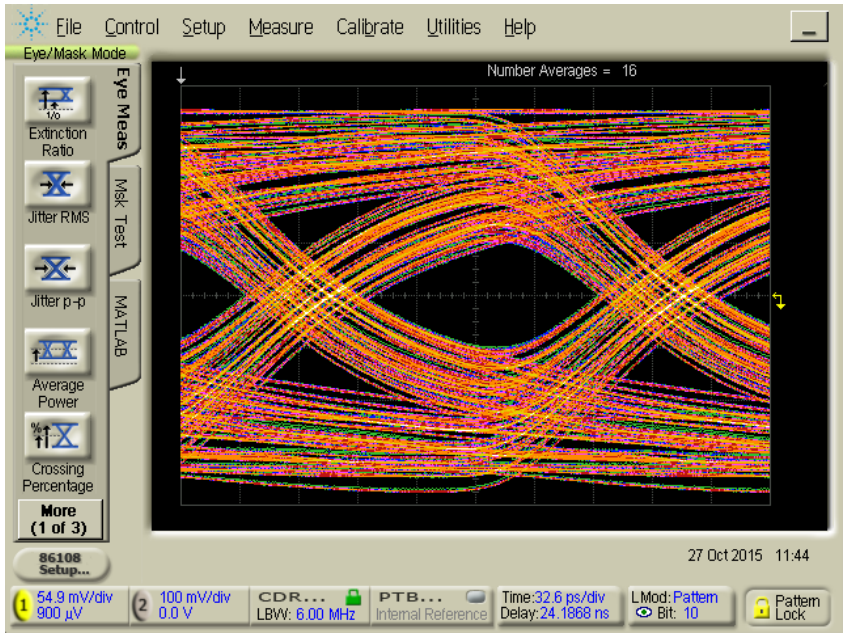


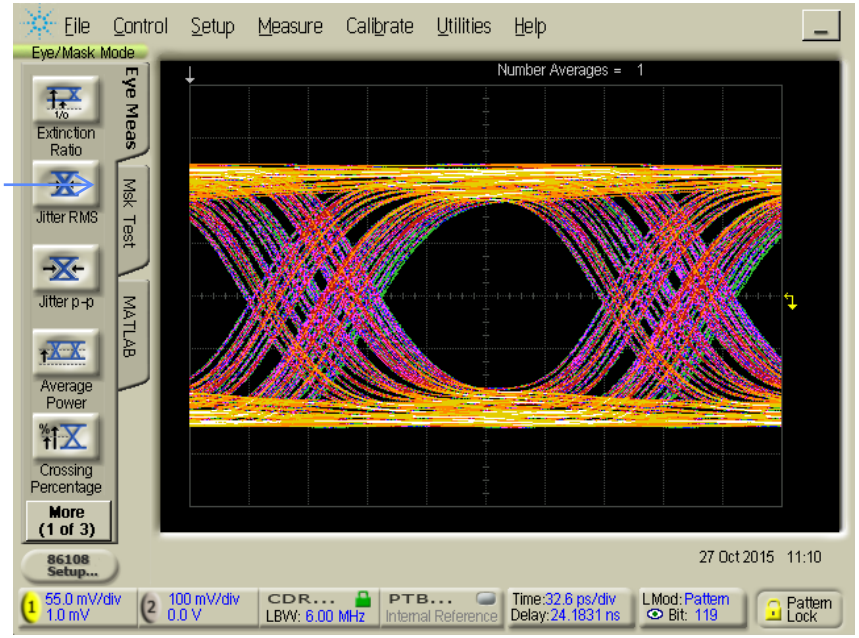


Signal Integrity with "Ideal" TX

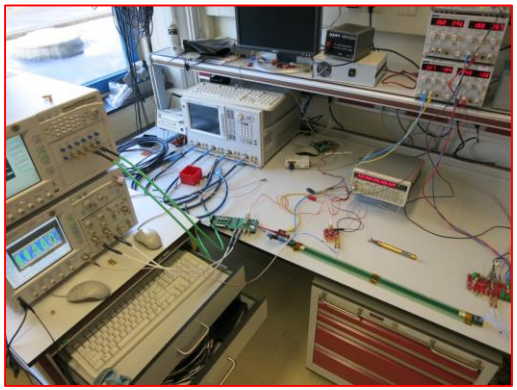






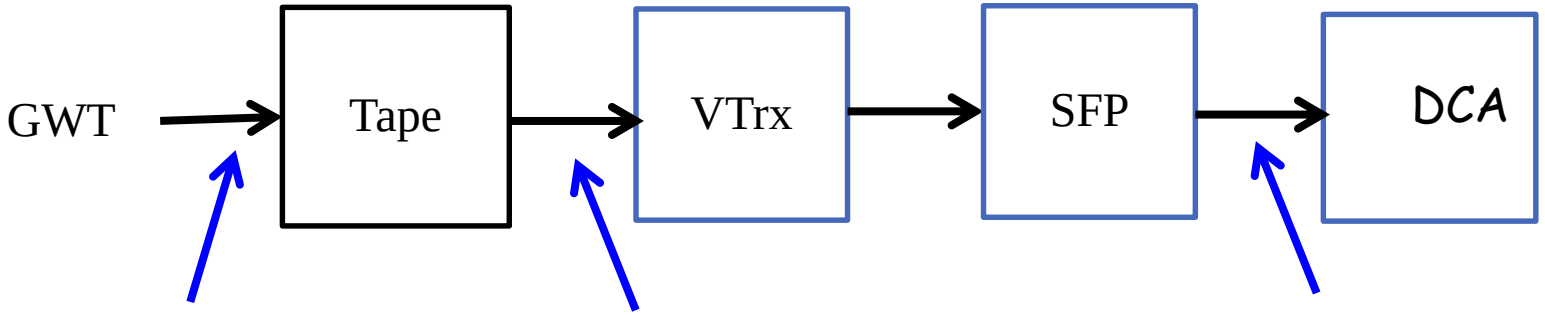


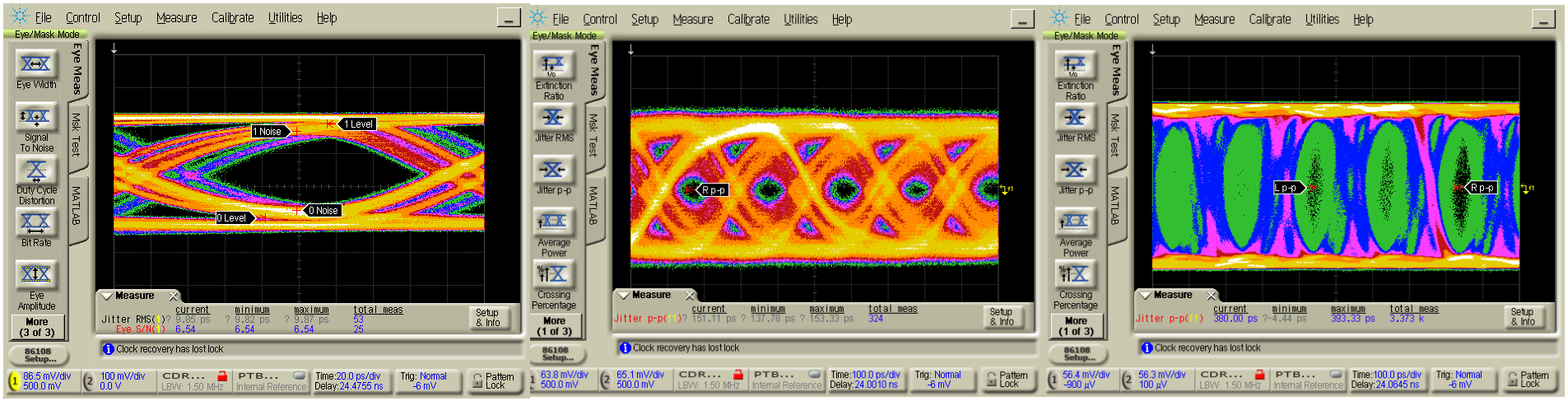
Signal Integrity with GWT TX



shows how careful you have to be with signal transmission if you are to avoid nasty surprises

Can be cured with a Continuous Time Linear Equalizer (CTLE), a peaking amplifier with a frequency slope inverse to that of the channel





Backup