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The CMS Phase-II Time Multiplexed Track Trigger Demonstrator

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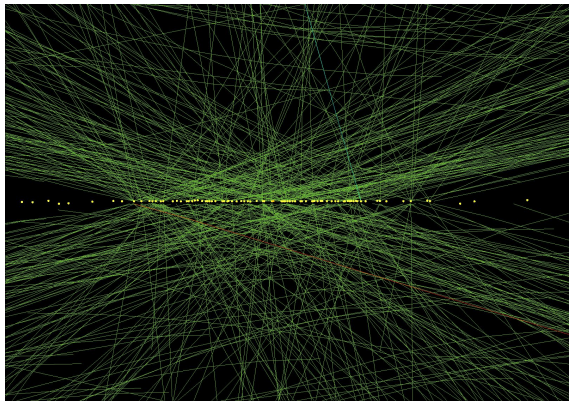
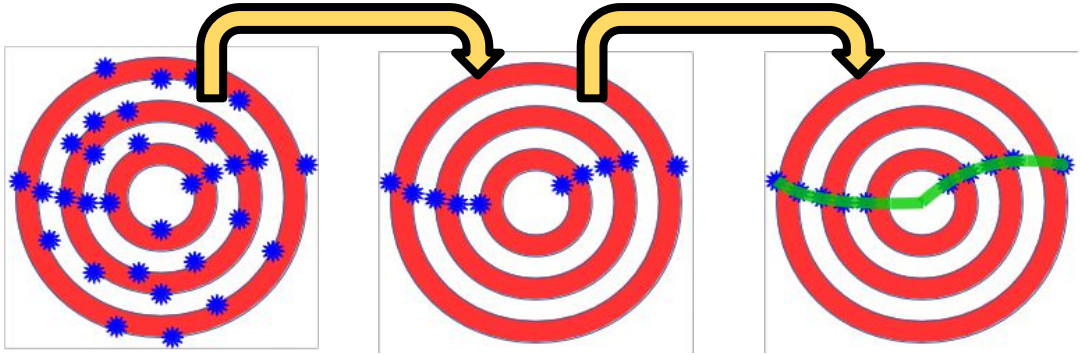
Track Reconstruction at L1

- High-Lumi LHC upgrade → Large pile-up
  - Triggering at Level 1 becomes noisy
  - → enhance trigger algorithms with track information
- Latency budget 12.5μs, bandwidth O(1Tb/s)
  - Need fast electronics to implement parallel processing





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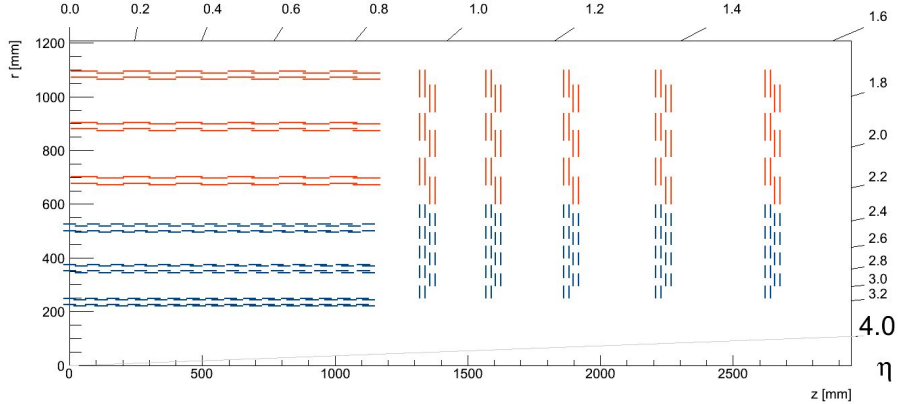
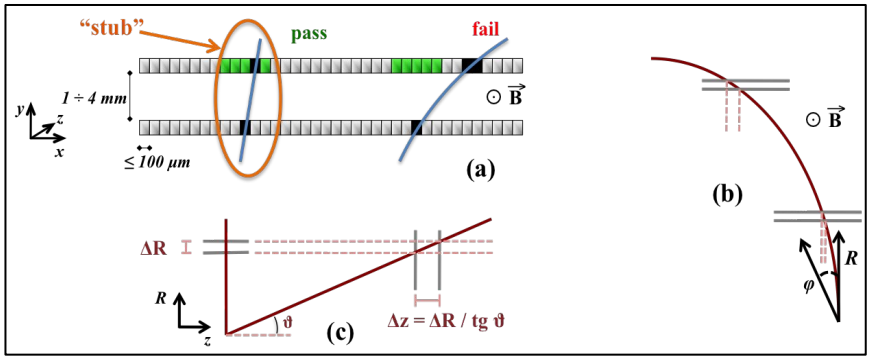
Input from the upgraded tracker

- Double sensor layers
  - 2 Strip layers (2S)
    - Cheaper, less channels
  - 1 Pixel + 1 Strip layer (PS)
    - High flux inner layers



Stub: pair of hits compatible with high pT track



- This arrangement provides an initial filter against combinatoric background
- **CMS chose a cutoff of 3 GeV/c**

Finding tracks in the rφ plane

- Real tracks → Stubs aligned along trajectory
- Relationship between angle & pT in rφ plane

$\varphi_T = \varphi_S - q/p_T * r_T$

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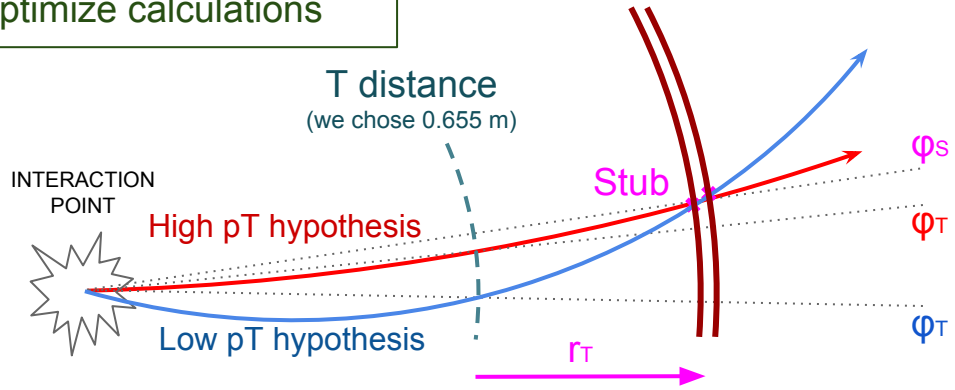
T is a fixed distance chosen to optimize calculations

φ_T = angle of track at radius T

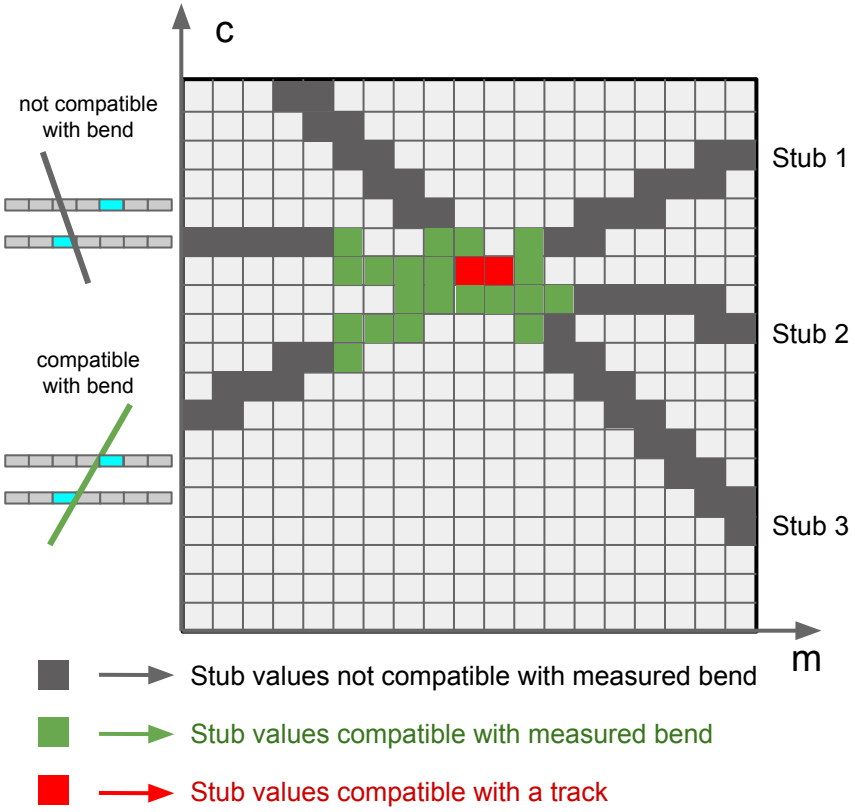
φ_S = angle of stub

r_T = radius difference from T

$c = \varphi_S - m * r_T$



Finding tracks in the rφ plane



Bend filter

- Consider only (c,m) values compatible with observed stub

Track finding

- Fill a histogram in (c,m) plane
  - Each stub represented by a line
  - Bin content is #layers with valid (c, m) values in the specific bin
- Bin content > 4 → Track found

Fake tracks & misassigned stubs

- The r-φ HT has a high identification efficiency, BUT:
  - Many stubs are misassigned to tracks they don't belong to
    - Mis-assigned stubs explode the χ^2 of the track fit
  - In dense environments (jets), HT histogram occupancy is high
    - Artifacts can be identified as tracks ("fake tracks")

- Fake tracks → Degrade downstream algorithms
- Misassigned stubs → Track fit may not converge

- It is <u>fundamental</u> to apply post-HT filters (more later...)

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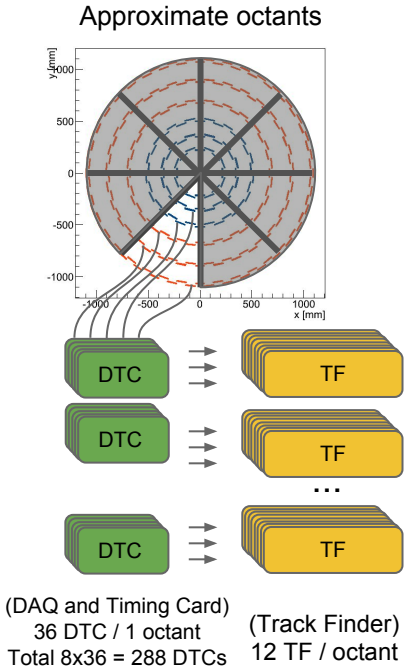
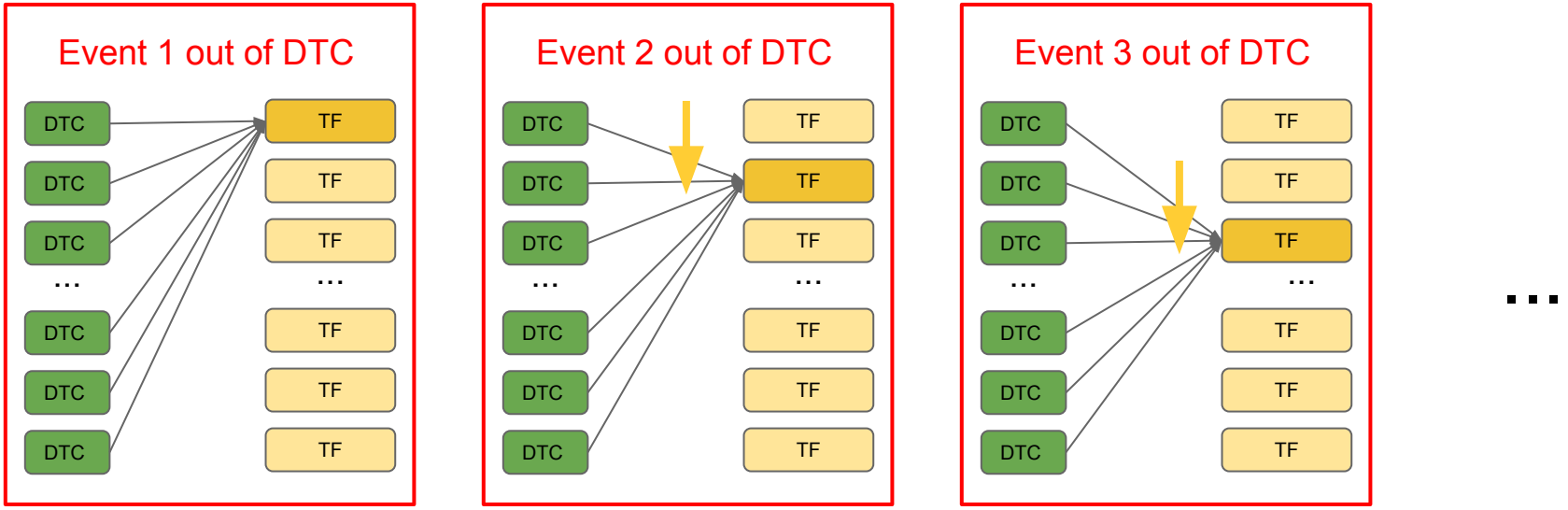
Final system architecture



- Tracker is roughly divided in octants
- Each octant is read out by 36 DTCs
  - "DAQ and Timing Cards"
  - Total: 288 DTCs
  - 2 output links per DTC @ 12Gbps
- The 36x2 links are fanned out to TF cards
  - "Track Finder Cards" read all 72 links
  - They process only stubs assigned to them
  - Stubs assigned to cards in a round-robin fashion (Time Multiplex)

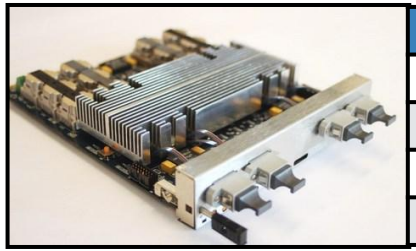
Time Multiplexing

- Processing time of an event > interval between events
  - Use more processing pipelines running in parallel
  - This rolling assignment gives TF enough time to complete events

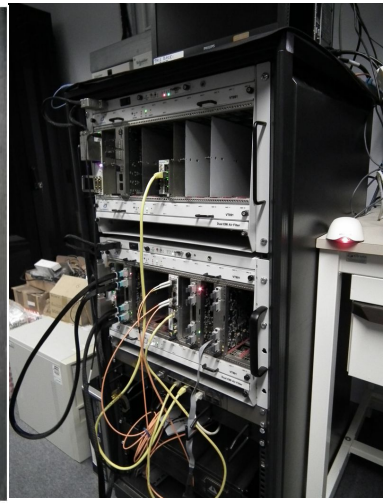


Demonstrator testbenches

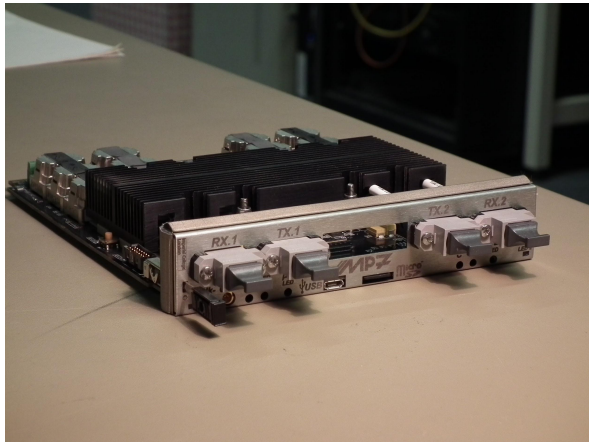
- Each processor functionality will be demonstrated using MP7 boards
- Two µTCA crates are used for our demonstrator (RAL & CERN)
- Communication with boards via mp7butler software

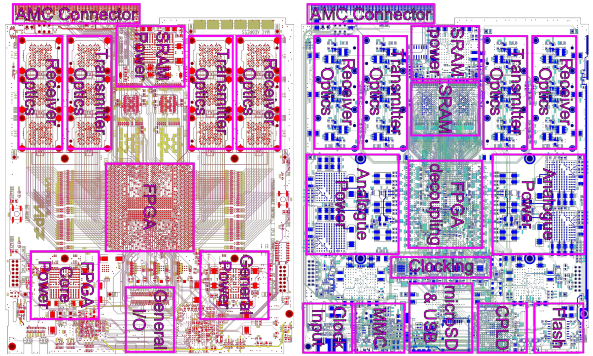


µTCA MP7
FPGA Virtex 7
72 I/O links
12.5 Gbps/link
Tot. bandwidth ~1 Tbps



The MP7 processing card





- XilinX Virtex-7 XC7VX690T (80 GTH links)
  - Available: 72 optical links @ 12.5Gbps
- Used for CMS Phase-I calo trig upgrade
  - Well-tested hw and sw
- The MP7 cannot fit the whole track finder
  - We use it as a demonstration platform
  - Future FPGAs → higher performance
- Demonstrator: split functions across MP7s
  - Geometrical Processor (MP1)
  - HT track finder (MP2)
  - Track filtering (MP3)
  - Helix trajectory fitter (MP4)

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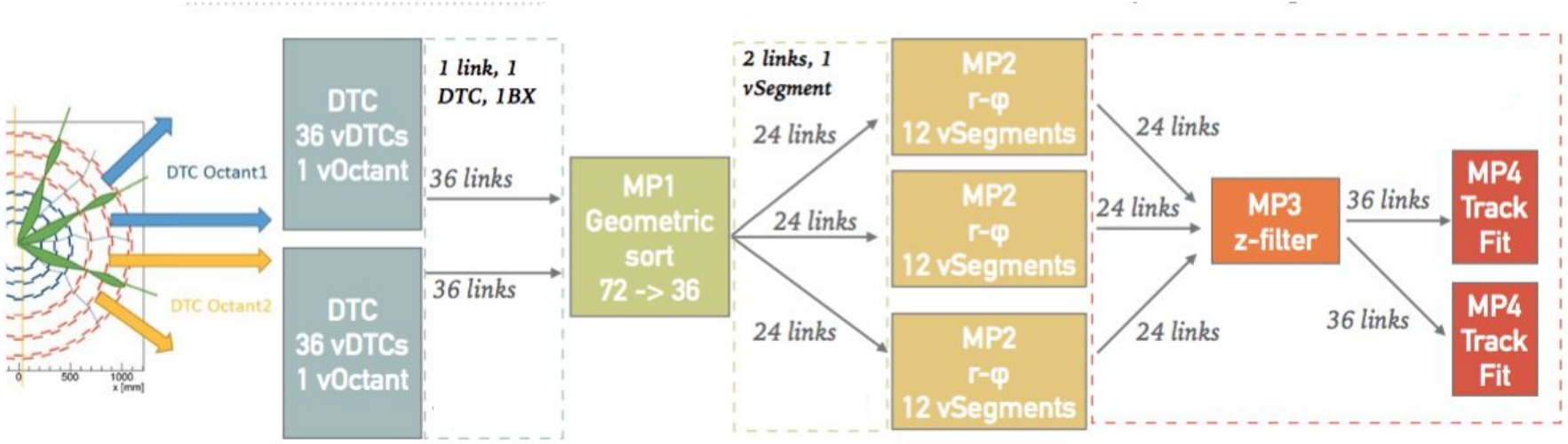
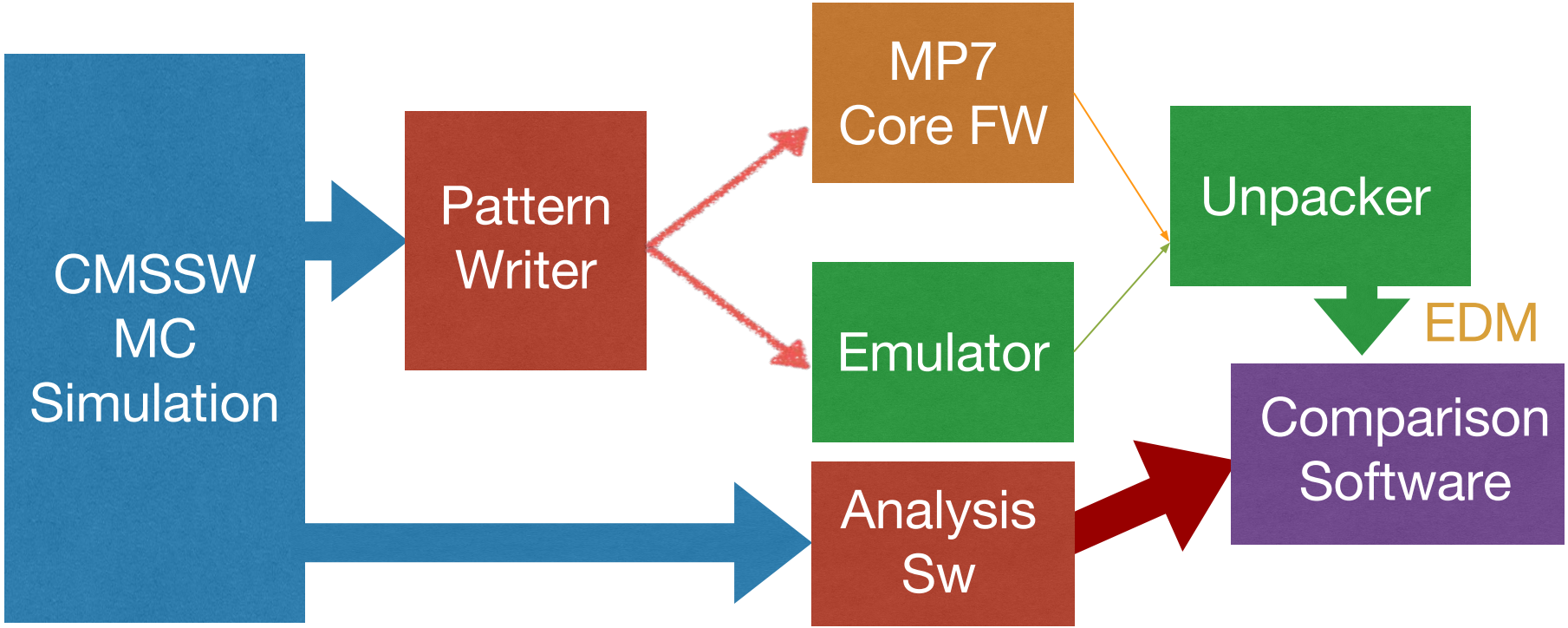
Demonstrator layout

- For the CMS review we will demonstrate in hardware the functionality of two neighbour φ-octants



Software infrastructure



Firmware State of the Art

- All needed fw (except Track Fit) have been developed and tested in simulation
- **GP & HT** fw have been already implemented in the **MP7 infra**
  - GP sorting has been validated with simple patterns (no coord. conversion)
  - HT fw validated using upgraded geometry simulated dataset
- vDTC ready in few weeks (data sorting)
- Track Filter fw tested in simulation
- Track Fitter fw under development

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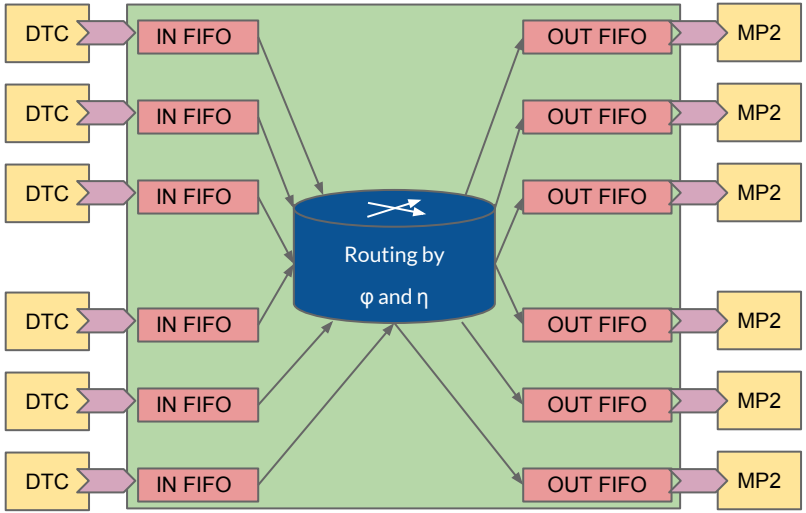
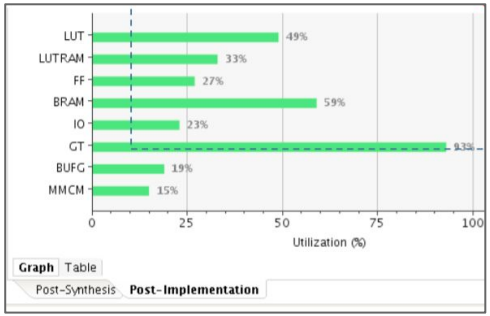
Geometric Processor (MP1)

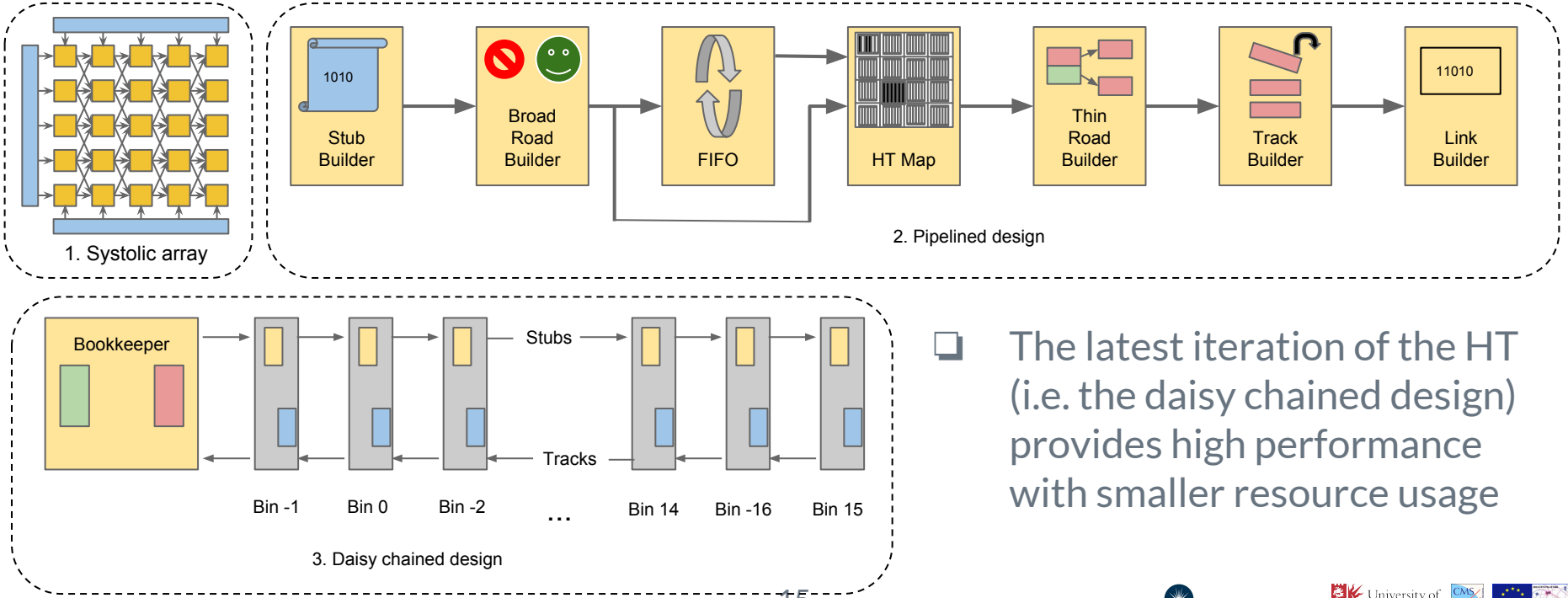


- The cabling of the tracker does not correspond to the optimal segmentation in φ and η for HT
- Furthermore, latency is reduced by splitting an event across multiple cards
- The Geometric Processor sorts stubs in φ and η and sends them to the correct track finder
- Being developed by Fionn Ball @ University of Bristol



Track Finder Processor (MP2)

- Finds tracks using a Hough Transform (3 proposed implementations)



- The latest iteration of the HT (i.e. the daisy chained design) provides high performance with smaller resource usage

HT implementations

- Systolic Array: backup
  - Two dimensional structure (c x m cells)
  - Stubs propagating from cell to cell
  - One HT array for all Φ sector in a chip
- Pipeline
  - One dimensional structure (m bins)
  - Fanout from one input to all bins
  - One HT per Φ sector, several HT arrays in a single chip
- Daisy chain
  - One dimensional structure (m bins)
  - Stubs propagate from bin to bin
  - One HT per Φ sector, several HT arrays in a single chip

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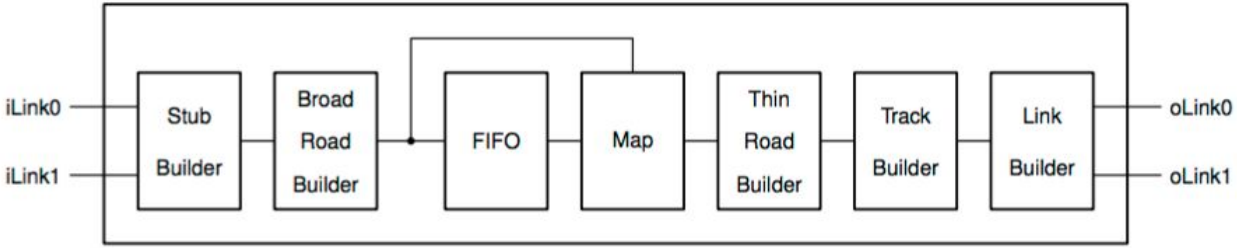
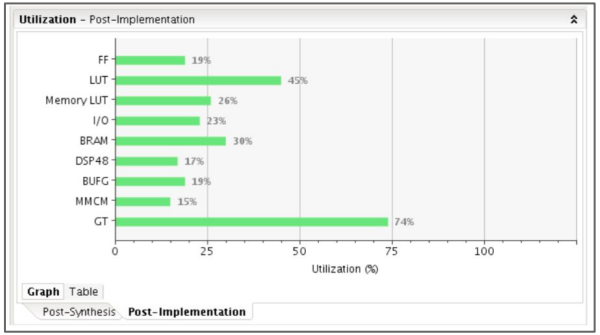
Pipeline





- 32x32 HT array, up to 12 segments in a single chip
- Stub Builder deliver one stub per clock
- Road Builder deliver 32 (m, c) pairs plus stub per clock
- FIFO delays these roads
- Map uses roads to count the number of layers for each cell to check the track condition
- Track Builder delivers one track stub per clock
- Link Builder splits them over to links

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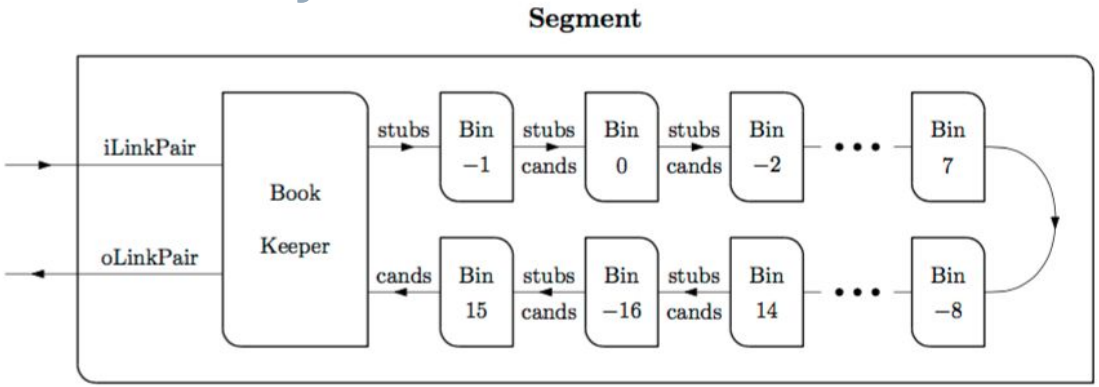
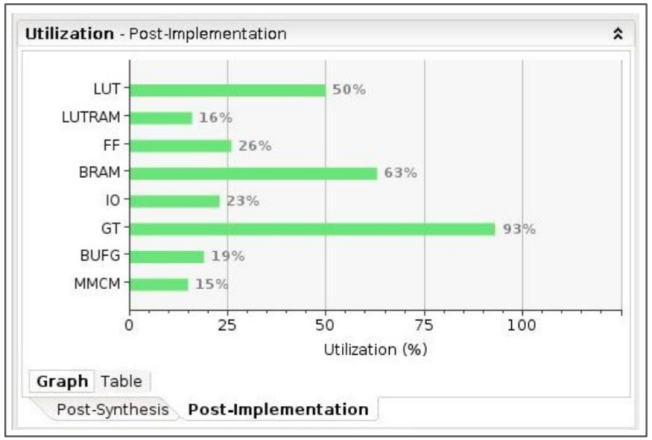
Daisy Chain

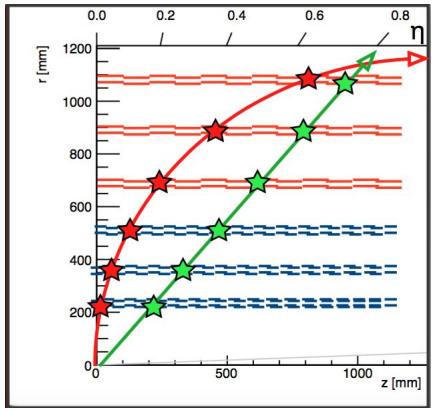




- 32x32 HT array, up to 18 segments in a single chip
- Duplication along c only in the necessary m bins (BRAM)
- Stubs propagate from m bin to m bin (High pT bin first)
- Less DRAMs (better balance), no DSP & lower latency
- Latency depends on # of input stubs per sector and the amount (and distribution) of stub duplication

Filtering tracks in the rz plane

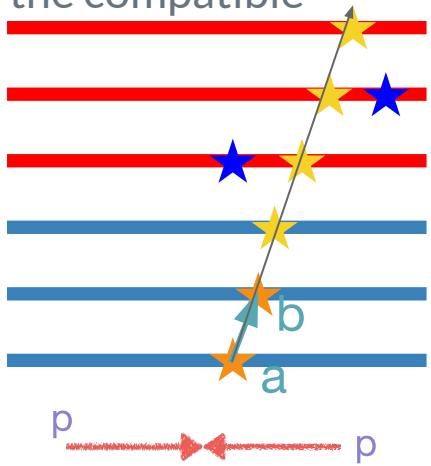
- Exploiting only rφ coordinates of stubs, after HT we still cope with a big amount of fake candidate tracks (~55% in ttbar+PU140 events)
- Solution: apply a track filter stage after the HT to each candidate track (cell in the HT)
  - Eta filter
  - z_R Filter
  - rz Hough Transform
  - Seed Filter



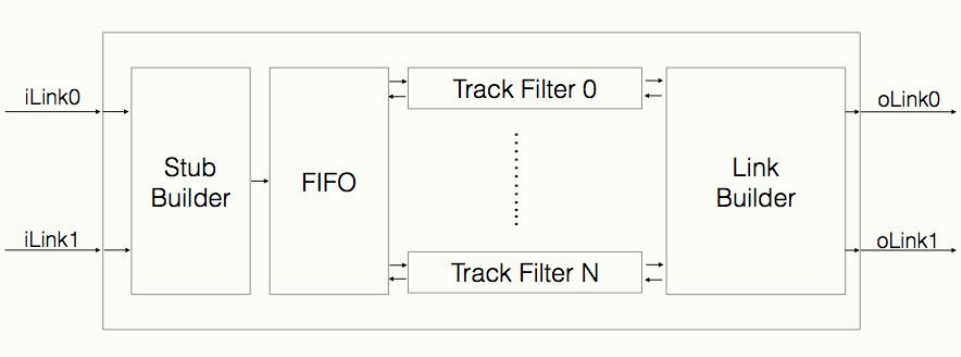
Seed Filter

Tracklet-like approach

a. Take two stubs in the innermost layers, belonging to PS modules
b. Draw a line (Seed) in the rz plane using the two seeding stubs
c. Check if seed is compatible with beamspot and eta sector
d. If yes, check if other stubs are compatible with the seeding line
e. If the seed has at least 5 stubs in 5 different layers, keep all the compatible stubs
f. Loop over all the possible seeding stub combinations
g. Keep all the stubs belonging to “good” seeds (No dups)



Seed Filter Implementation (MP3)



Utilization – Post-Implementation

Resource	Utilization	Available	Utilization %
LUT	12350	433200	2.85
LUTRAM	3081	174200	1.77
FF	15543	866400	1.79
BRAM	31	1470	2.11
DSP	130	3600	3.61

Graph | **Table**

Post-Synthesis | **Post-Implementation**

- Pipelined structure, one filter per ηΦ segment
- Each segment processes N tracks in parallel (N=10 implemented)
- Seed parameters calculated via DSPs
- S seeds are calculated at the same time per each track (S=10 implemented)
- Firmware tested in simulation, currently being implemented on the MP7

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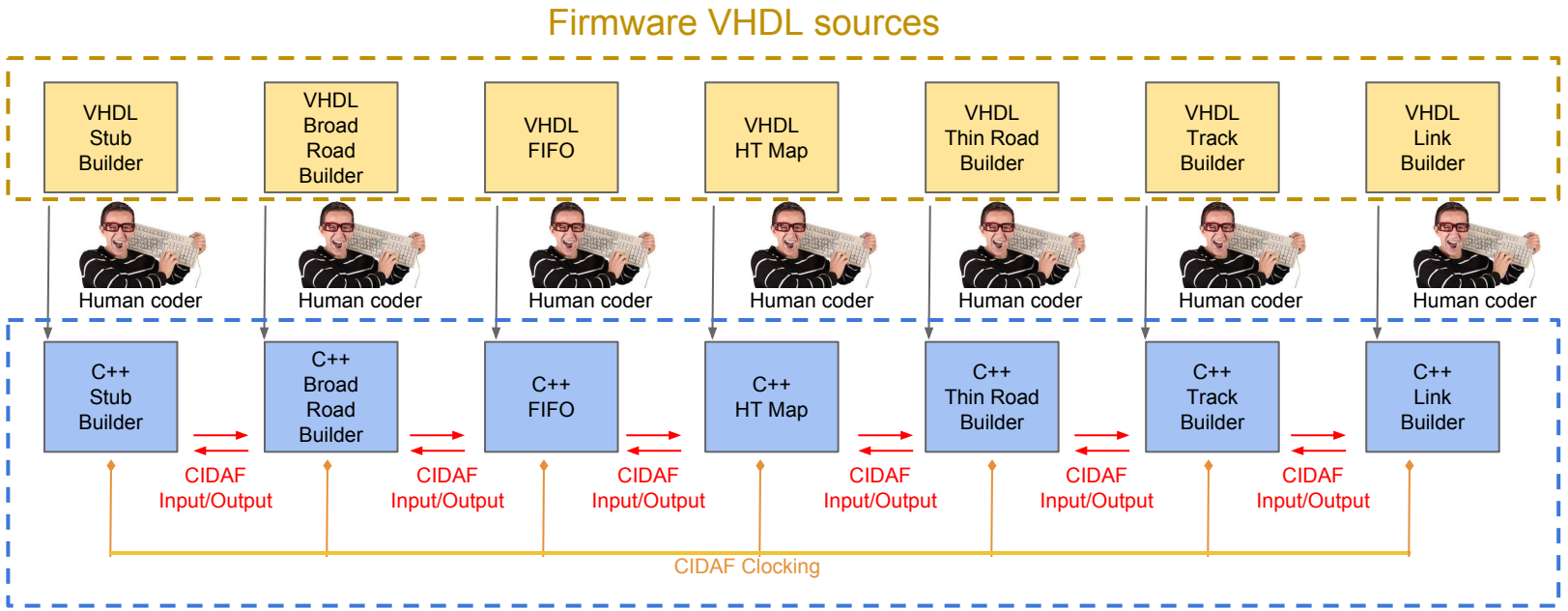
Software emulation in CIDAF

- CIDAF emulation framework developed to establish common interfaces when writing the emulators for the different proposed firmwares.

Example: Pipelined HT 2-cbin version



Emulation of the Track Finder

- Emulations for the pipelined 2-cbin and 1-cbin HT ready
  - Bugs need fix, but right now not a priority as the fw may not be used
- Currently writing the emulation for the daisy chain HT
  - The simple structure of this firmware is easier → progressing fast
- The emulator for the Geometric Processor is being written using CIDAF by Fionn Ball @ Bristol University
- CIDAF allows plugging component emulators together
  - Full-system emulation foreseen for the future

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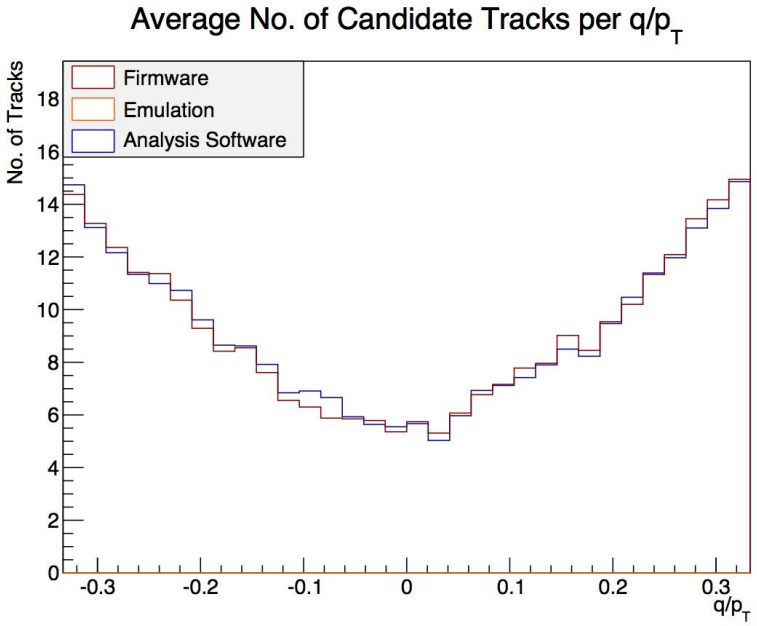
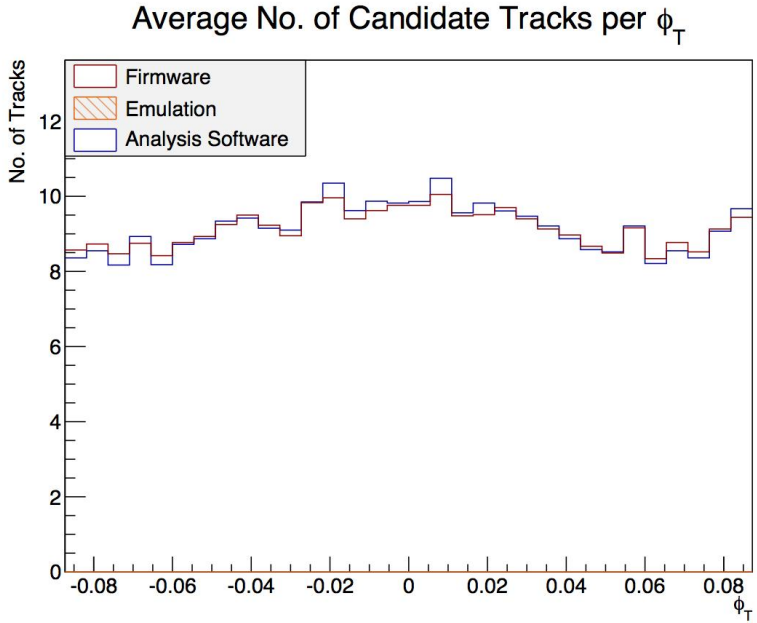
Demonstrator Results

- Pipeline HT firmware has been validated using 100 ttbar+PU140 events against our analysis sw





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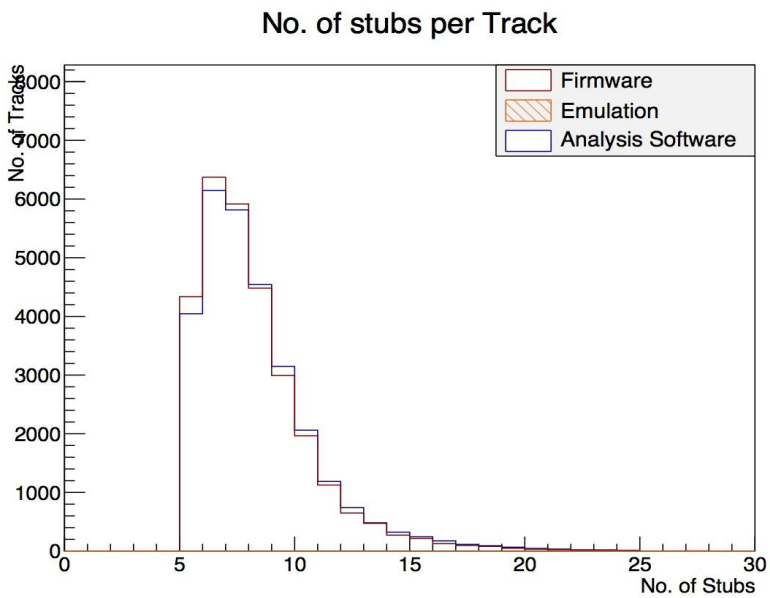
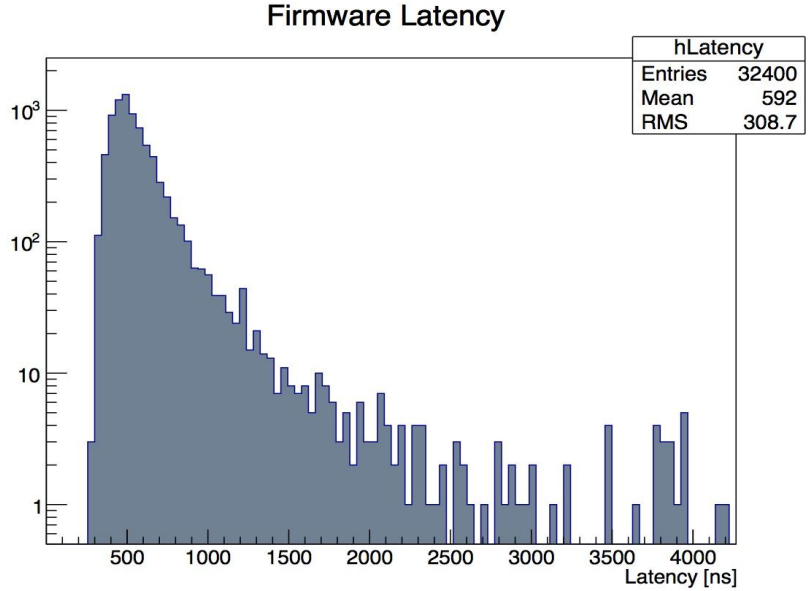
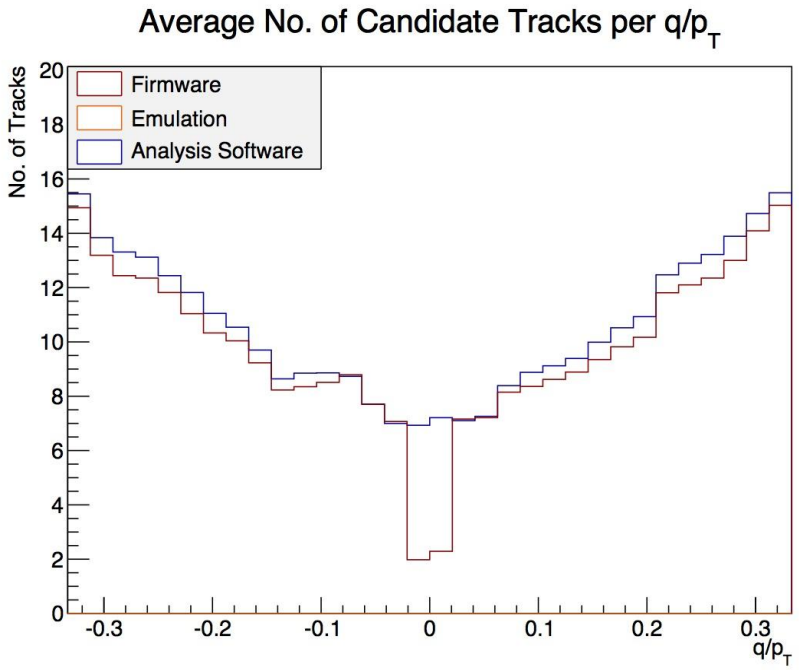
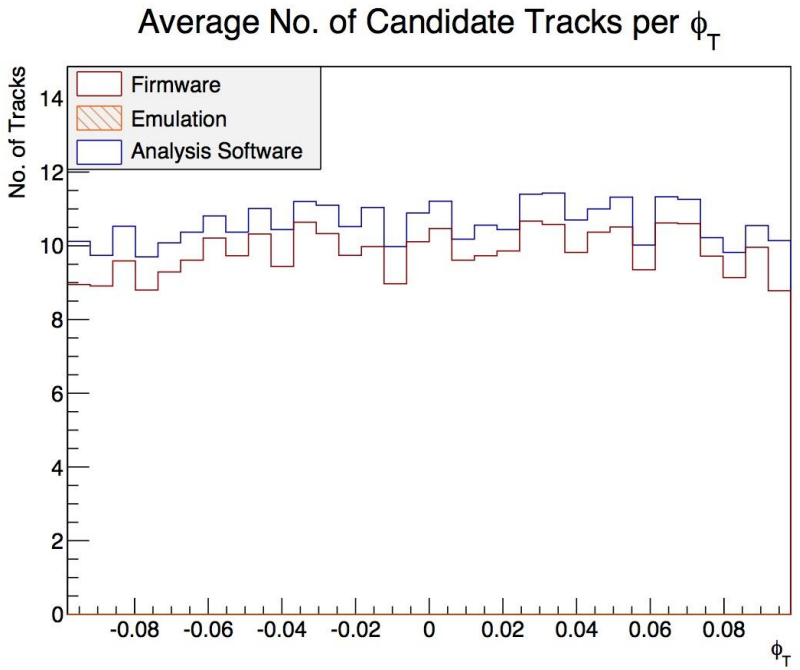




Switching to a Daisy Chain HT

- Preliminary results obtained with 100 ttbar+PU140 events





Summary

- Architecture for a Time Multiplexed Track Trigger has been presented
- Hardware demonstrators, representing a scalable slice of the overall system, are installed both at RAL & CERN
- First hardware results from the track finder processor show good agreement with our C++ simulation (99.8% pipelined, 93% DaisyChain)
- DTC/GP/TrackFilter fw under validation
- Track Fitter under study

Future Plans

- Short Term (CMS L1 midterm review, May 2016)
  - Demonstrate in hardware a partial TMTT chain (DTC => MP2)
  - Currently building the system at CERN, connecting MP7s through optical links
  - Migrate to the DaisyChain Hough Transform implementation
- Long Term (CMS L1 final review, December 2016)
  - Validate individually against emulator/analysis sw individual processor functionalities
  - Demonstrate in hardware the full chain (DTC => MP4)

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