Configuration of the Operation Modes for LHCbs Scintillating Fibers at LPNHE

T Sierra-Polanco [1] C.E.Vera[2] D. Milanés[3]

[1]Universidad de Ibagué, [2]Universidad del Tolima y [3]Universidad Nacional de Colombia

[1]tomas.sierra@unibague.edu.co, [2]cvera@ut.edu.co, [3]diego.milanes@cern.ch

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Outline

Introduction

This particle detection project has the purpose of getting a higher data rate in the acquisition by using VHDL code configuration for FPGA boards due to the new luminosity levels for the LS2 (Long Shutdown 2).

Parameter	**RUN1**	**RUN2**	**RUN3**
Period	$2010 - 2013$	$2015 - 2018$	2019 onwards
Center-of-Mass Energy	$7TeV - 8TeV$	$13TeV$	$14TeV$
Sampling Frequency	$1MHz$	$1MHz$	$40MHz$
Instantaneous Luminosity	$4 \times 10^{32} cm^{-2} s^{-1}$	$4 \times 10^{32} cm^{-2} s^{-1}$	$2 \times 10^{33} cm^{-2} s^{-1}$
Integrated Luminosity	$\sim 3, 2 fb^{-1}$	$8 fb^{-1}$ expected	$50 fb^{-1}$ expected

Table: Parameter Comparison Between RUNs

LHCb Sub Detectors

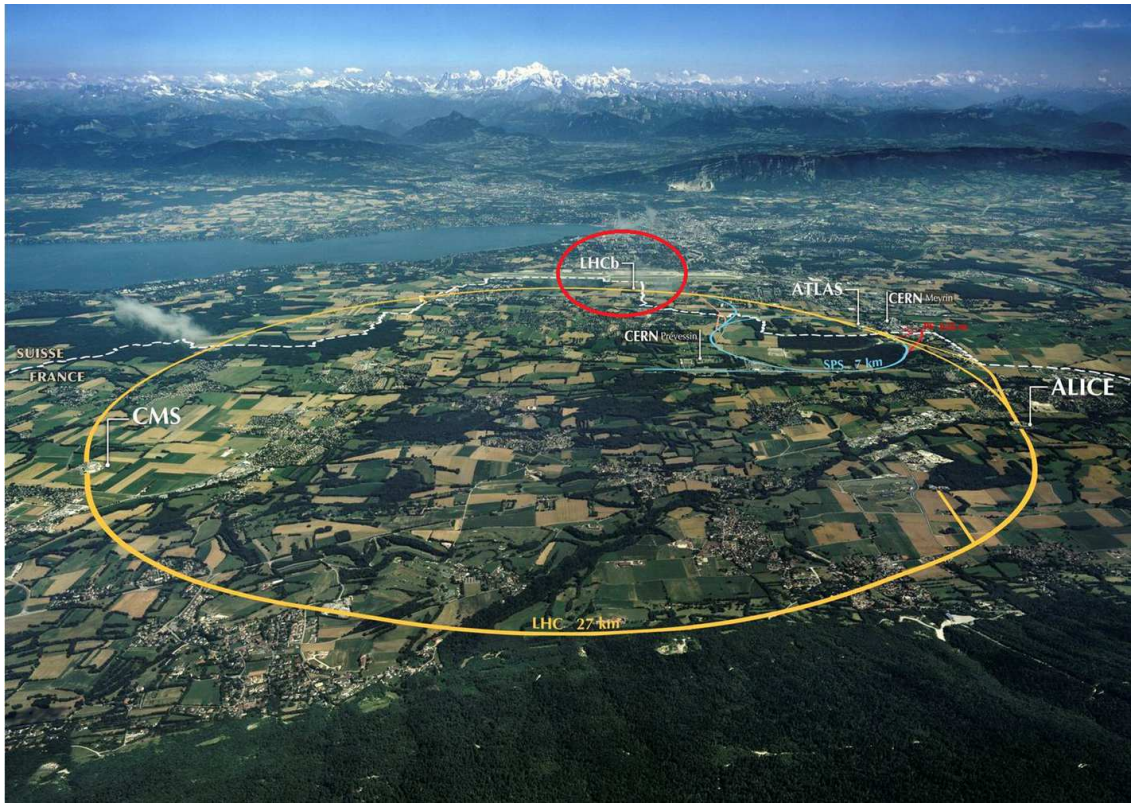

Figure: CERN

LHCb Sub Detectors

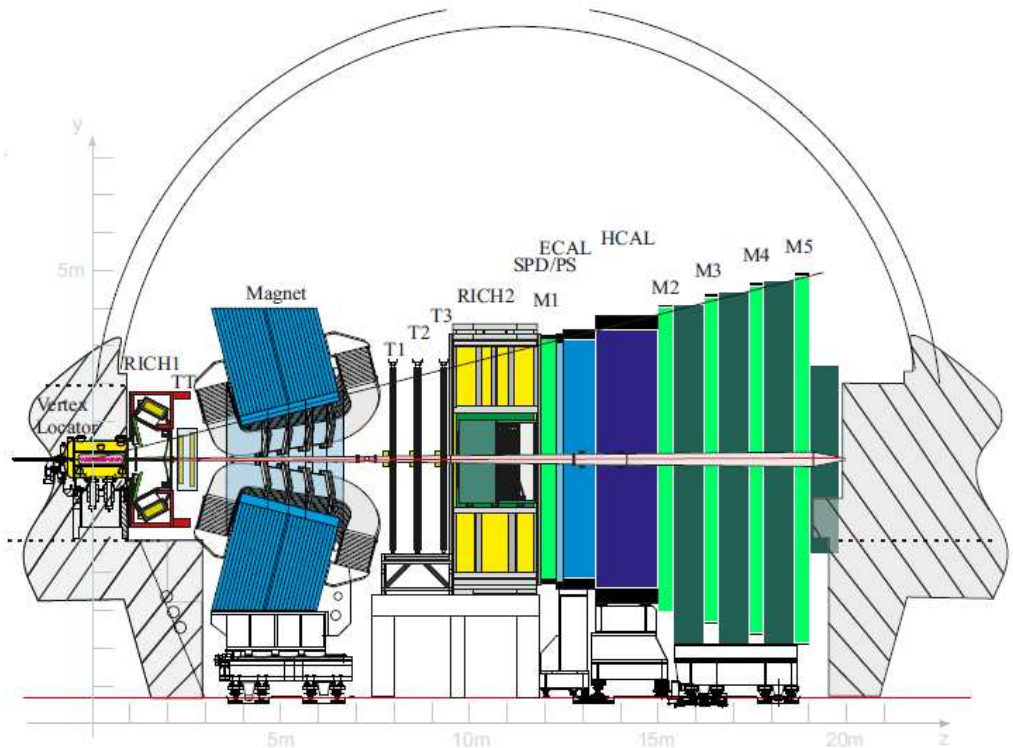

Figure: Schematic View of the Current LHCb Detector

LHCb Sub Detectors

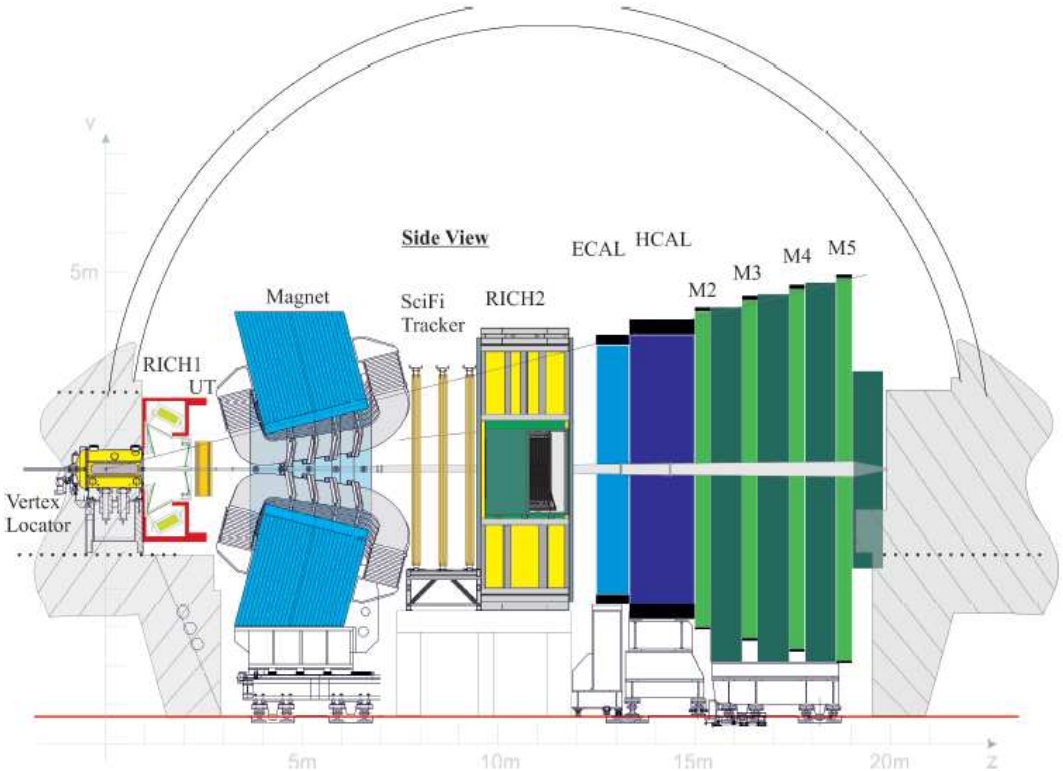

Figure: Schematic View of the LHCb Upgrade Detector

Scintillating Fibers (SciFi)

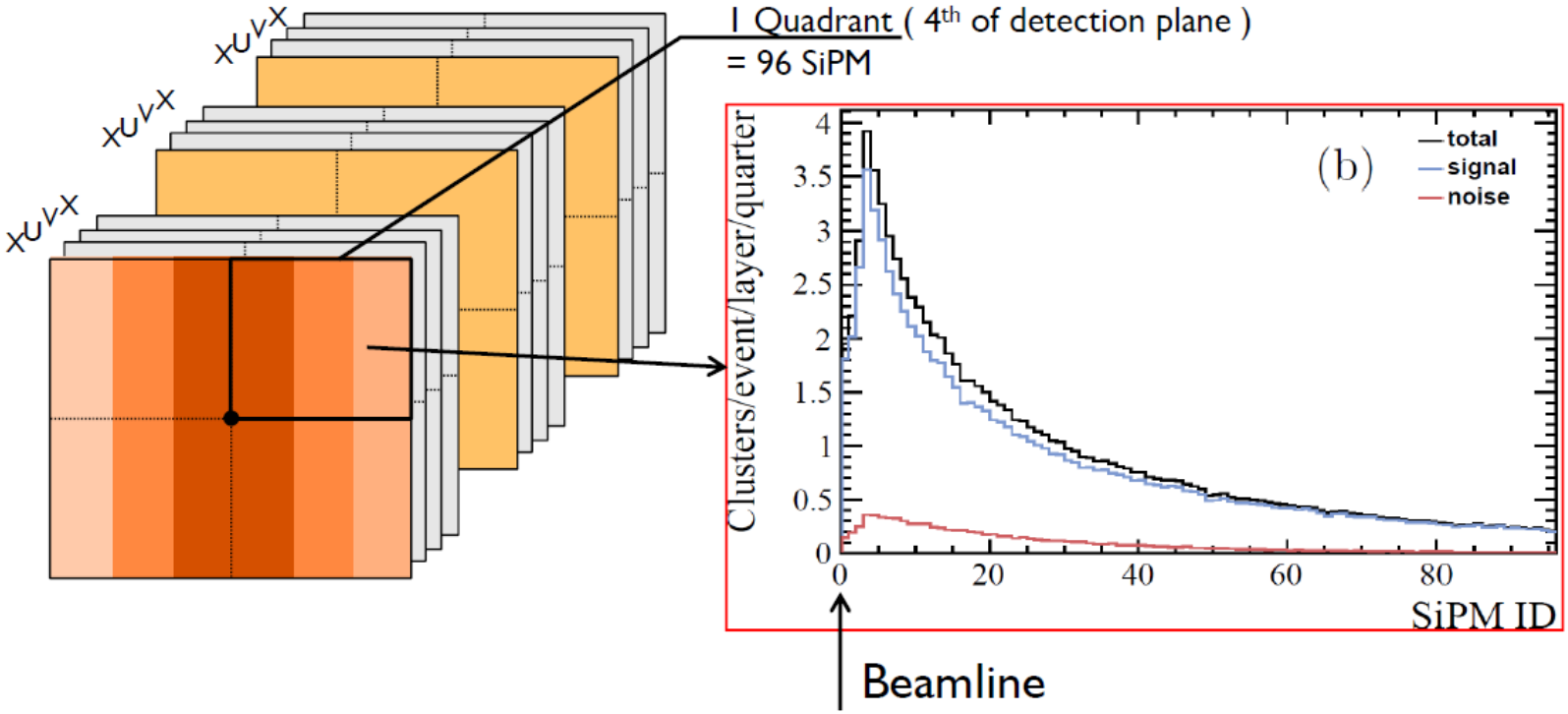

Figure: Scintillating Fibers (SciFi)

Scintillating Fibers (SciFi)

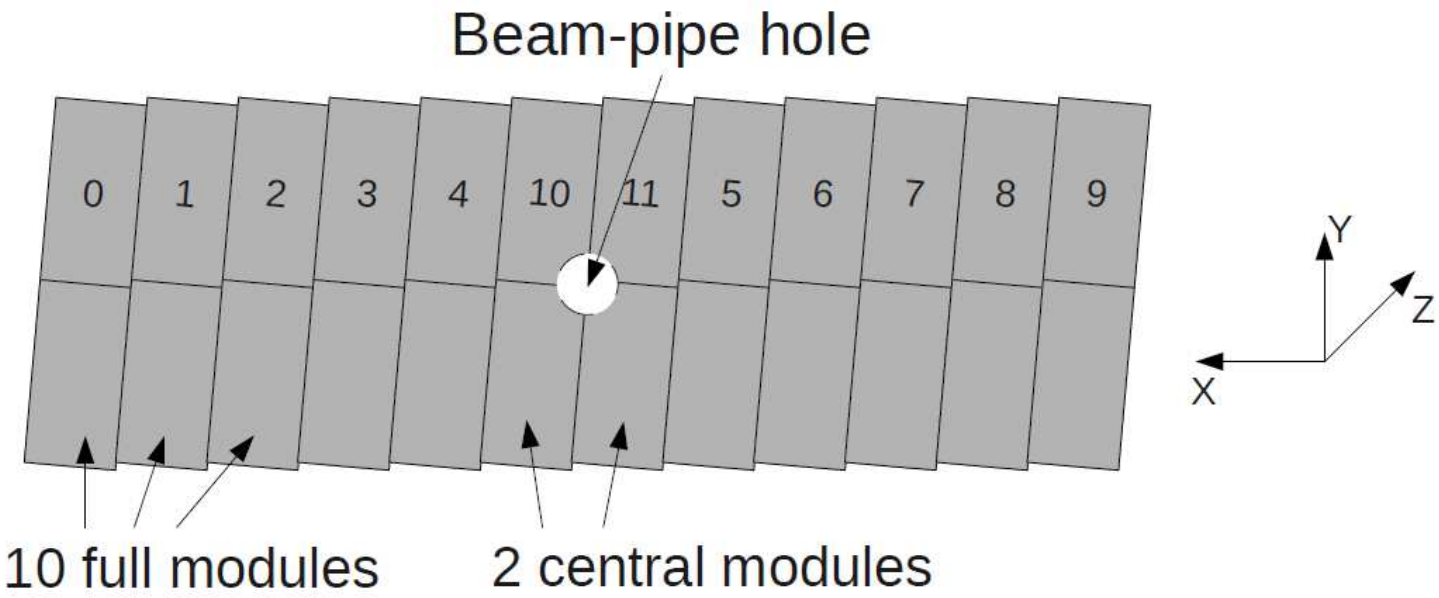

Figure: Layer Detection Structure

Scintillating Fibers (SciFi)

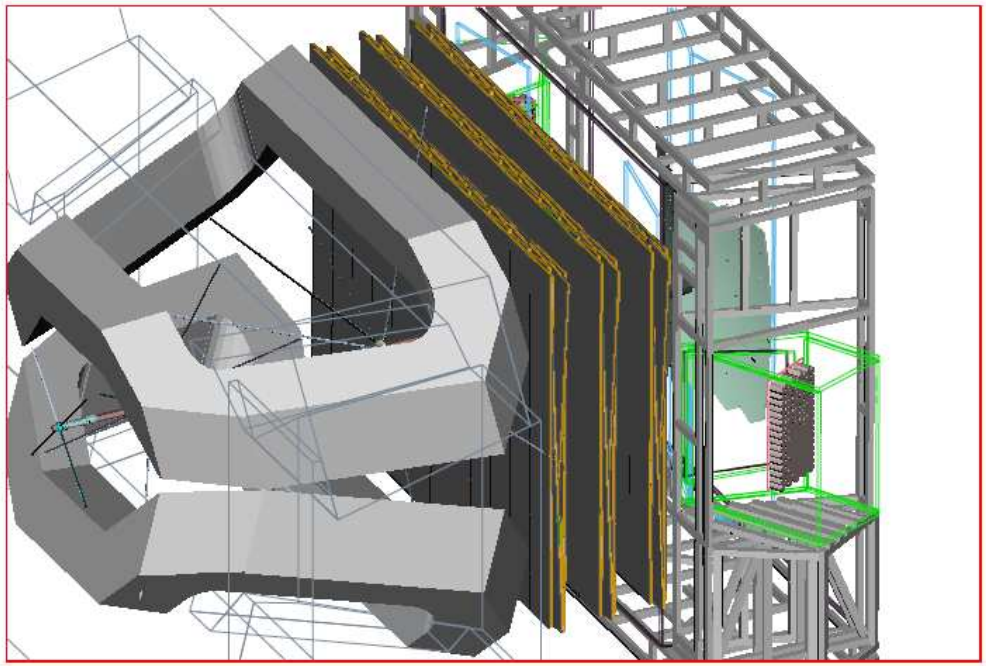

Figure: SciFi Location Between the Magnet and the RICH

Scintillating Fibers (SciFi)

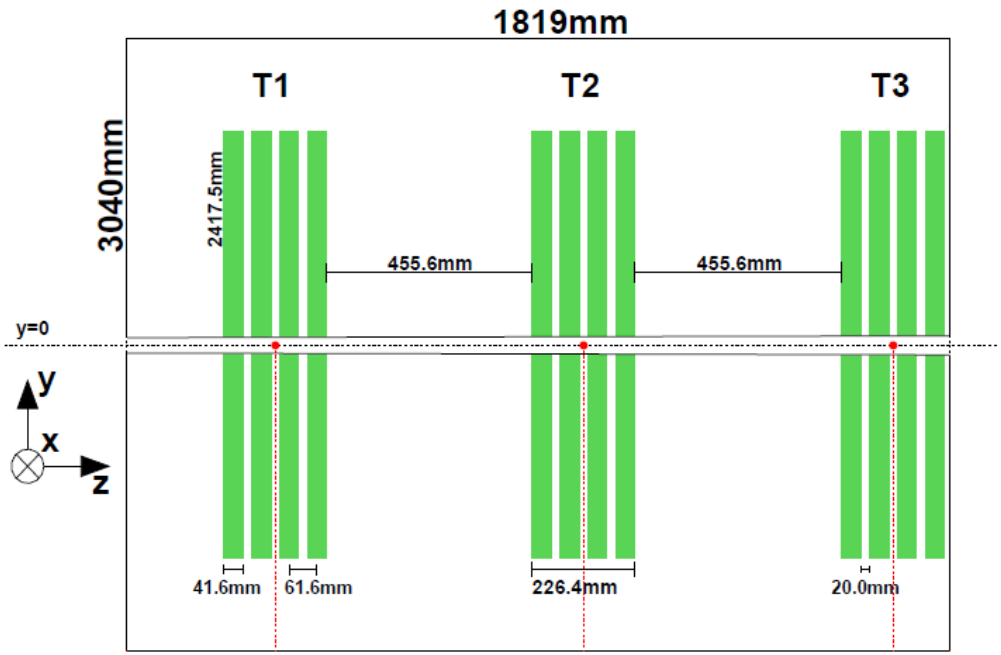

Figure: SciFi Side Disposition

Scintillating Fibers (SciFi)

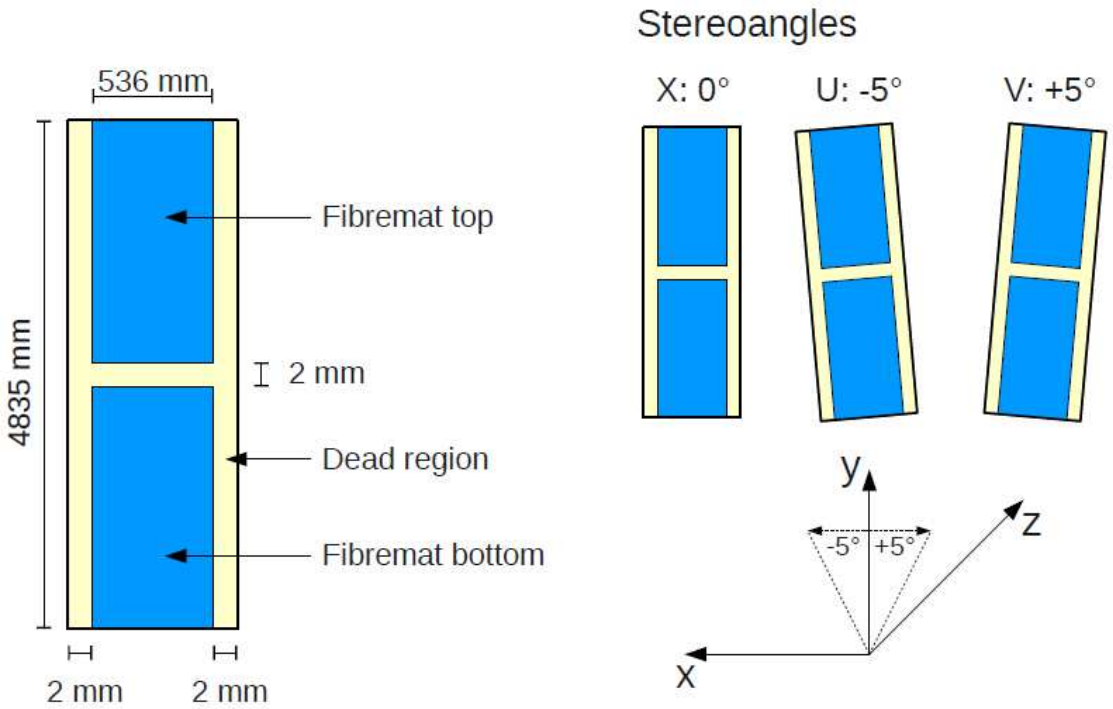

Figure: Stereo Angles

Digital Electronics

- MiniDAQ
  - FE (Front End)
  - BE (Back End)
  - GBT (GygaBitTransceiver)
- VHDL
  - VHSIC (Very High Speed Integrated Circuit)
  - HDL (Hardware Description Language)
- FPGA (Field Programmable Gate Array)
  - Stratix V GX
- GIT and FORGE Deposit

GBT/FE/BE

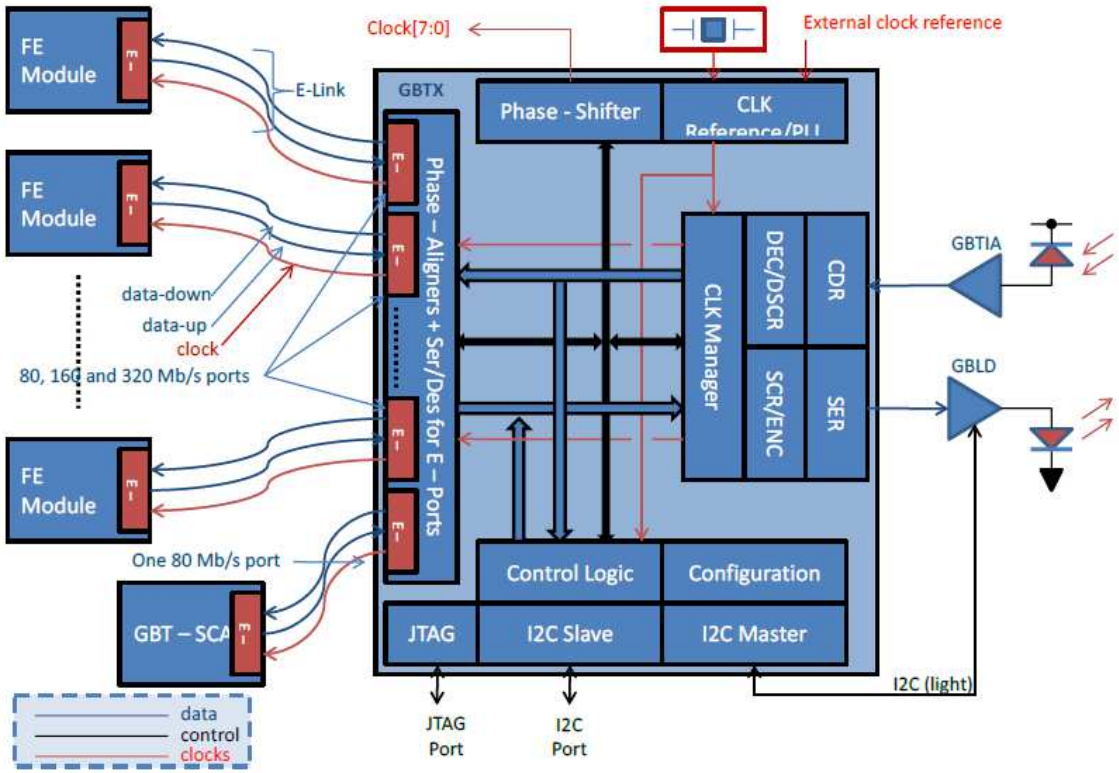

Figure: Gigabit Transceiver

Standard Mode Format

- Header: 4 bits
- Data: 80 bits
- Control: 32 bits (FEC), 4 bits (SC)
- Efficiency: 66%

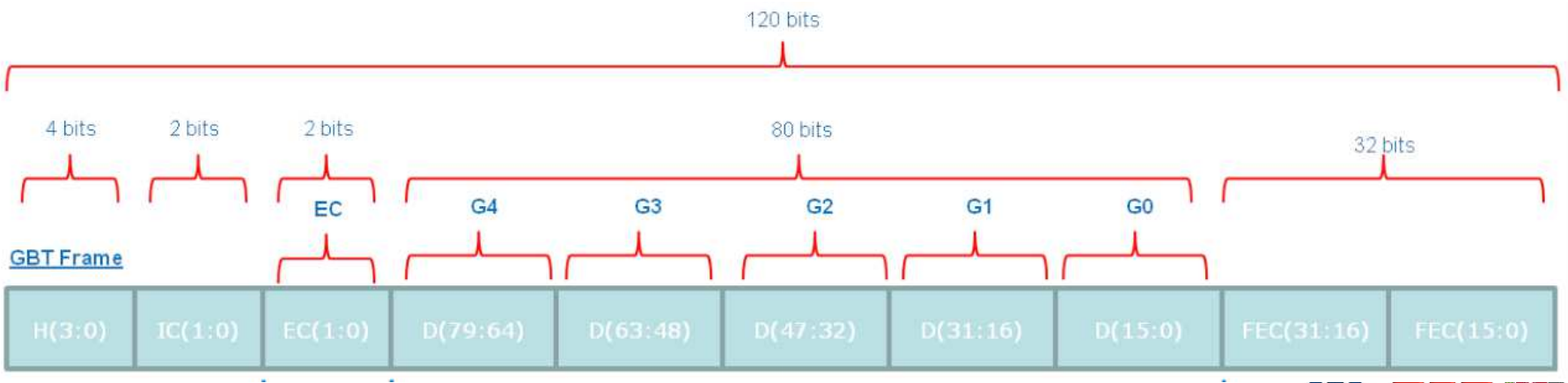

Figure: Standard Mode Frame

Standard Mode Format

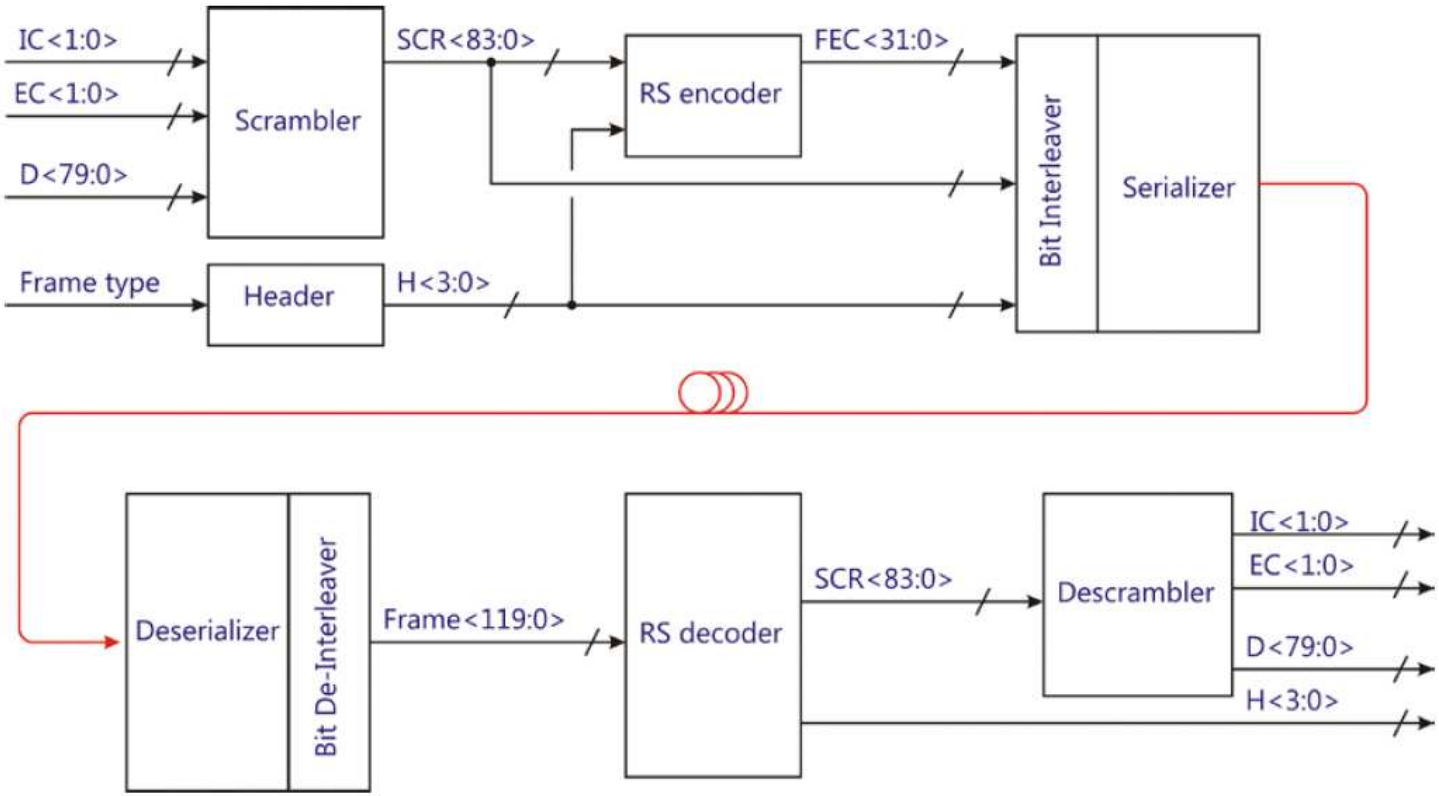

Figure: Standard Mode Block Diagram

Wide Bus Mode Format

- Header: 4 bits
- Data: 112 bits
- Control: 4 bits (SC)
- Efficiency: $93,\bar{3}\%$

Figure: WideBus Mode Frame

Wide Bus Mode Format

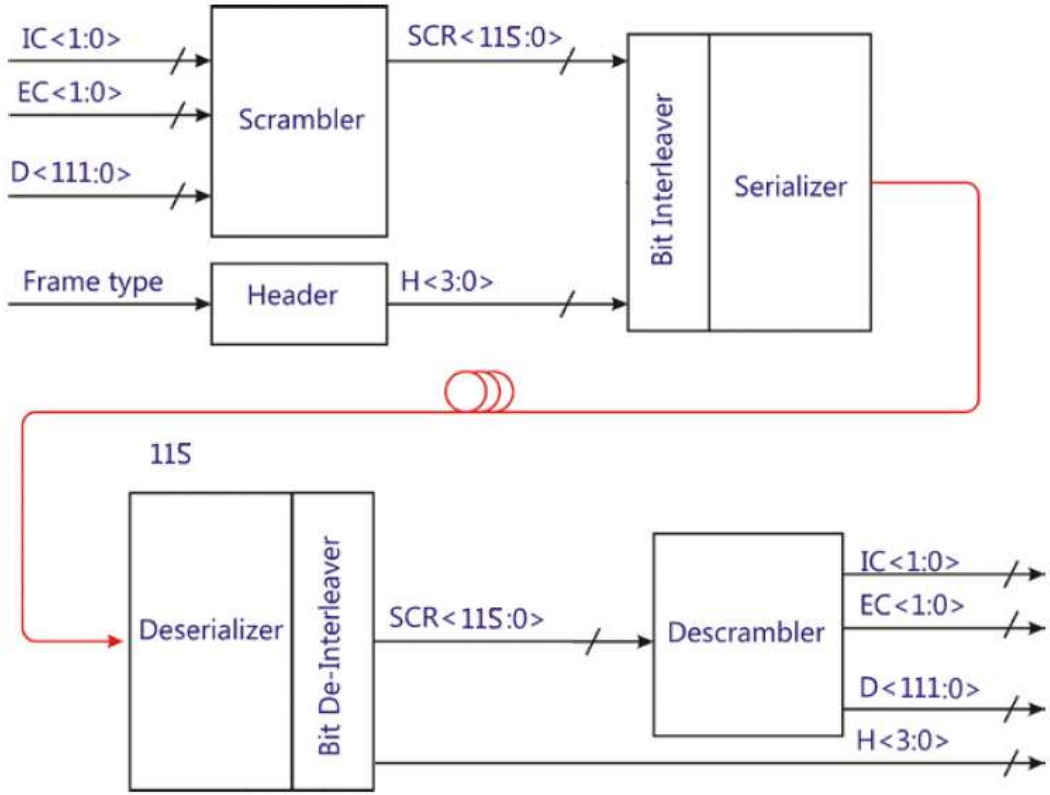

Figure: WideBus Mode Block Diagram

Tasks for LPNHE

- Configure the code for the GBT Link in order to simulate the WideBus Mode and obtain a higher efficiency.
- Change the parameters in the code for the correct simulation of the GBT WideBus Mode.
- Use a test bench to check the simulations proper functioning.

Results

- The operation mode configurations has been made as planned.
- The simulations were run according to the established formats for the code.
- The WideBus configuration collects more data per frame with a less powerful control than the Standard Mode.
- Increase the efficiency in the DAQ from 66% to over $93,\bar{3}\%$.

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!That's all folks!