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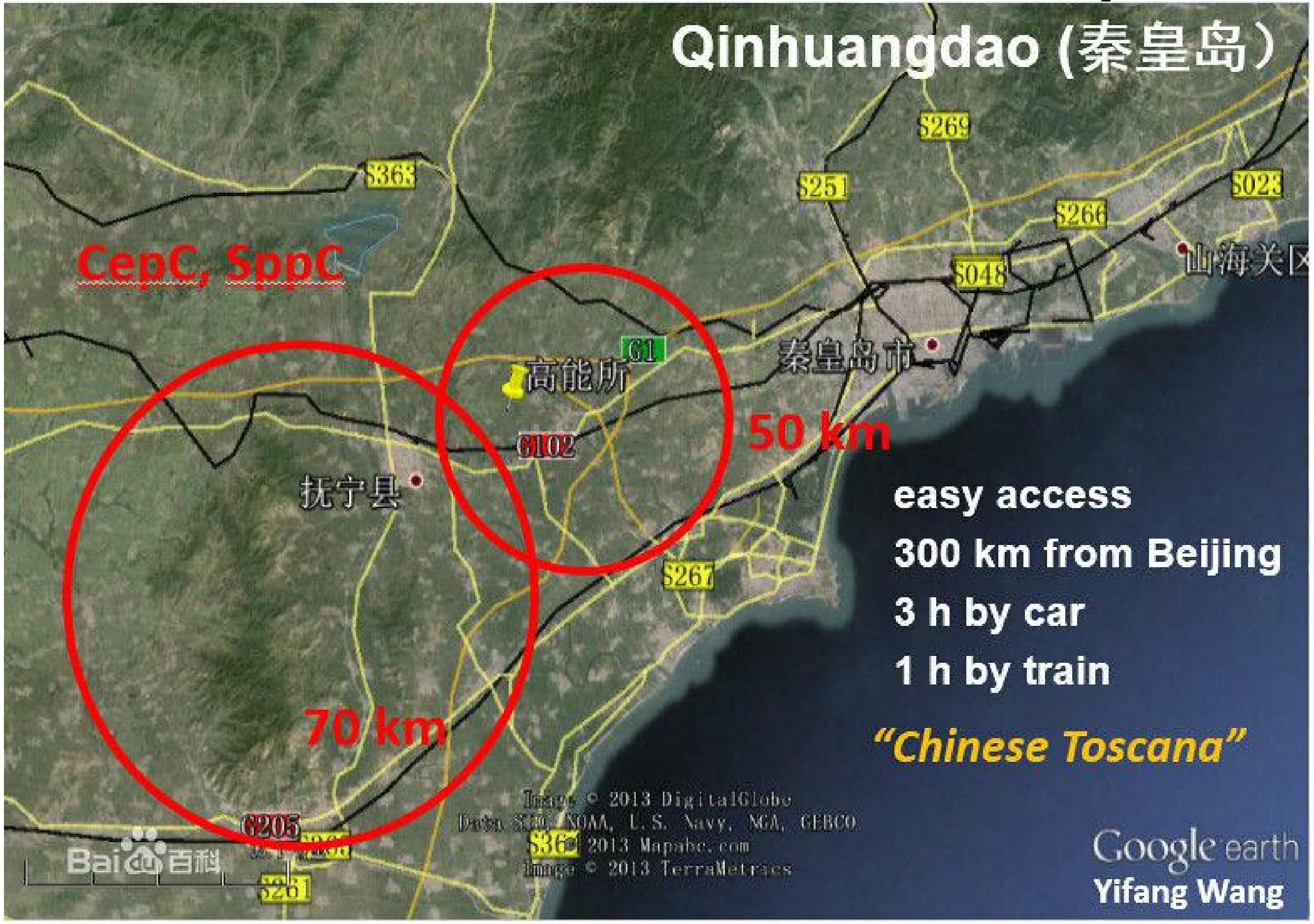
CEPC vertex detector

Xiangming Sun

CCNU

IHEP
SDU
CCNU
... ...

CEPC(Circular Electron Positron Collider)



Higgs factory in China in the future

CEPC vertex detector

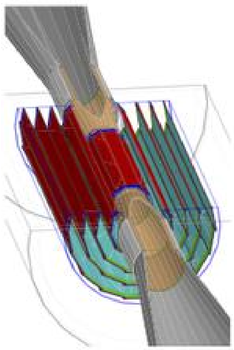
requirement
baseline solution
CMOS techology selection
readout structure
self-support
summary

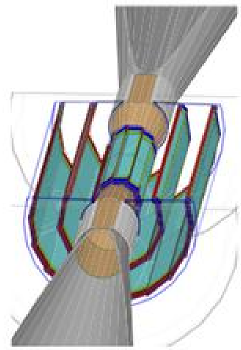
CEPC vertex requirement

parameters in research proposal:

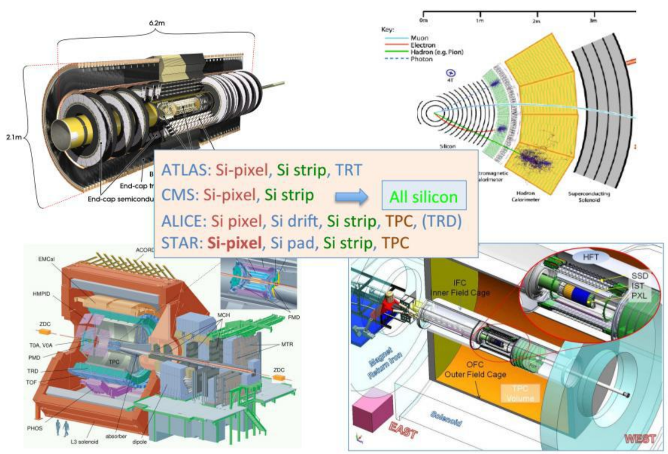
position resolution	5um
readout time	10-100us
power consumption	100mW/cm^2

baseline solution





preCDR: ILD-like solution
It will consist of multiple layers of state-of-art silicon pixelsensors, which enables the measurement of the position of charged particles with excellent accuracy. Much R&D has gone into reducing the thickness of each layer, which reduces the distortion of the path of the incoming particles.



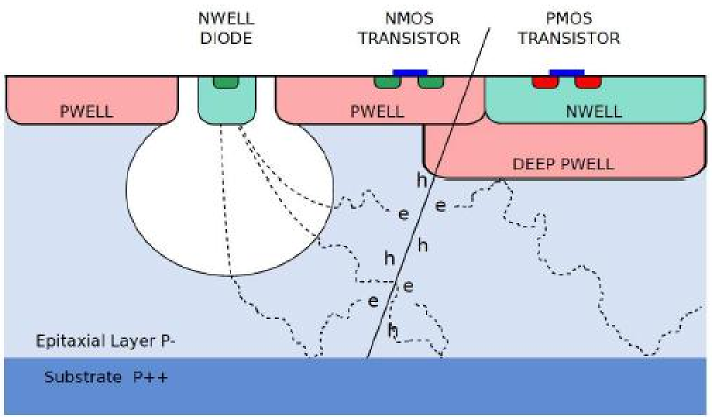
- MAPS
- carbon fiber structure
- lvds + optical link

applications：

STAR HFT
ALICE ITS upgrade

design chip matching CEPC requirement

CMOS MAPS



Integrated sensor and readout electronics on the same silicon bulk with "standard" CMOS process → low material budget, low power consumption, low cost …

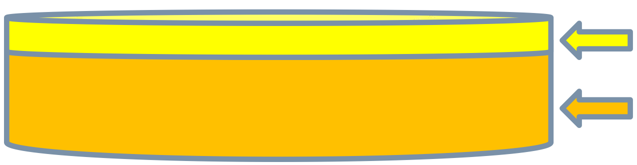
Ultimate (Mimosa 28) installed for STAR PXL, technology for ALICE ITS Upgrade

- primary candidate technology:
  TowerJazz 0.18 μm CIS technology for R&D, featuring:
  - Quadruple well process: deep PWELL shields NWELL of PMOS transistors, allowing for full CMOS circuitry within active area
  - Feature size of 0.18 μm and 6 metal layers: high-density and low power
  - Thick (20 – 40 μm) and high resistivity (1 kΩ cm) epitaxial layer
  - Thin gate oxide (3 nm): radiation tolerance

High-Resistivity Silicon Wafer Detector Pixel

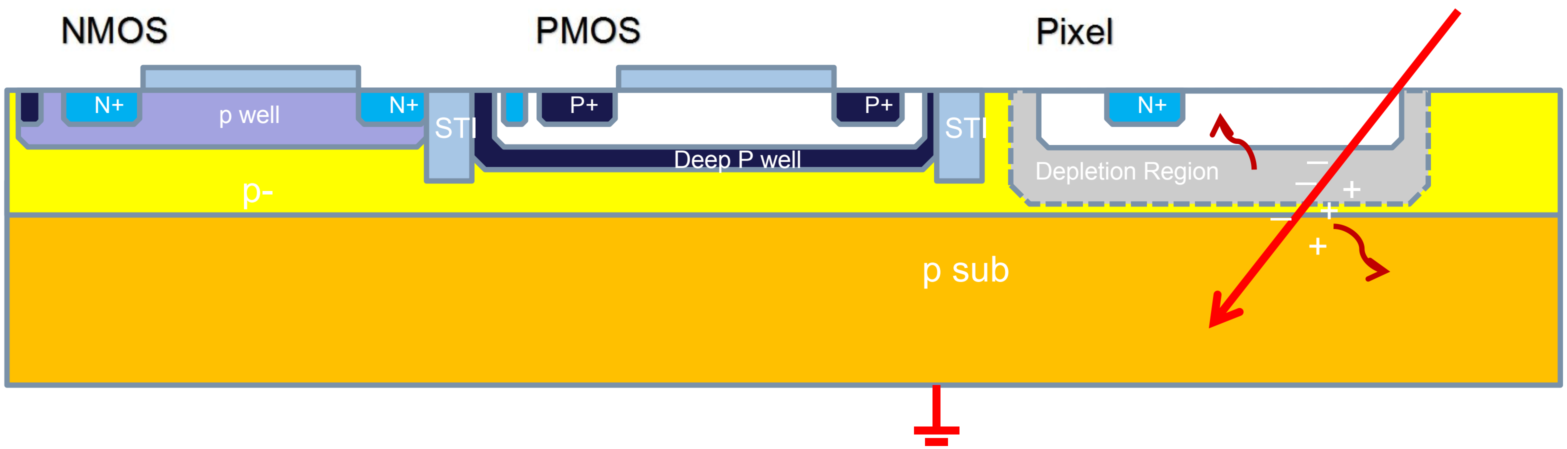
Process Introduction (I): Wafer Prepare

- .13/.18um bulk silicon process
- TD (Technology Development) process or matured commercial process
- Epi high resistivity bulk silicon wafer: SimGui or order from third party



Process Introduction (II): Device Fabrication HHGrace

- **Compatible with HHGrace existing high voltage process, which having HV pwell surrounding nwell.**
- **Device performance will be close to that of originally processed devices**
  - **Gate oxide thickness might be different in ~10% due to the growth speed difference on HR surface.**
  - **Device performance change should be covered by corner model.**



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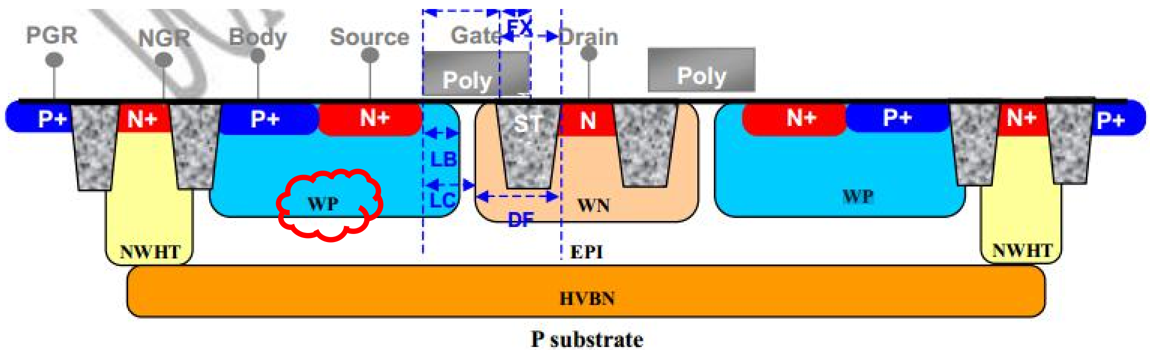
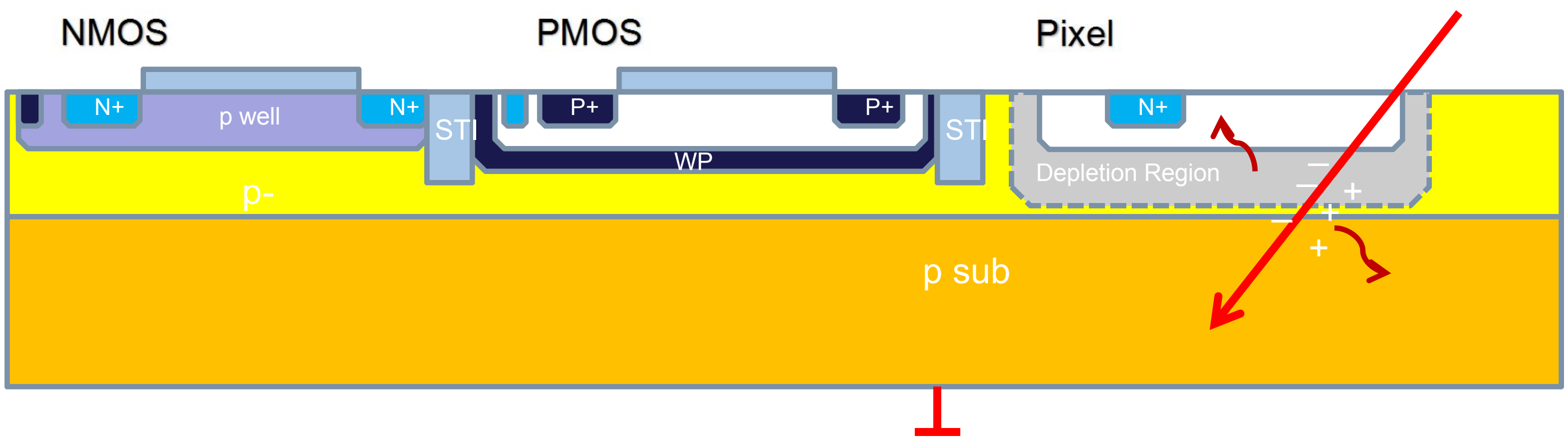
Process Introduction (III): Device Fabrication SMIC

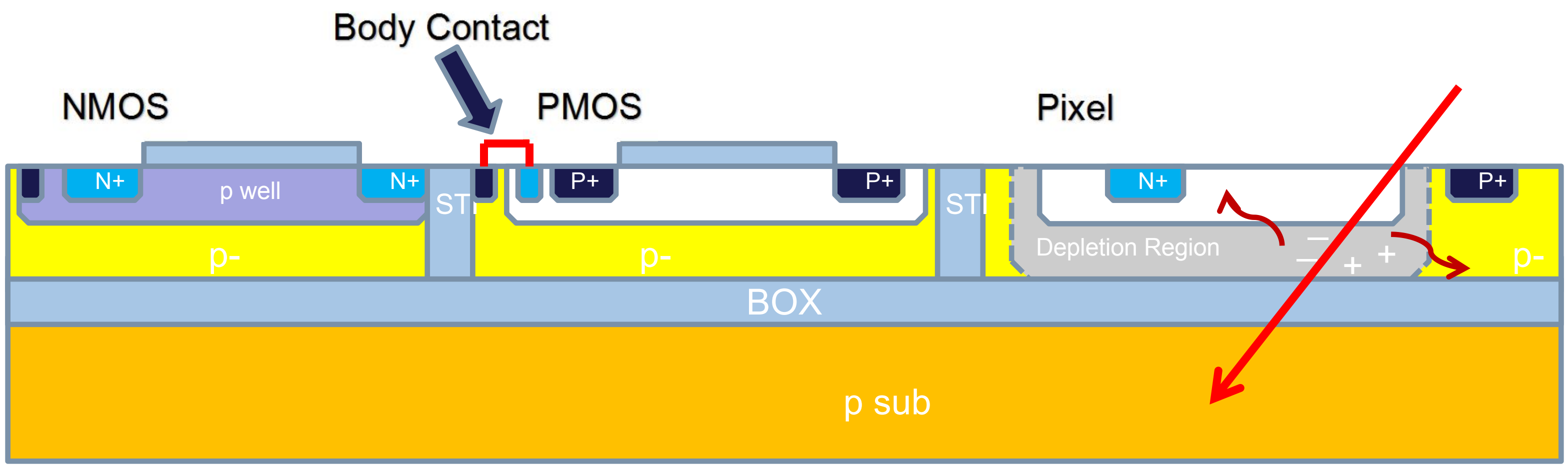
- **Compatible with SMIC existing high voltage process, similar to HHGrace, there is a WP layer**





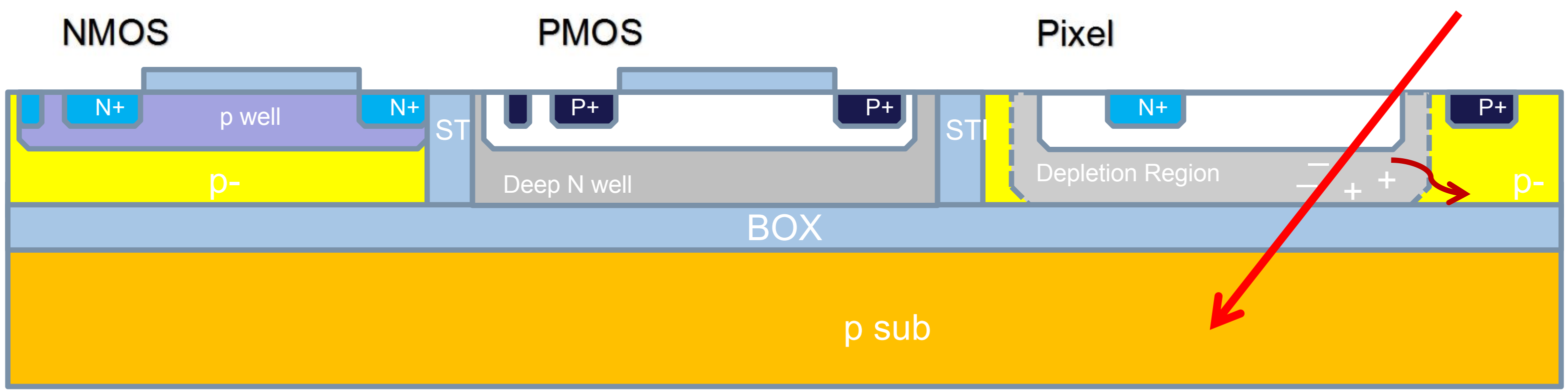
New Proposal : SOI Structure (I)

- **Epi SOI wafer with 2um thick top silicon.**
- **Compatible with TSMC SOI process, which supporting 2um thick top silicon and 2um BOX.**
- **Add extra body contact in p- region and short this with body contact in nwell.**
- **PMOS and NMOS can be totally isolated due to BOX. In this way, p- in PMOS and p- in NMOS can be biased differently, while in bulk process it is difficult.**
- **Thus nwell and p- in PMOS won't be reversed and the depletion region won't be large.**



New Proposal : SOI Structure (II)

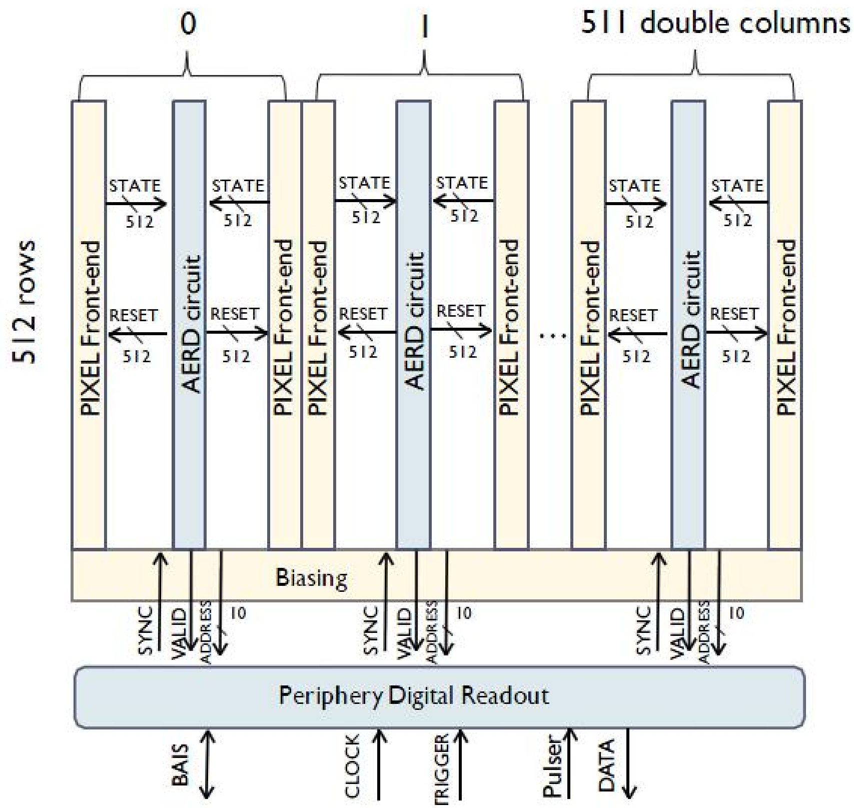
- Add one more extra mask to create deep nwell, which reaches BOX to exclude p- in PMOS.



CMOS techology selection

- **It is worth to try commecial .13/.18um bulk process with extra HV-like mask layer**
- **Closely collaborate with fabs, SimGui and support team**
- **Better process and customized steps**
- **Better support**
  - **Epi wafers: 20um/1000Ω and 50um/1000Ω**

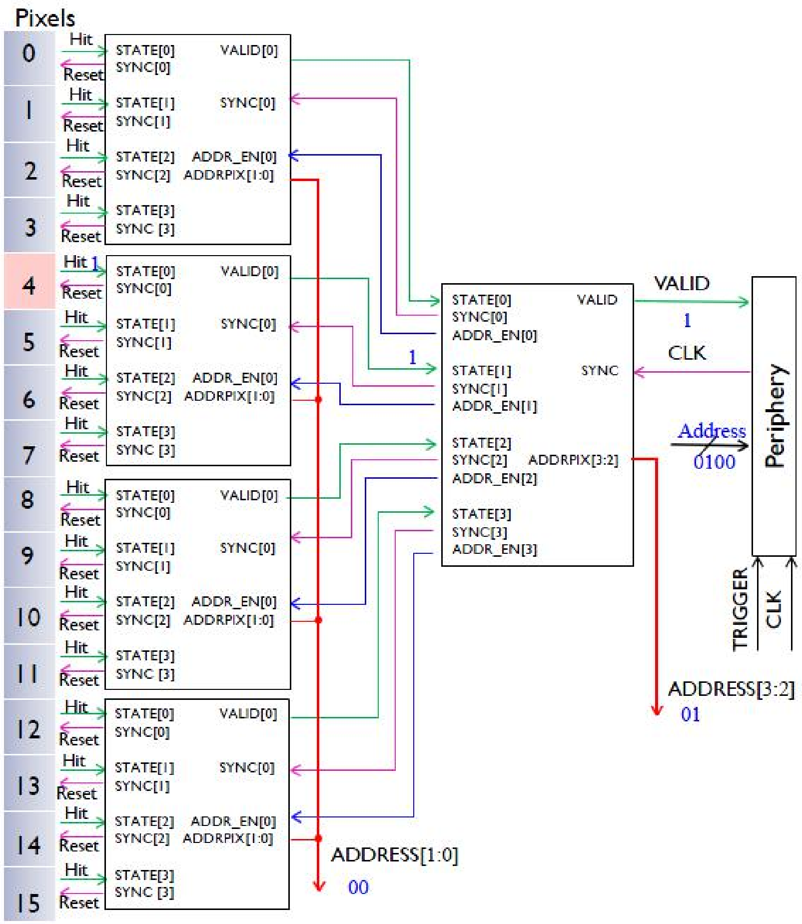
readout design

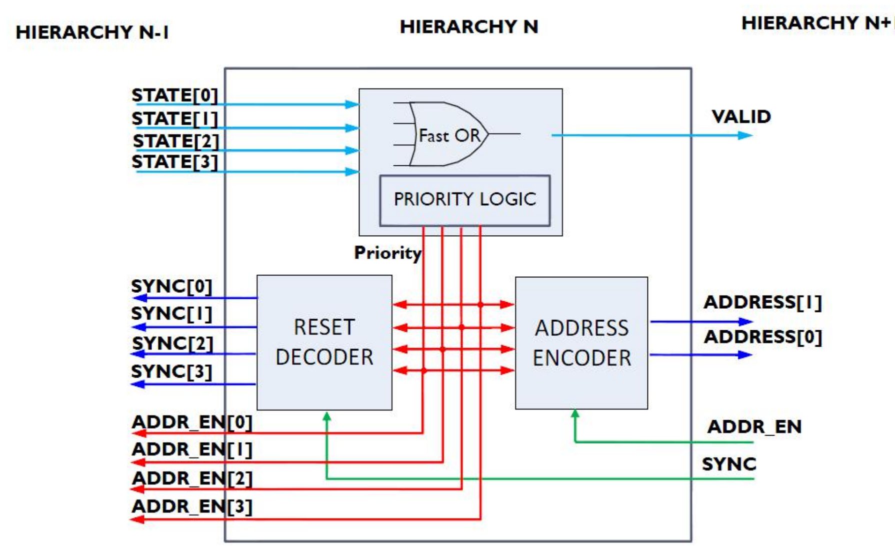


ALPIDE sensor readout structure

similar readout structure like ALPIDE sensor for ALICE ITS upgrade

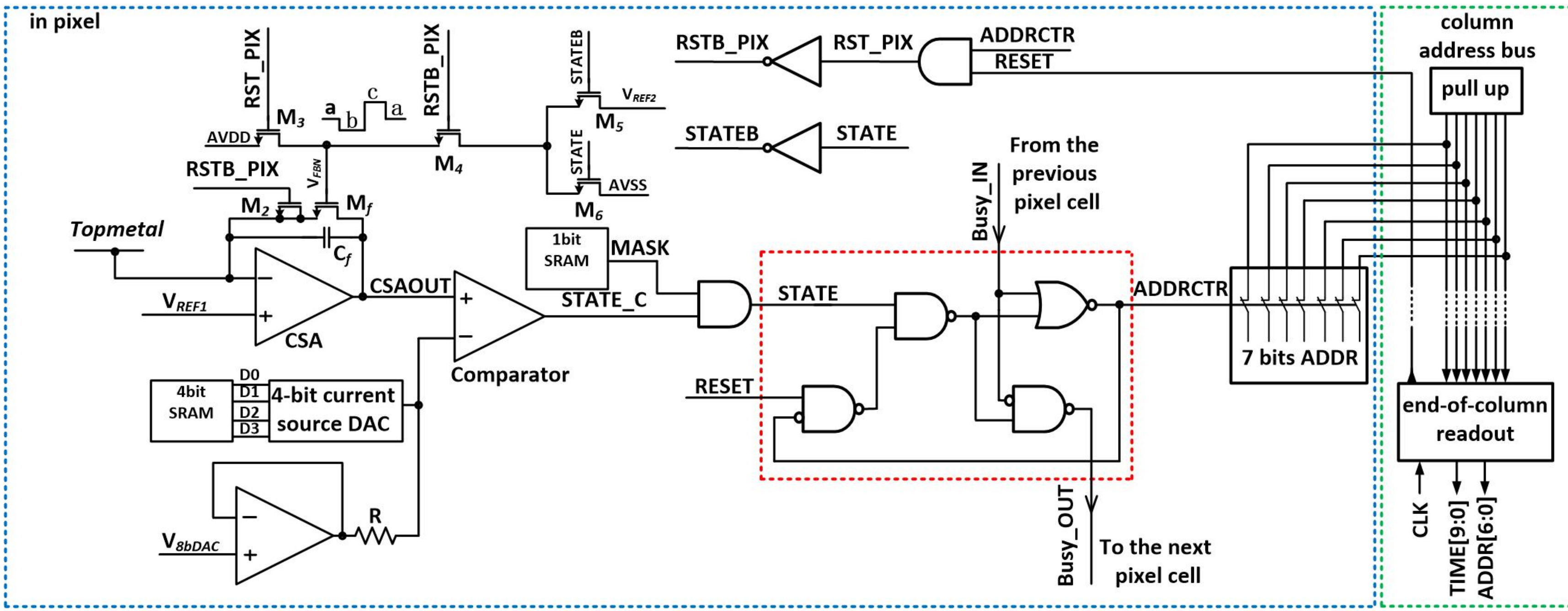
column readut





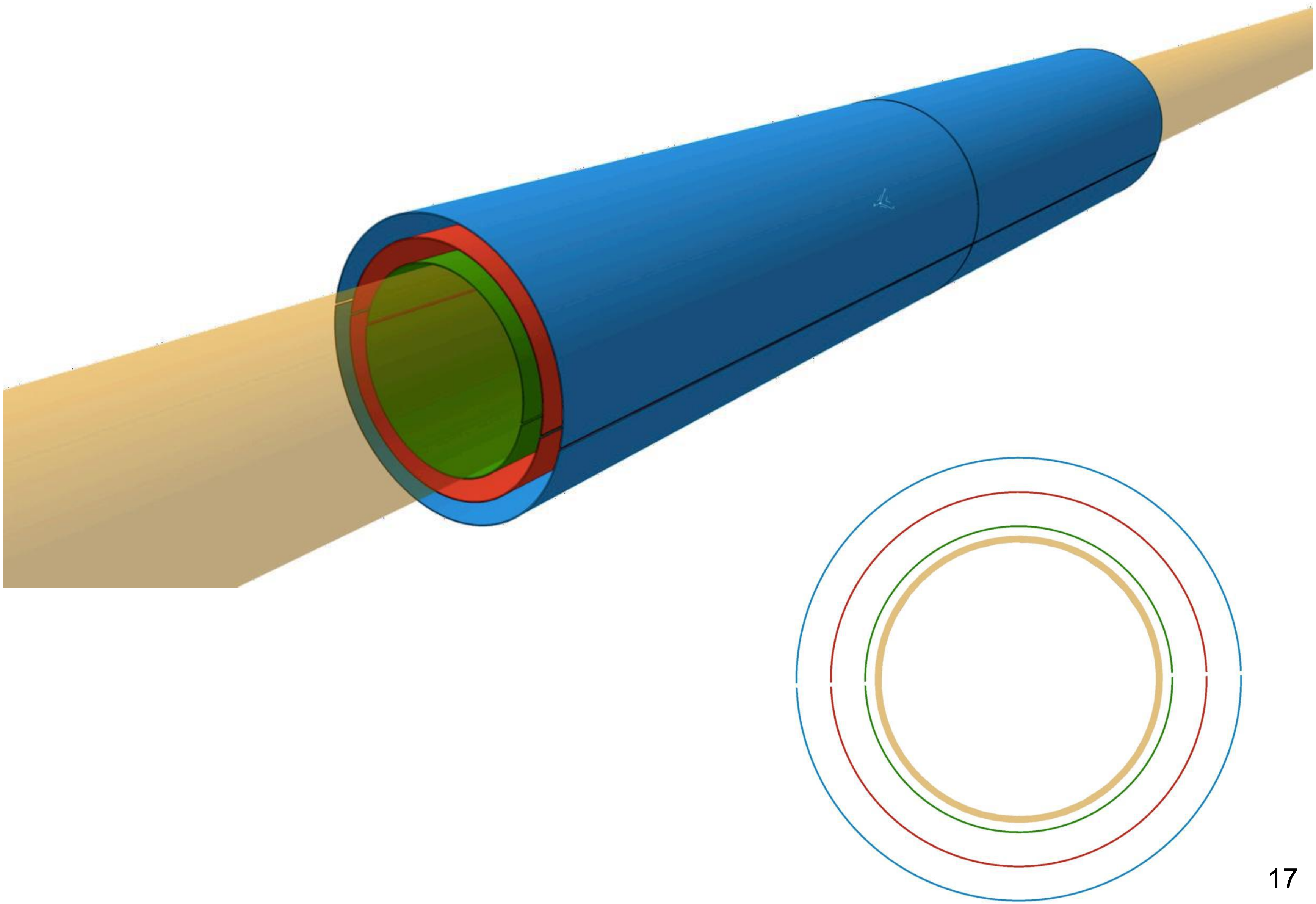
column readout module

address encoding

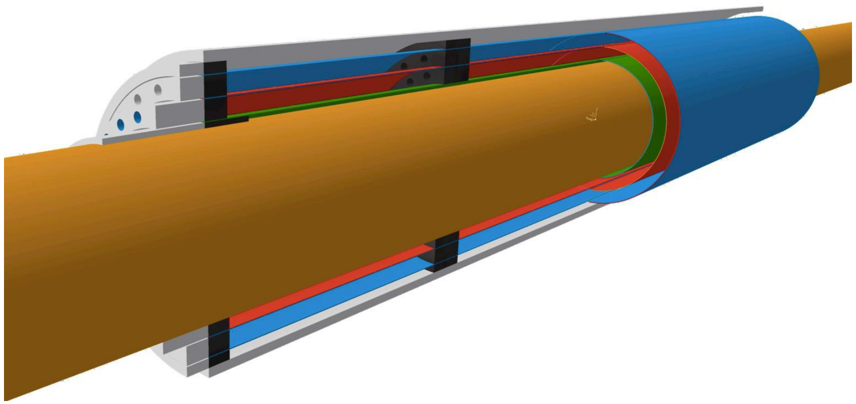


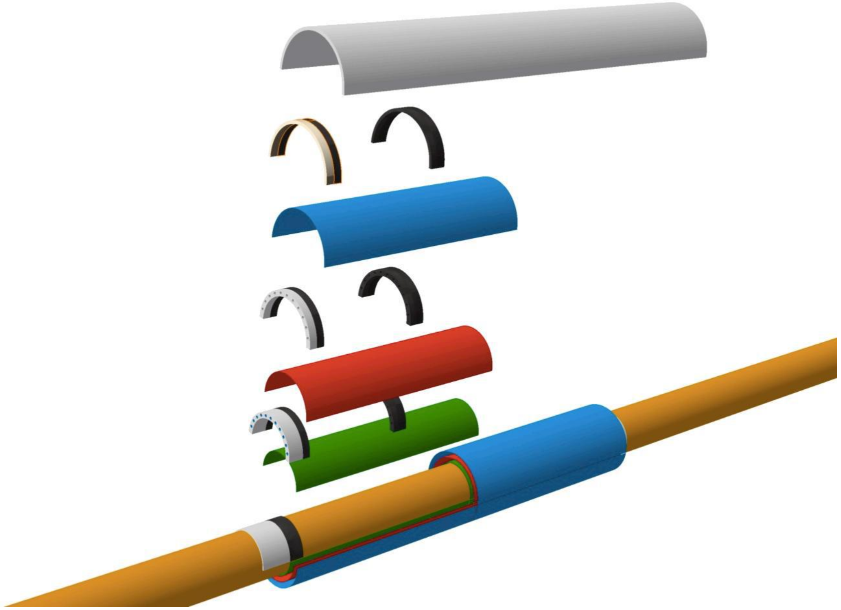
using address encodeing to make the column readout module compact

self-support

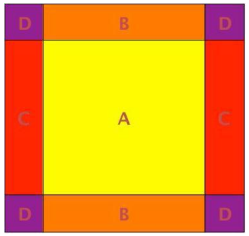


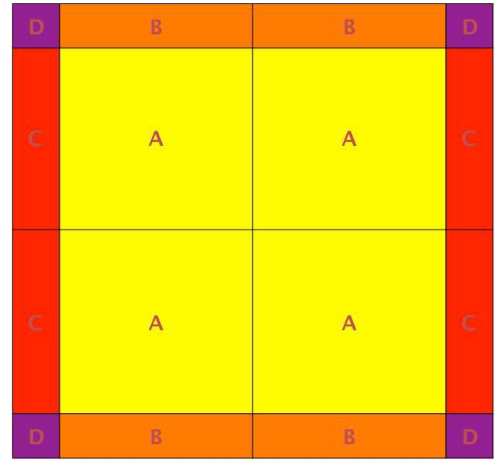
self-support

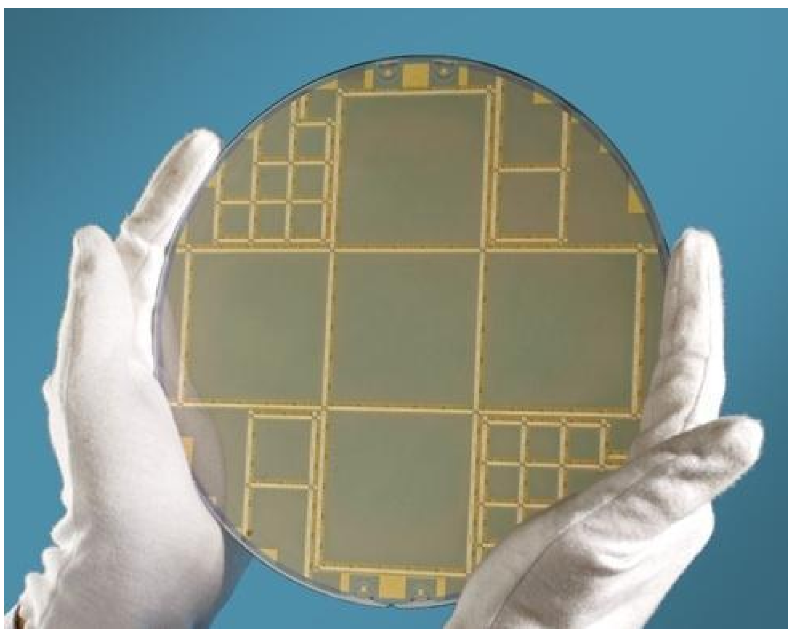


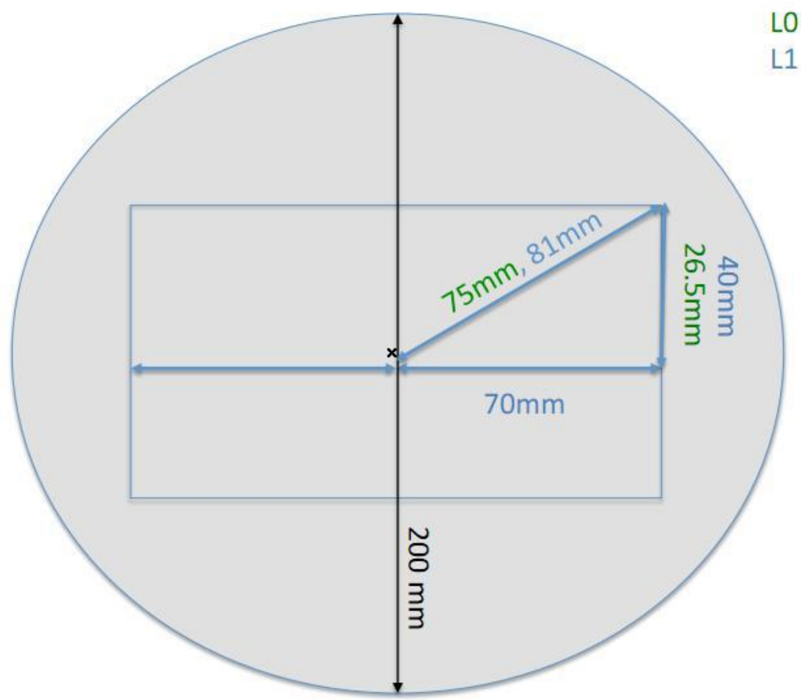


sensor design for selp-support





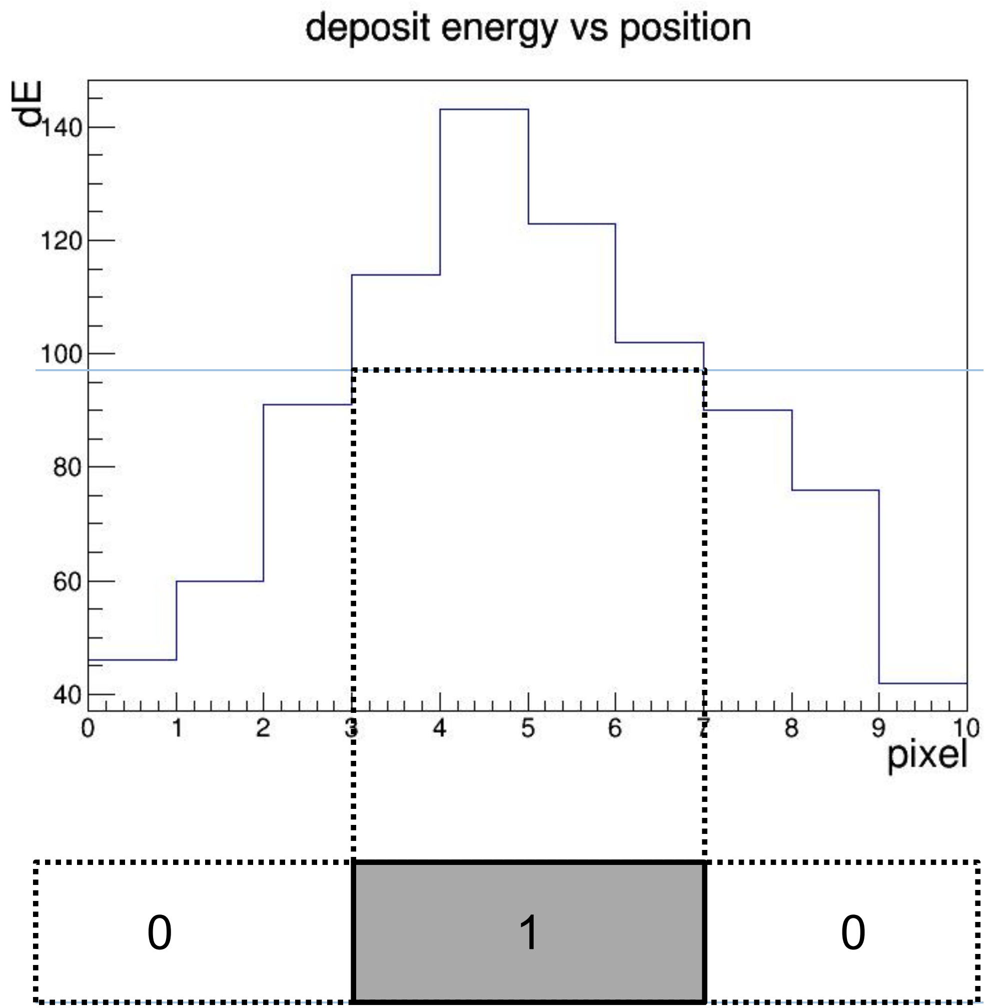




Thank you for attention

better position resolution solution

postion resolution-weighting method



increase postion resolution to 1/10

MC simulation

- pixel size 10um
- ADC bits 9位
- threshold 3 σ
- ENC 10 e^-
- diffusion 10um
- signal charge 2000

energy deposition：
2000e~7.2KeV~8um depleted region
shape of signal：
guass

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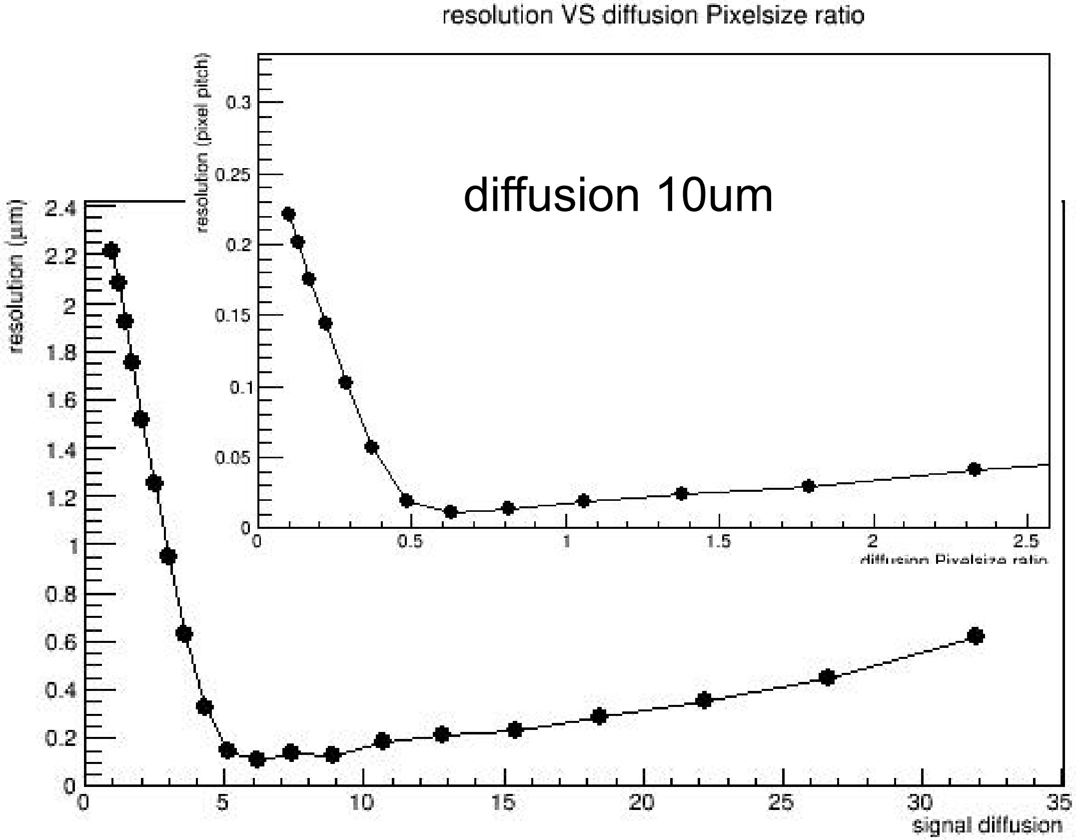
diffusion

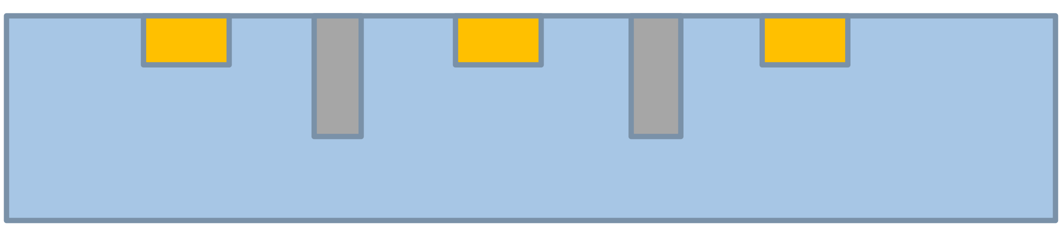


thickness L=20*10^-6;
bias V=3;

Diff=u*k*T/q;
EField=V/L;
driftSpeed=EField*u;
t=L/driftSpeed;

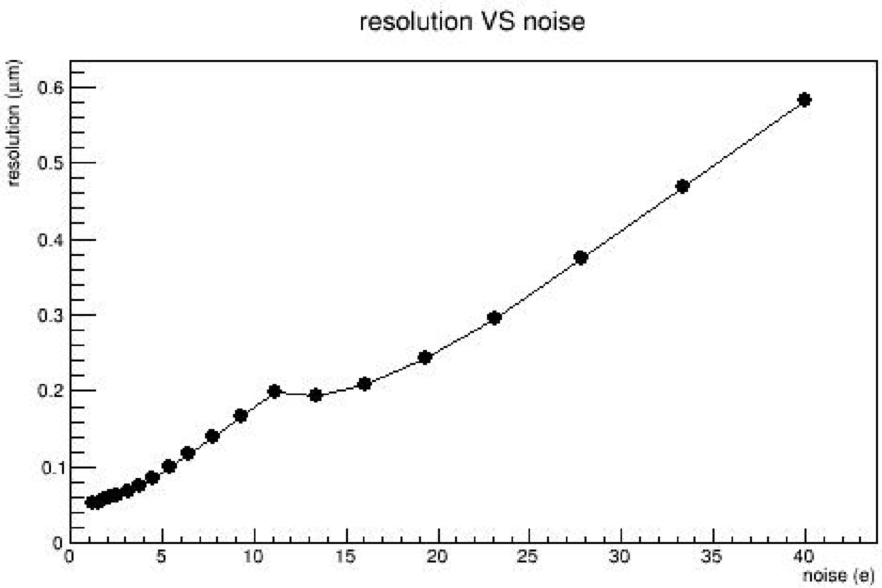
thickness L=20*10^-6;
bias V=3;
Sigma= 5.25um

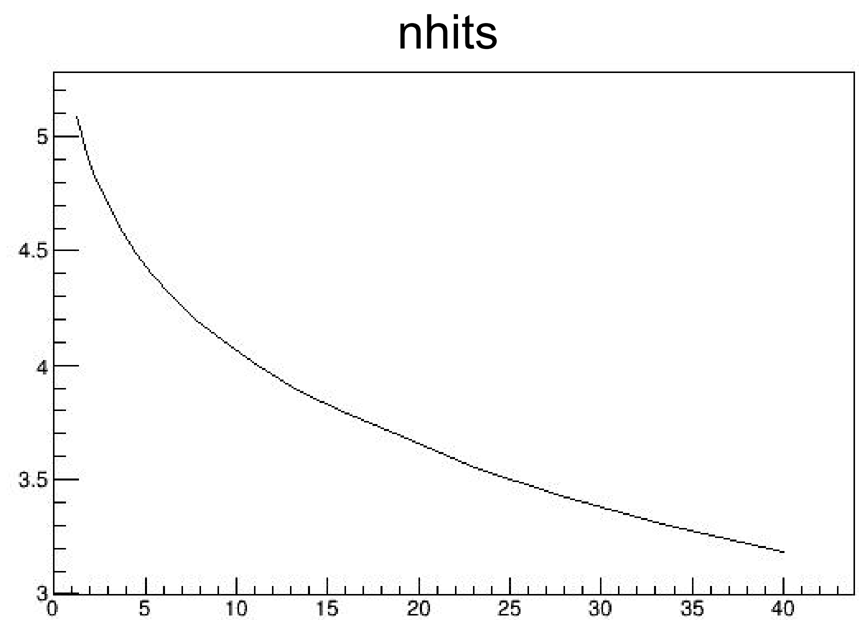
Weighting Field also affect diffusion



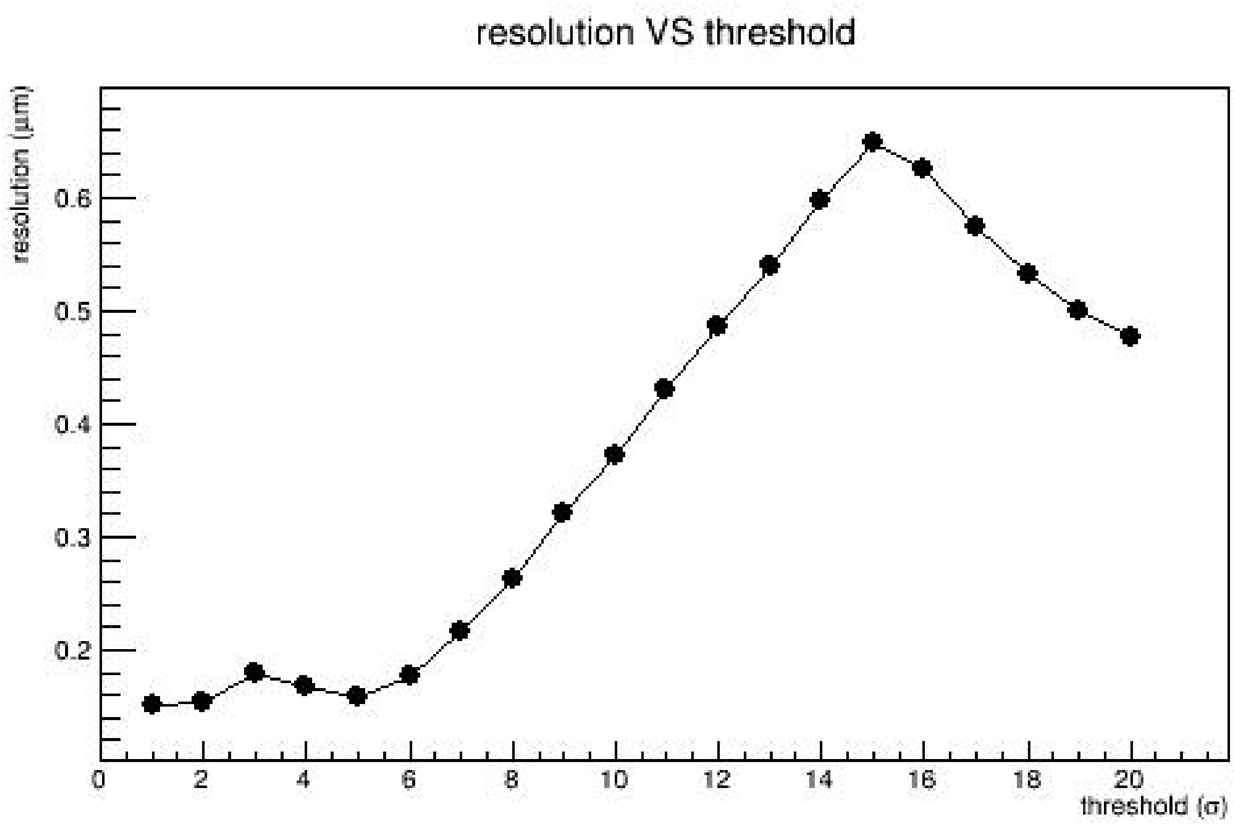
NWell
p trench
p epi

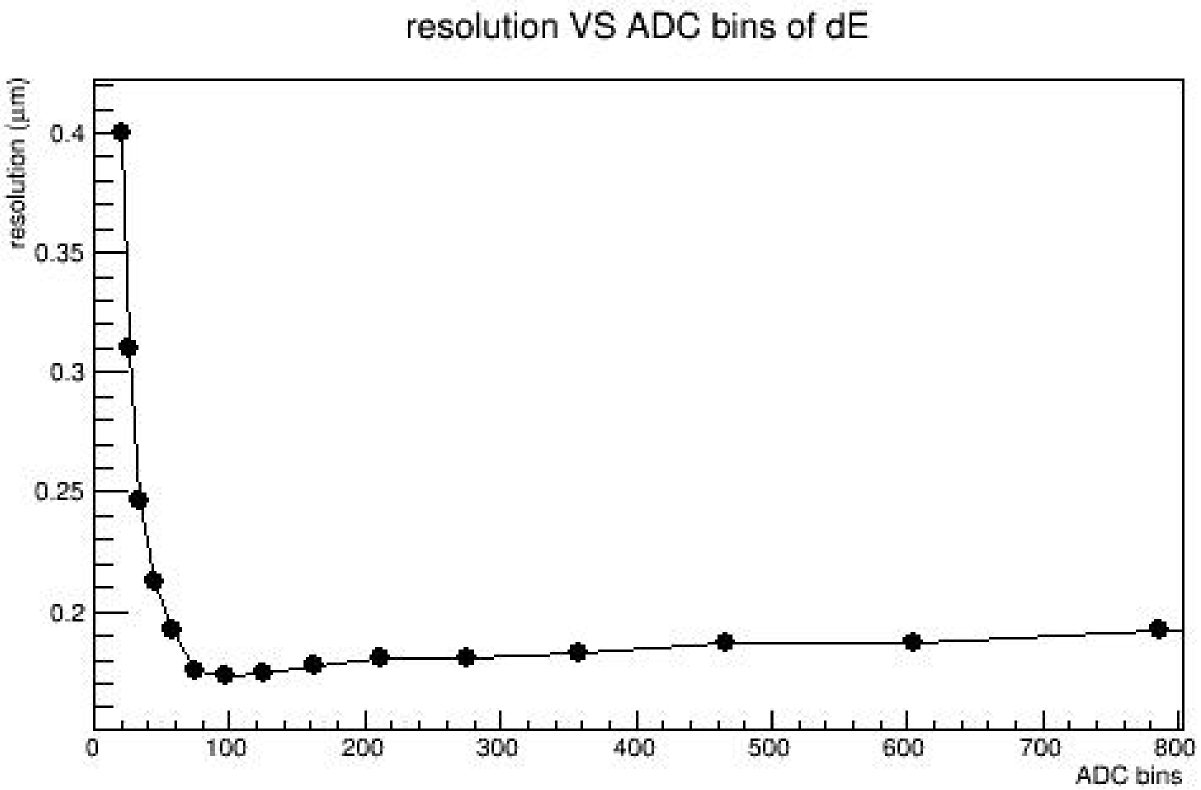
noise



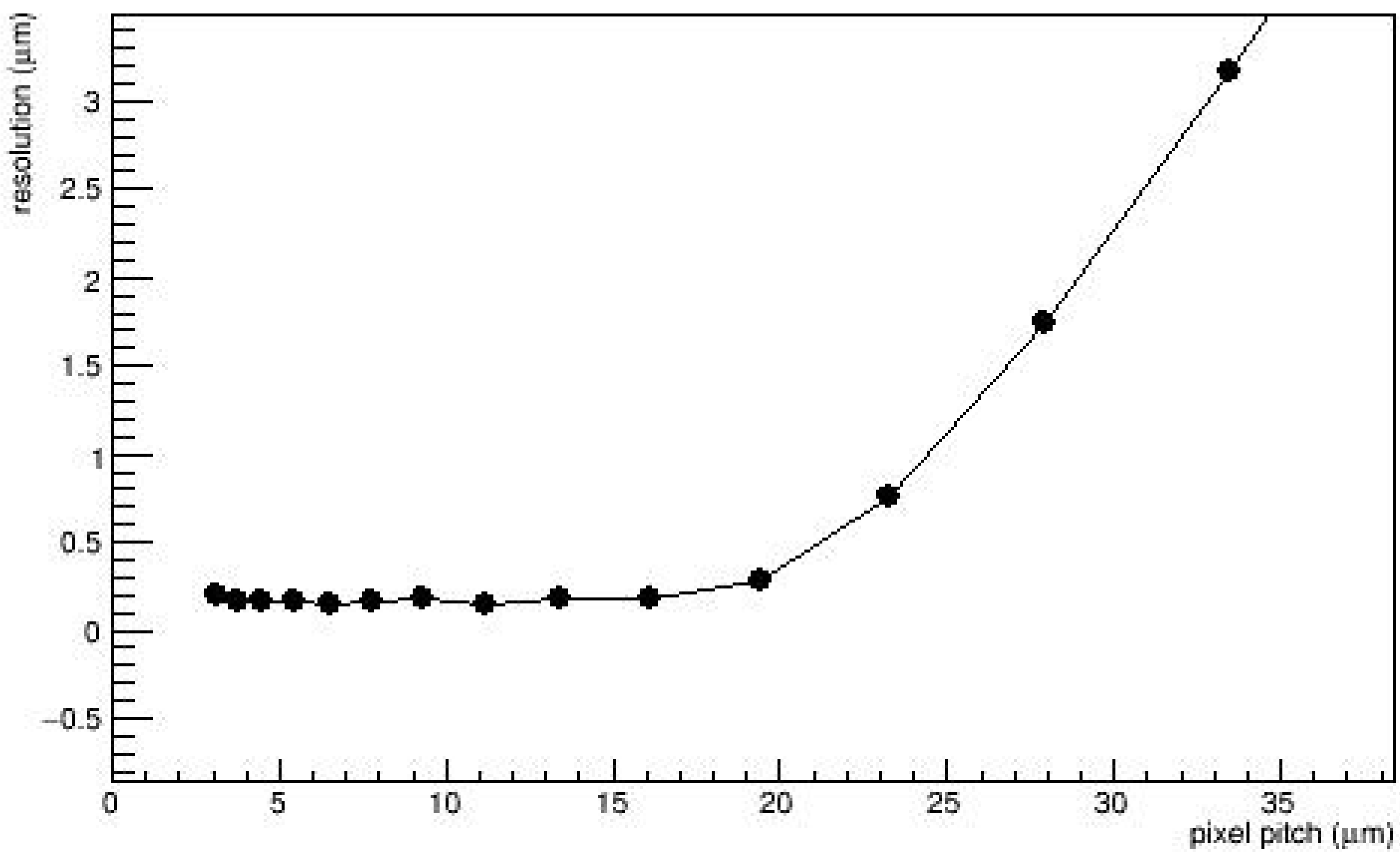


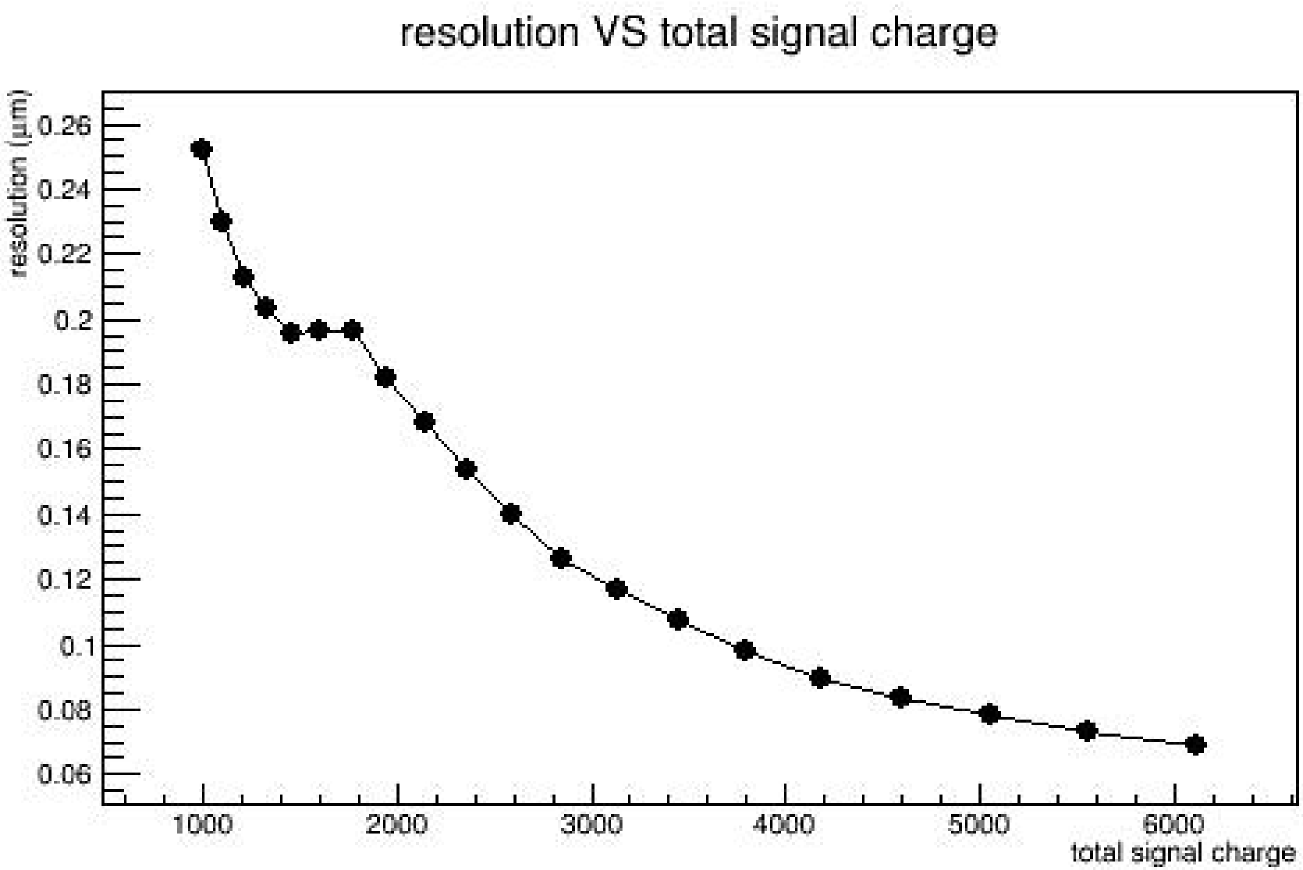
pixel number in weighting method vs noise


resolution VS threshold
resolution (μm)
0.2
0.3
0.4
0.5
0.6
0
2
4
6
8
10
12
14
16
18
20
threshold (σ)


resolution VS ADC bins of dE
resolution (μm)
0.4
0.35
0.3
0.25
0.2
0
100
200
300
400
500
600
700
800
ADC bins

resolution VS pixel pitch



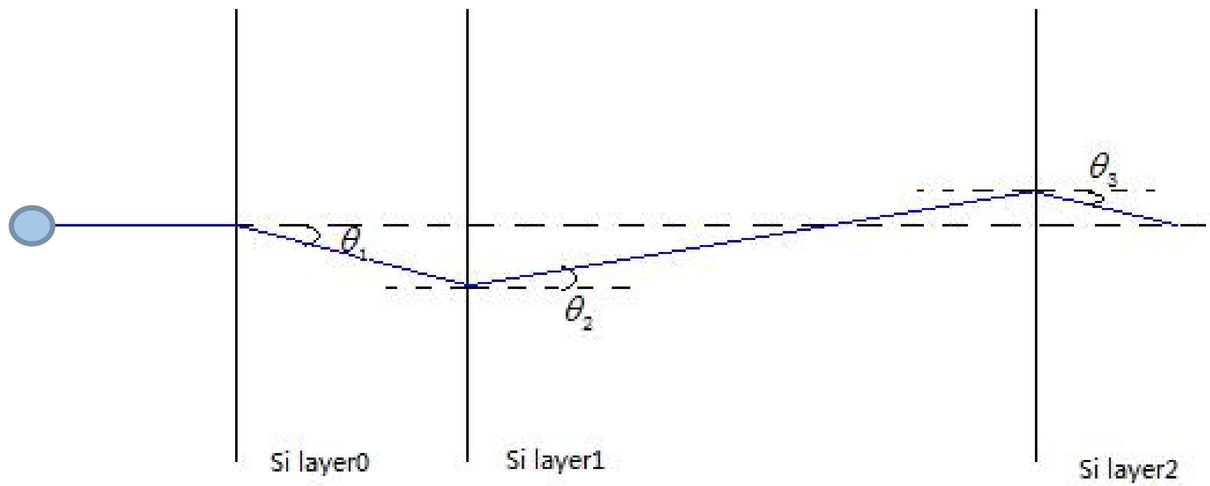

resolution VS total signal charge
resolution (μm)
0.26
0.24
0.22
0.2
0.18
0.16
0.14
0.12
0.1
0.08
0.06
1000
2000
3000
4000
5000
6000
total signal charge

position resolution

- pixel size 10um
- ADC bits 9
- threshold 3 σ
- ENC 10 e^-
- diffusion 10um
- signal charge 2000

position resolution
0.2um

vertex resolution

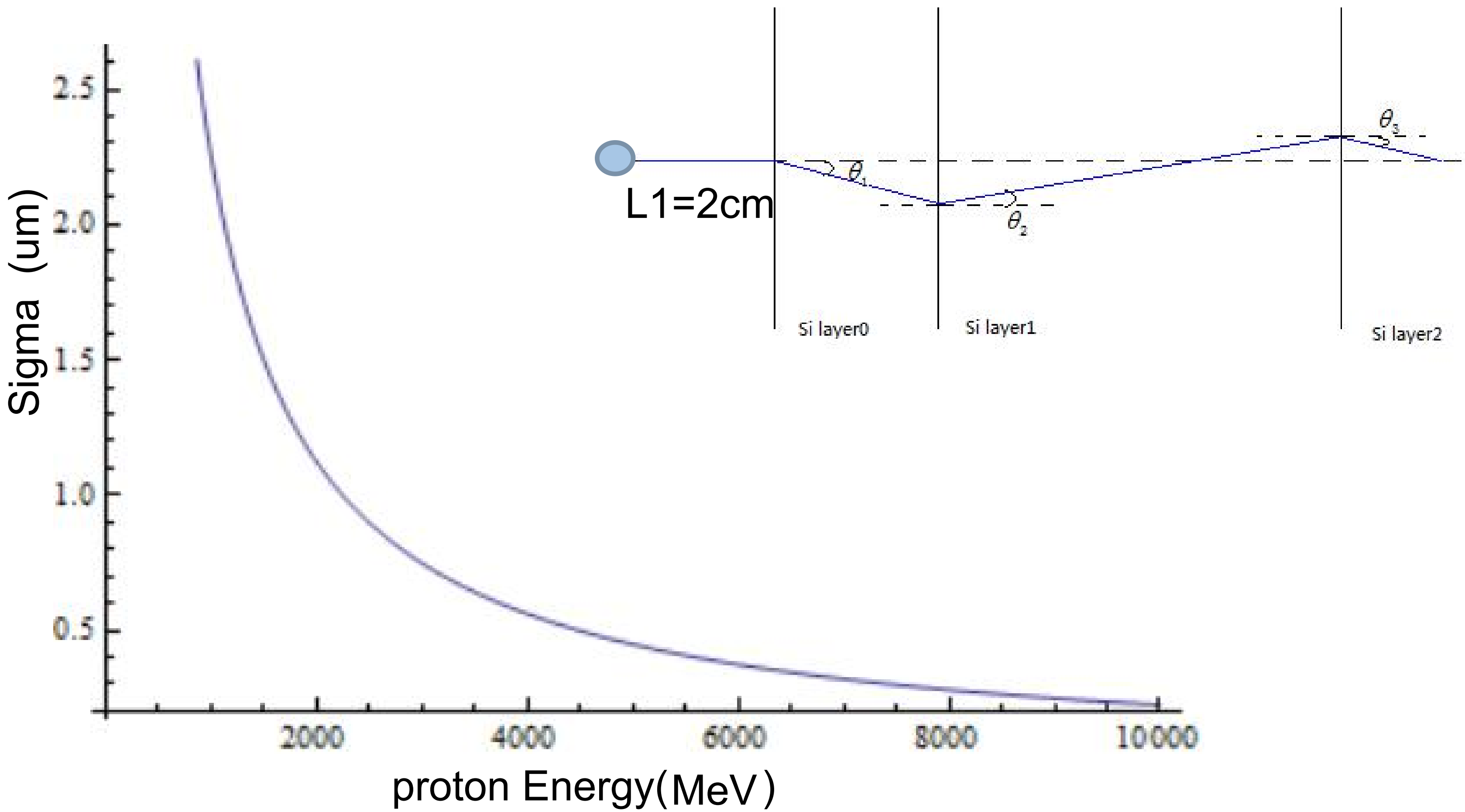


vertex resolution：

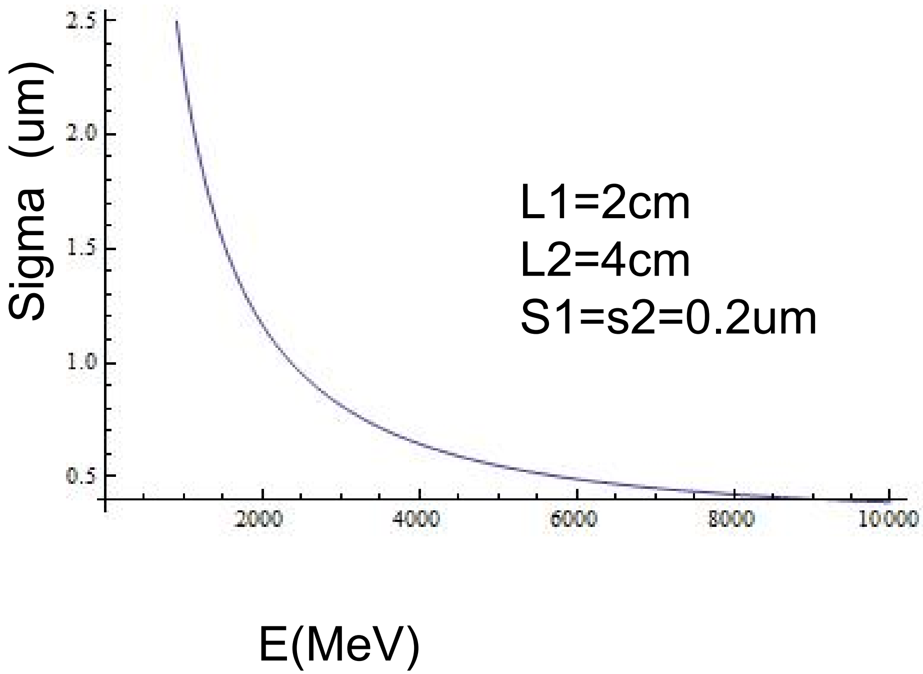
sigma= ((sita*L1)^2 + (s1*(L1 + L2)/L2)^2 + (s2*L1/L2)^2)^0.5

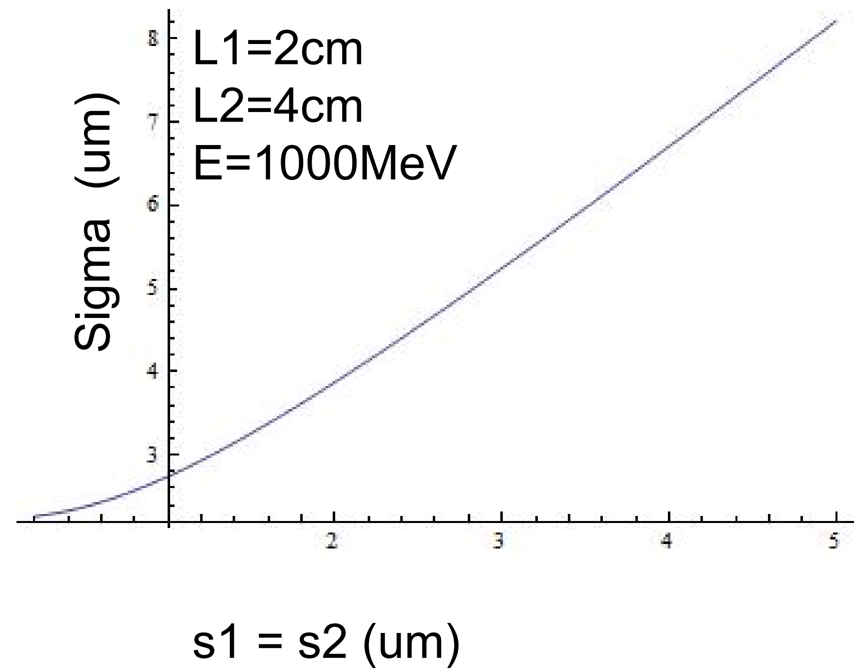
L1 : distance between vertex and layer1;
L2 : distance between layer1 and layer2 ;
sita : multiple coulomb scattering angle for layer1=1.12*10^-4 for 50um Si 1GeV proton
s1 : position resolution of layer1;
s2 : position resolution of layer2;

multiple Coulomb scattering



vertex resolution





sigma= ((sita*L1)^2 + (s1*(L1 + L2)/L2)^2 + (s2*L1/L2)^2)^0.5

data rate

$$frameRate := 10^4 \cdot \frac{1}{s}$$

$$timeRes := 10^{-7} \cdot s$$

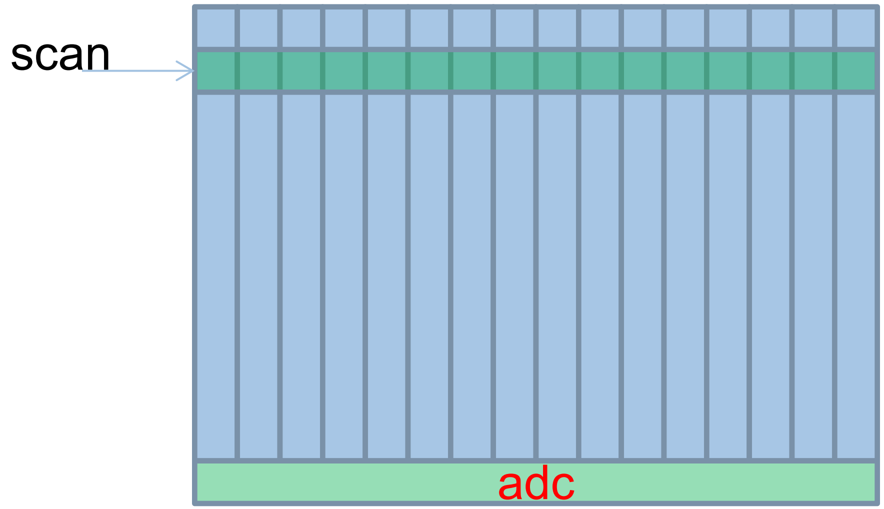
$$hitRate := 10^7 \cdot \frac{1}{s}$$

$$hitPerParticle := 3$$

$$chipSize := 3 \cdot cm$$

$$pixelSize := 20 \cdot \mu m$$

$$analogBit := 8$$



$$timeBit := \log\left(\frac{1}{frameRate \cdot timeRes}, 2\right) = 9.966$$

$$positionBit := \log\left(\frac{chipSize}{pixelSize}, 2\right) = 10.551$$

$$clkFre := frameRate \cdot \left(\frac{chipSize}{pixelSize}\right)^1 = 1.5 \times 10^7 s^{-1}$$

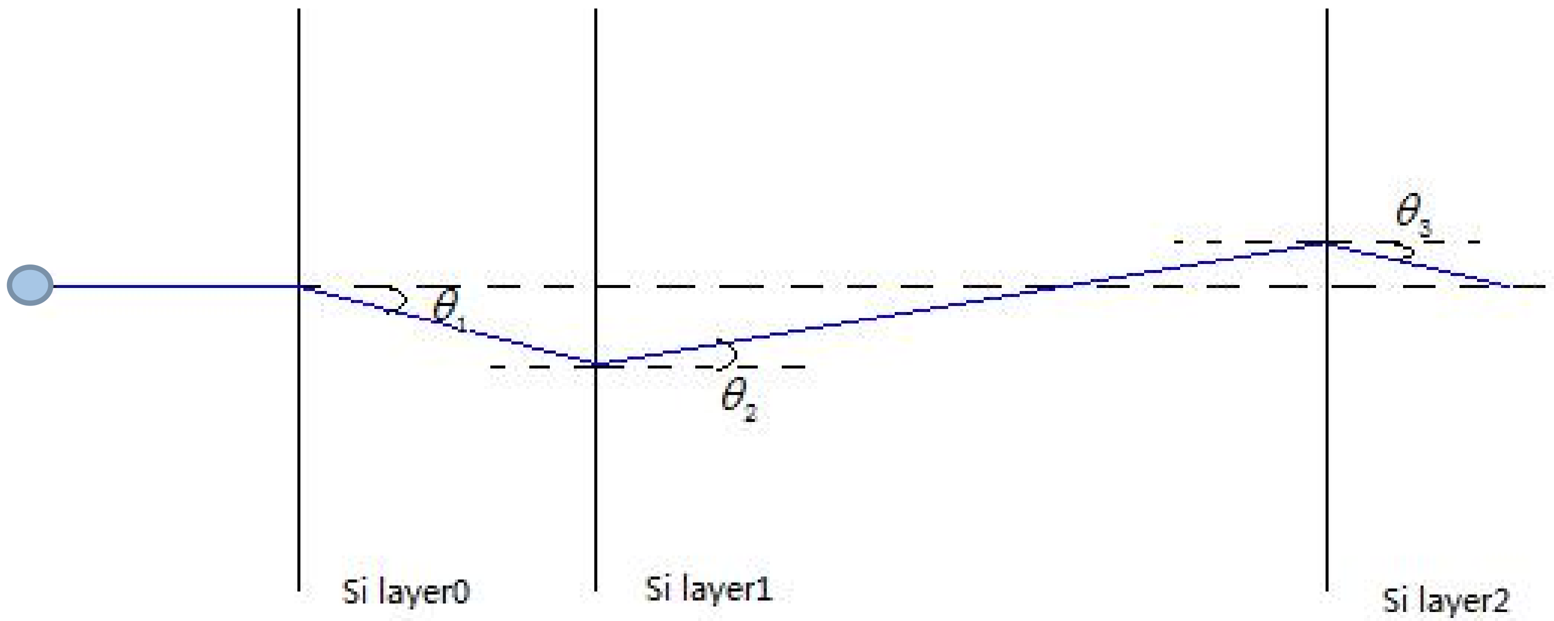
$$dataRate := [2 \cdot (positionBit) + timeBit + analogBit] \cdot hitRate \cdot hitPerParticle = 1.172 \times 10^9 s^{-1}$$

readout structure and power consumption added

- priority address encoding
- SCA on each column
- ADC is for each section

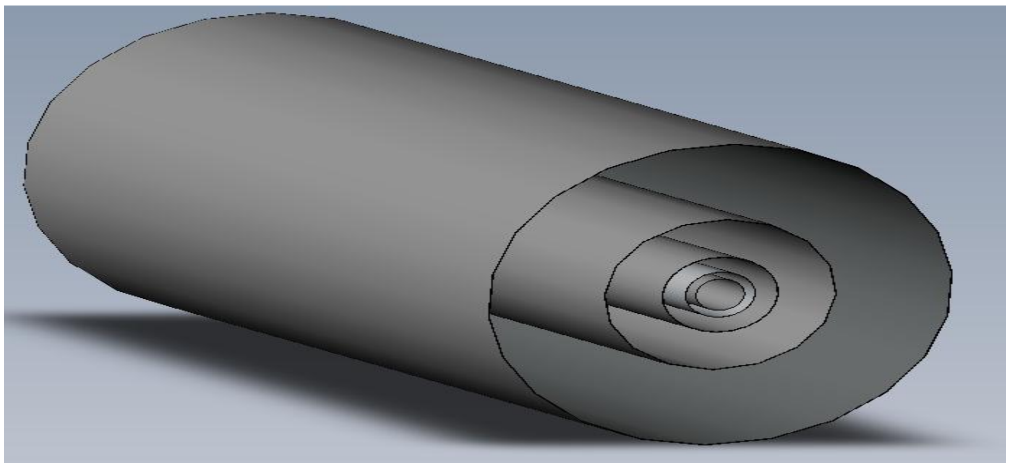
+SF+SCA+ADC on each hits

detector design requirement



only θ 1 matters
the first layer should be as thin as possible
vacuum between collision point to the first layer

自支撑结构仿真



探测器结构为五层，最内两层为50μm硅，100 μm铍束流管，外面三层为自支撑结构的硅探测器。

Geant4仿真中，除了上面这些部分设定材料外，其他空间填充的为空气。

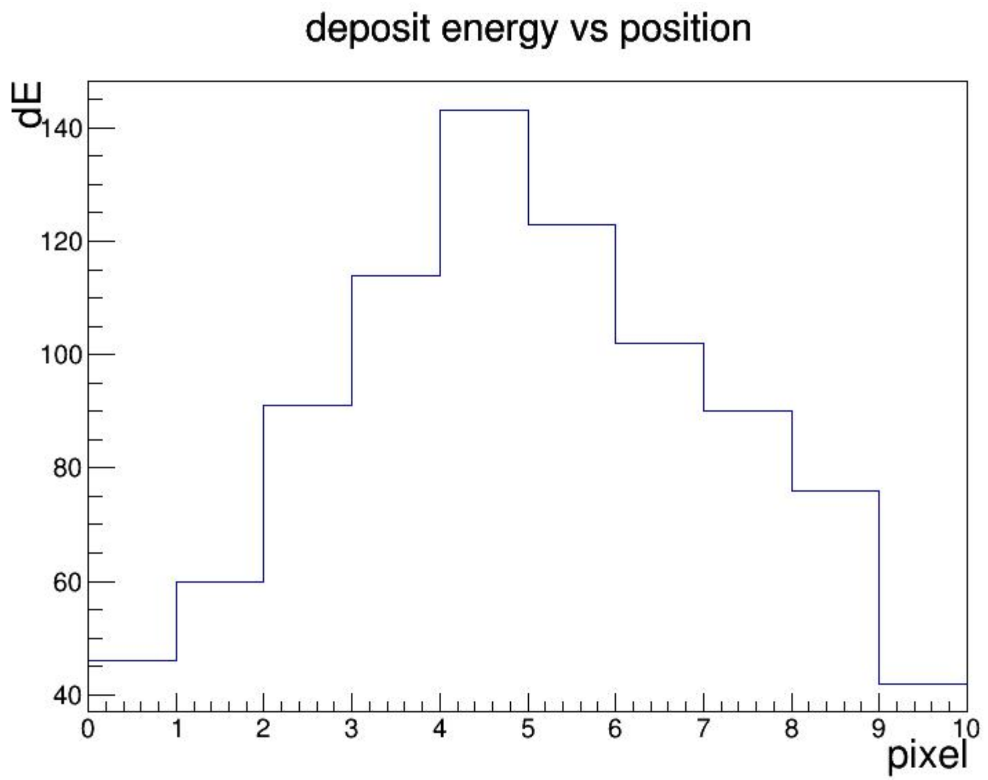
仿真中，由几何中心位置沿一定方向发射能量范围为1GeV到10GeV的质子。

进一步提高空间分辨能力

- 硅的厚度不可能无限减小下去，50um已接近目前工业极限。
- 像素的尺寸也有限制，分辨率无法突破1um

- 要进一步提高空间分辨能力，需要让出射粒子直接打到第一层探测器上，第一层探测器需放在束流管内。称为束流管层

束流管层+重心法



重心法可以达到小于单通道探测器大小1/10以上的精度

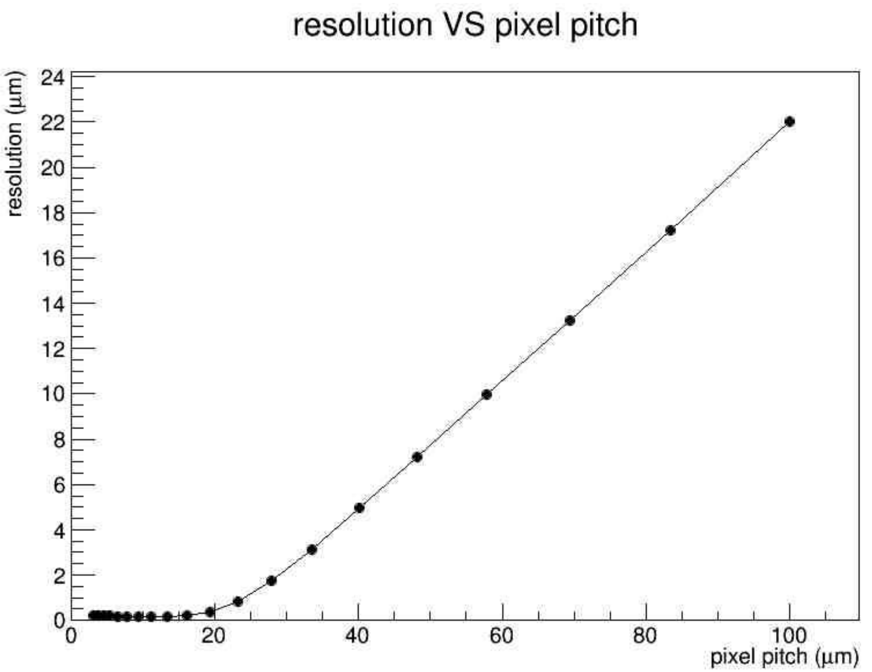
用在像素探测器上?

東流管层空间分辨的影响因素

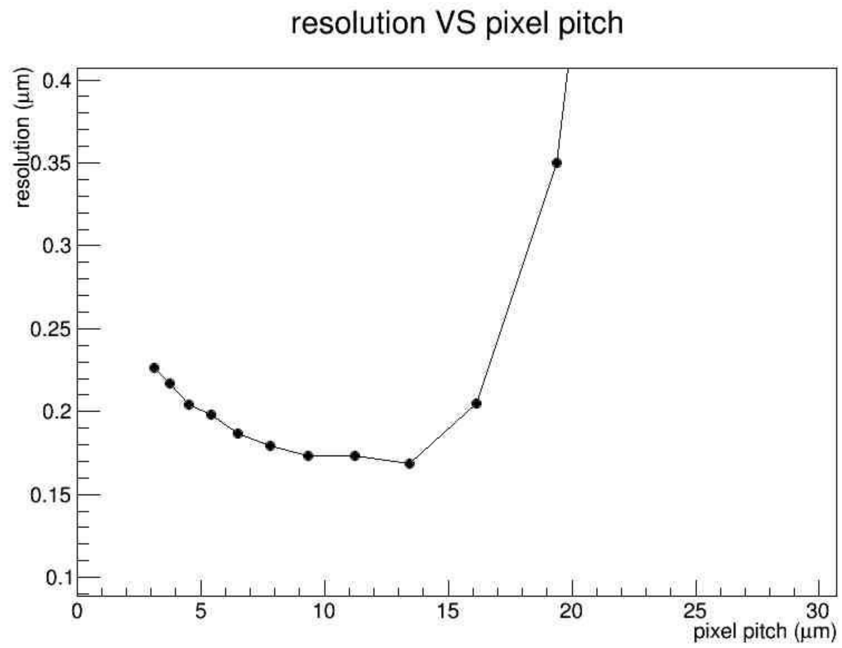
- 像素大小 10um
- ADC位数 9位
- 像素阈值 3 σ
- 像素噪声 10 e^-
- 信号扩散 10um
- 信号电荷 2000

能量沉积设为：
2000个电子~7.2KeV~8um耗尽层
信号的形状设为：
高斯分布

像素大小

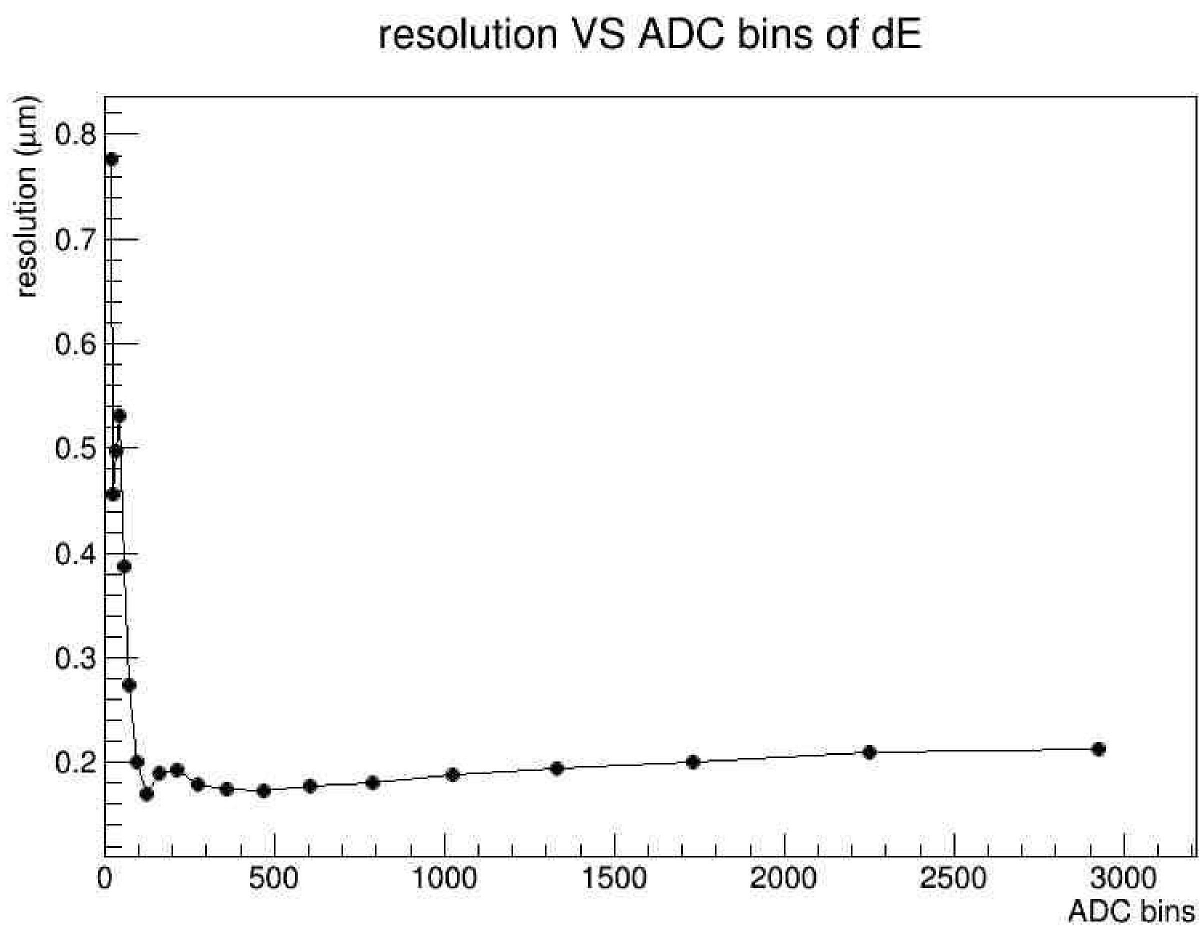


resolution VS pixel pitch
resolution (μm)
24
22
20
18
16
14
12
10
8
6
4
2
0
0
20
40
60
80
100
pixel pitch (μm)

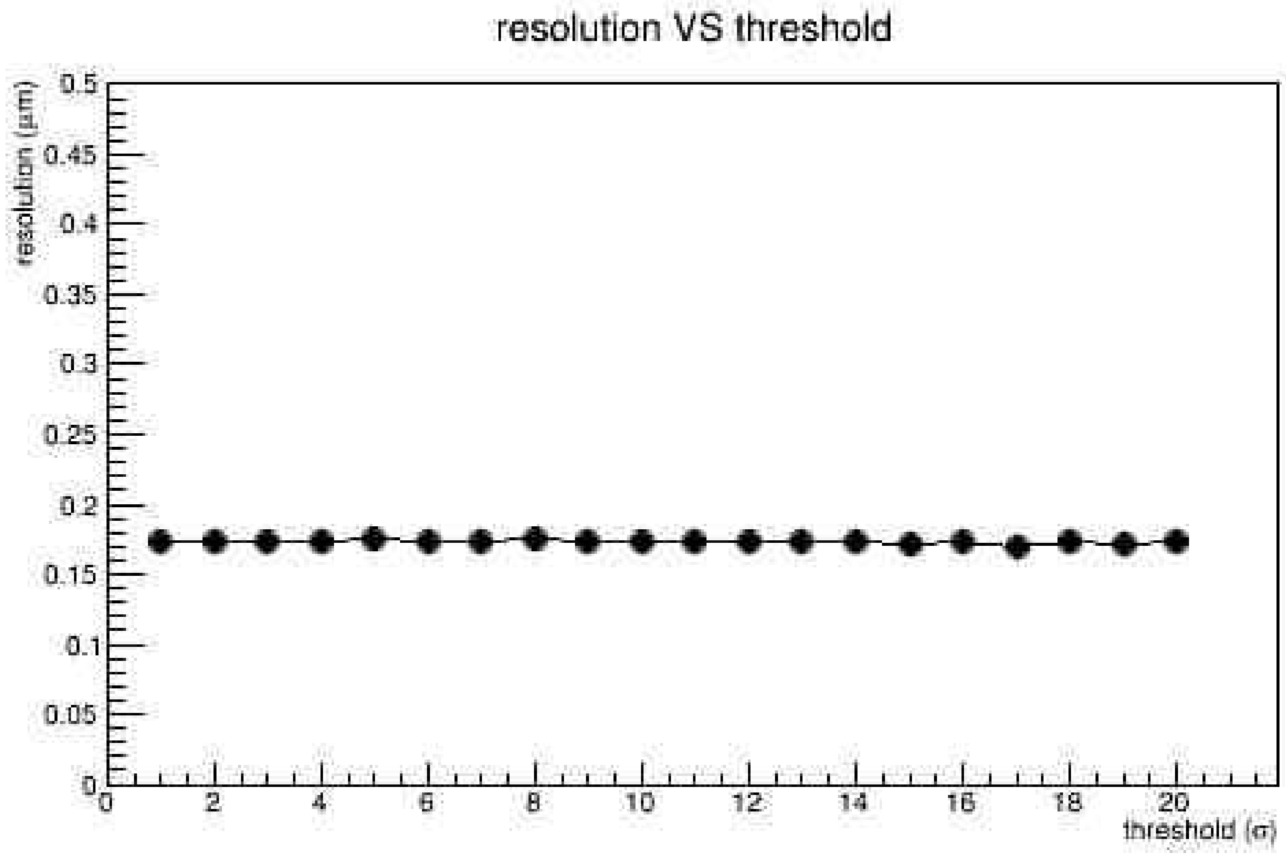


resolution VS pixel pitch
resolution (μm)
0.4
0.35
0.3
0.25
0.2
0.15
0.1
0
5
10
15
20
25
30
pixel pitch (μm)

ADC位数


resolution VS ADC bins of dE
resolution (μm)
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0
500
1000
1500
2000
2500
3000
ADC bins

像素阈值



resolution VS threshold
resolution (μm)
0.5
0.45
0.4
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0
0
2
4
6
8
10
12
14
16
18
20
threshold (σ)

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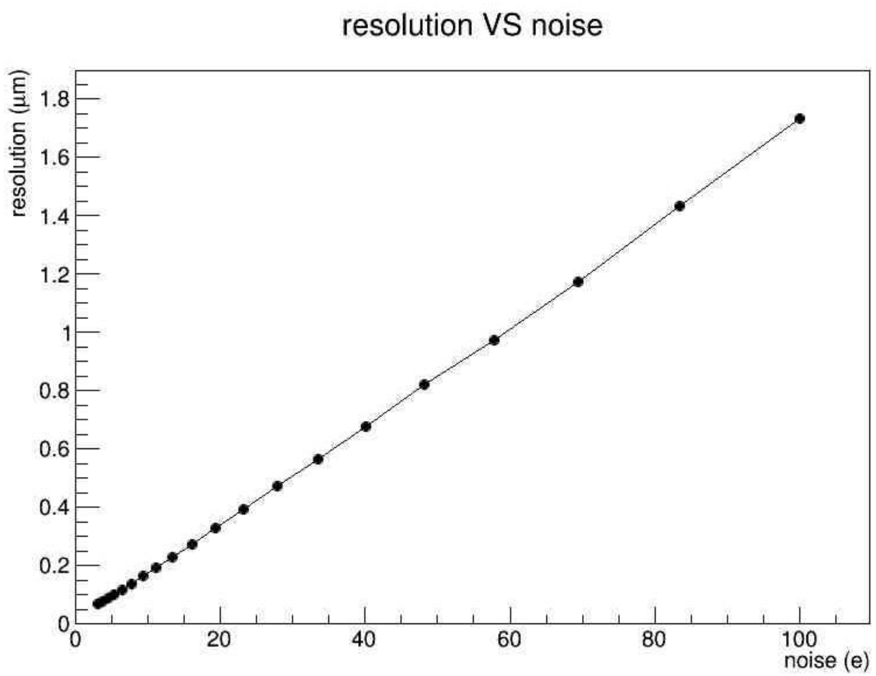
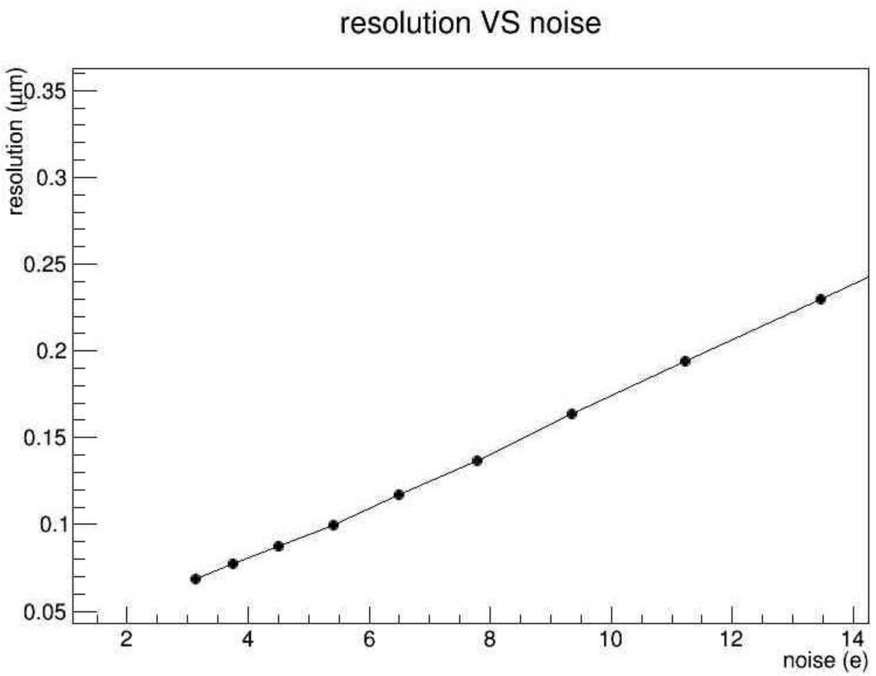
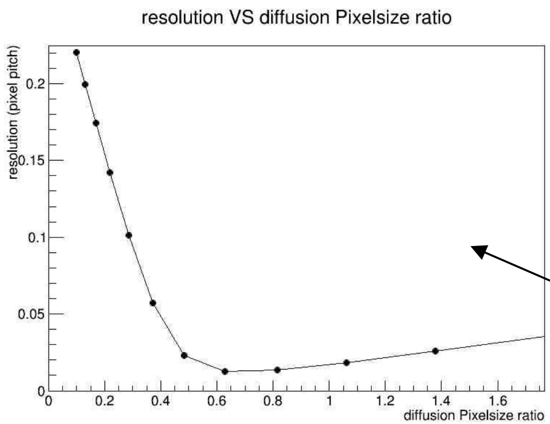
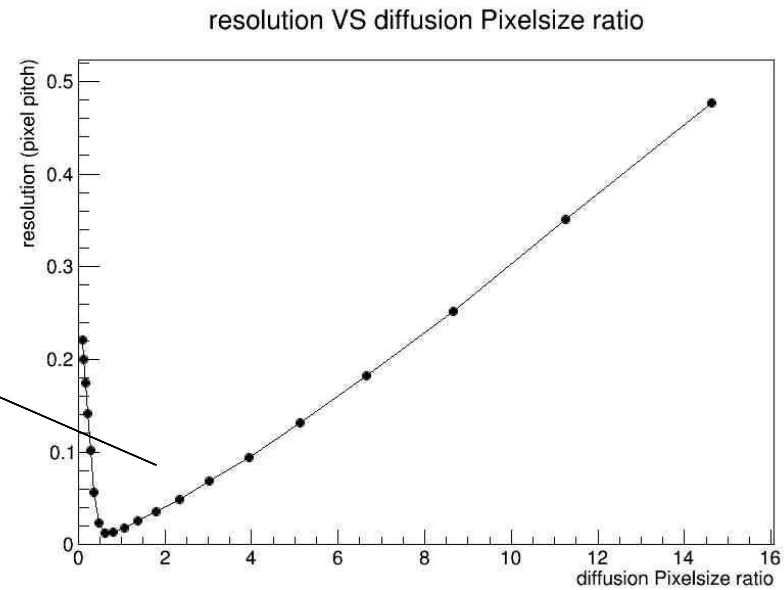
像素噪声

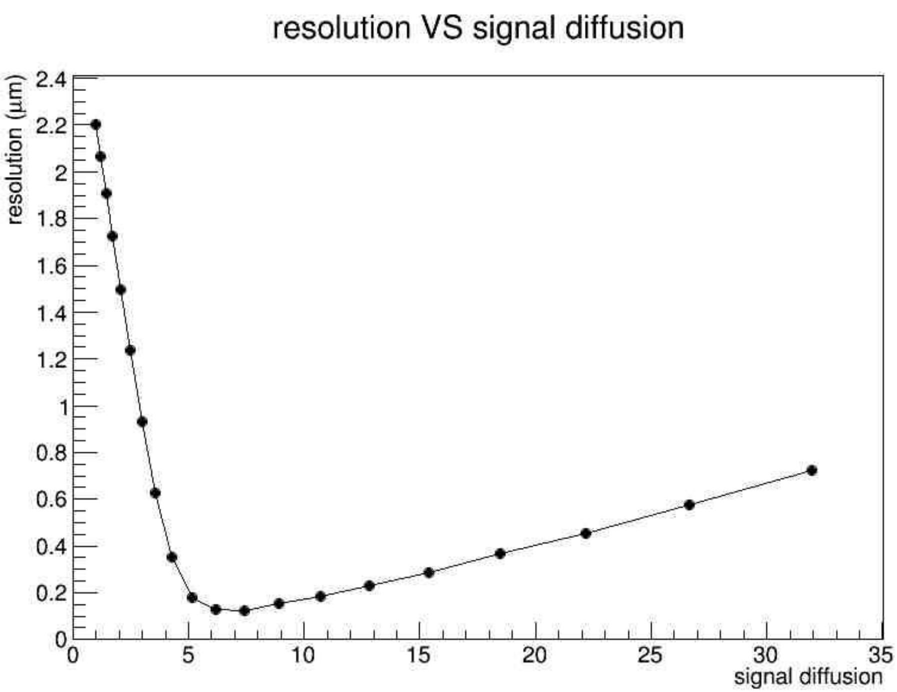

resolution VS noise
resolution (μm)
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
20
40
60
80
100
noise (e)


resolution VS noise
resolution (μm)
0.35
0.3
0.25
0.2
0.15
0.1
0.05
2
4
6
8
10
12
14
noise (e)

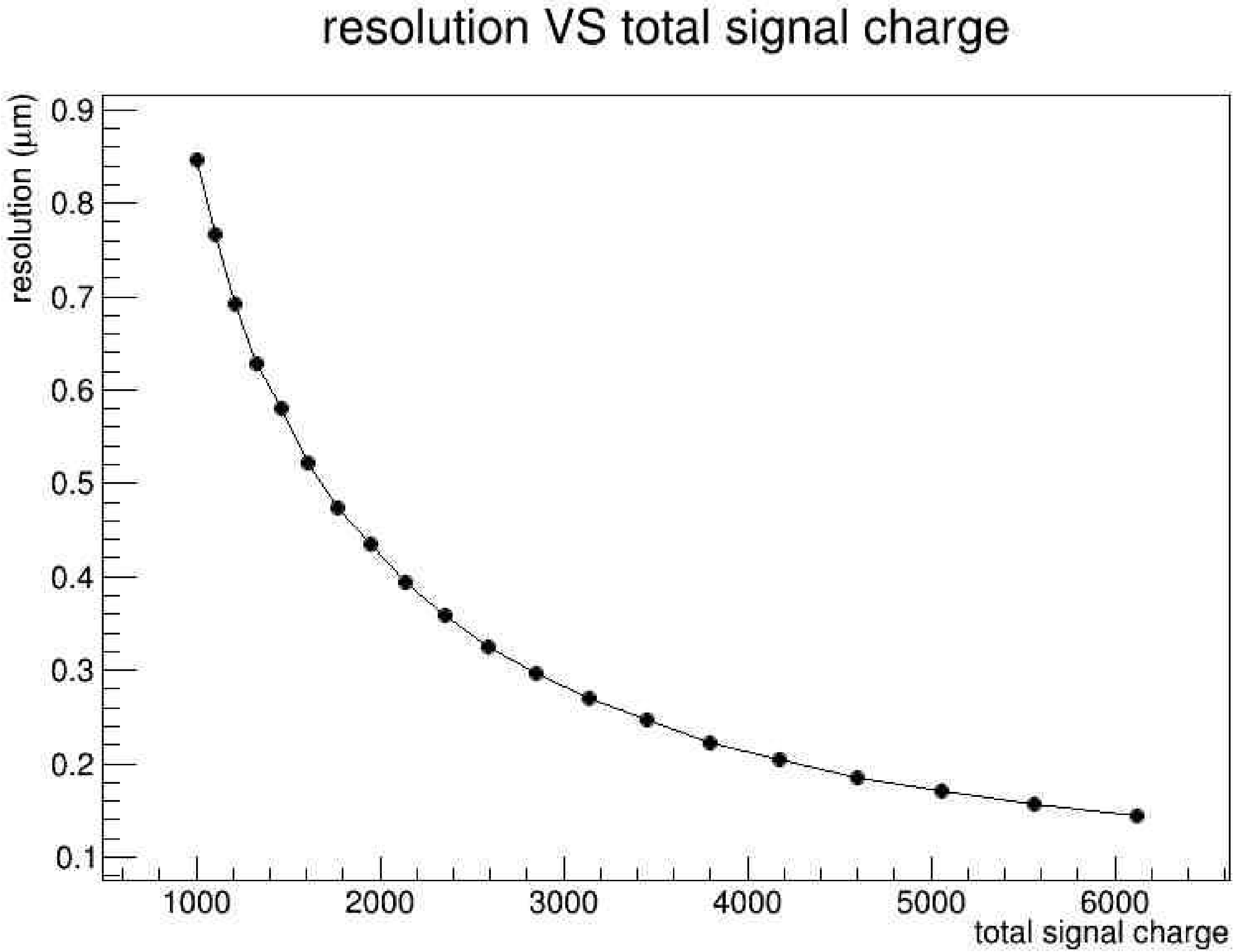
信号扩散


resolution VS diffusion Pixelsize ratio
resolution (pixel pitch)
0 0.05 0.1 0.15 0.2
0 0.2 0.4 0.6 0.8 1 1.2 1.4 1.6
diffusion Pixelsize ratio


resolution VS diffusion Pixelsize ratio
resolution (pixel pitch)
0 0.1 0.2 0.3 0.4 0.5
0 2 4 6 8 10 12 14 16
diffusion Pixelsize ratio


resolution VS signal diffusion
resolution (μm)
0 0.2 0.4 0.6 0.8 1 1.2 1.4 1.6 1.8 2 2.2 2.4
0 5 10 15 20 25 30 35
signal diffusion

信号电荷


resolution VS total signal charge
resolution (μm)
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
1000
2000
3000
4000
5000
6000
total signal charge

束流管层的空间分辨

- 像素大小 10um
- ADC位数 9位
- 像素阈值 3 σ
- 像素噪声 10 e
- 信号扩散 10um
- 耗尽层厚度 60 um

在以上参数时，仿真得到空间分辨可到200nm

但是......

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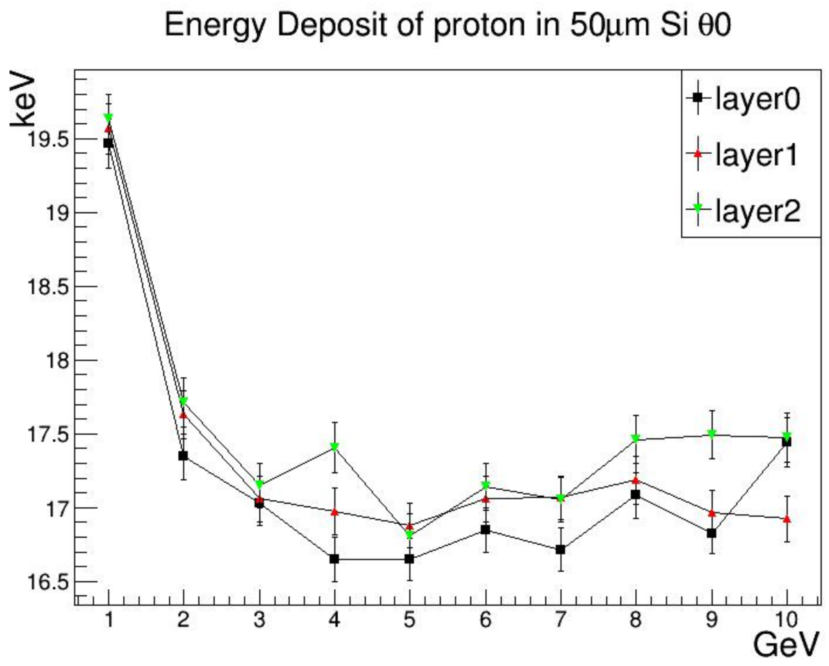
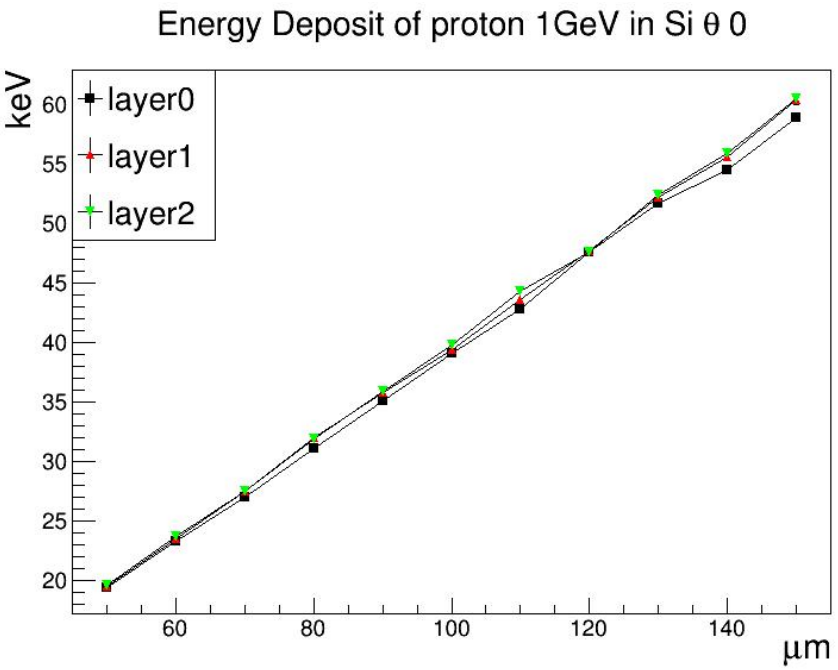
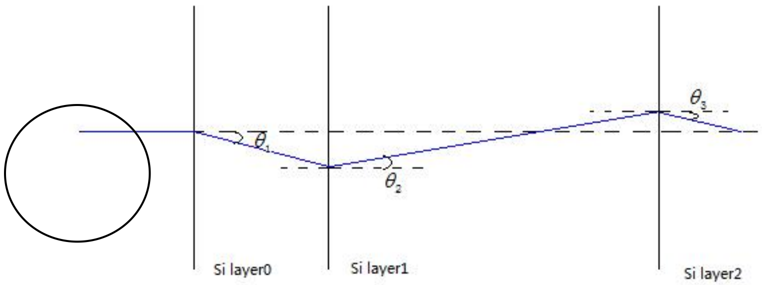
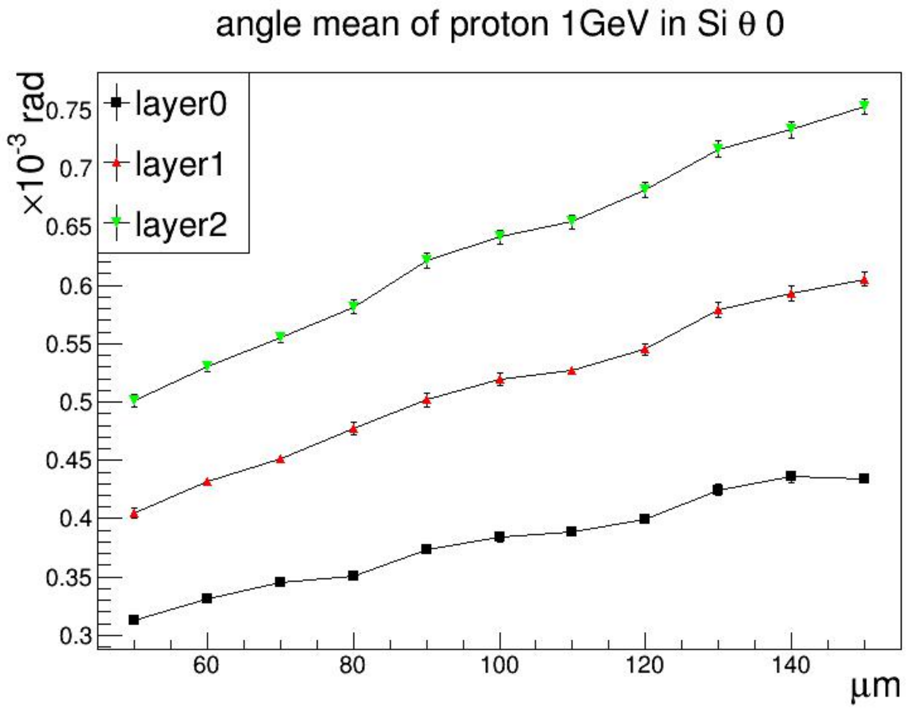
能量损失

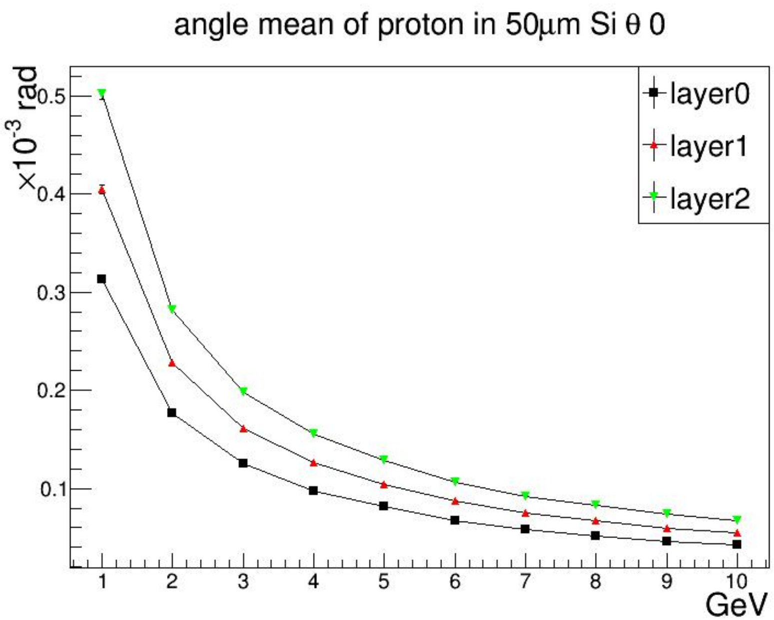

Energy Deposit of proton in 50μm Si θ0
keV
GeV
layer0
layer1
layer2
19.5
19
18.5
18
17.5
17
16.5
1
2
3
4
5
6
7
8
9
10


Energy Deposit of proton 1GeV in Si θ 0
keV
μm
layer0
layer1
layer2
60
55
50
45
40
35
30
25
20
60
80
100
120
140

散射角度







依靠自支撑技术，
可将散射角度减小约
30%

第一层的散射角在1cm距
离上产生2-3um的偏移

谢谢