

TRENDS IN HPC AND DATA CENTER POWER, PACKAGING, AND COOLING

Michael K Patterson, PhD, PE, DCEP

Power, Packaging, and Cooling Intel, Technical Computing Systems Architecture and Pathfinding

Legal Disclaimer

Today's presentations contain forward-looking statements. All statements made that are not historical facts are subject to a number of risks and uncertainties, and actual results may differ materially.

NO LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT. EXCEPT AS PROVIDED IN INTEL'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, INTEL ASSUMES NO LIABILITY WHATSOEVER, AND INTEL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY, RELATING TO SALE AND/OR USE OF INTEL® PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT. INTEL PRODUCTS ARE NOT INTENDED FOR USE IN MEDICAL, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS.

Intel does not control or audit the design or implementation of third party benchmarks or Web sites referenced in this document. Intel encourages all of its customers to visit the referenced Web sites or others where similar performance benchmarks are reported and confirm whether the referenced benchmarks are accurate and reflect performance of systems available for purchase.

Intel processor numbers are not a measure of performance. Processor numbers differentiate features within each processor family, not across different processor families. See www.intel.com/products/processor_number for details.

Intel, processors, chipsets, and desktop boards may contain design defects or errors known as errata, which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Intel, Intel Xeon, Intel Core microarchitecture, and the Intel logo are trademarks or registered trademarks of Intel Corporation or its subsidiaries in the United States and other countries.

*Other names and brands may be claimed as the property of others

Copyright © 2011, Intel Corporation. All rights reserved.



Overview

Data Center Choices IT & HPC Drivers Metrics Power Cooling Density Resources



Data Center Choices

Air cooling vs liquid cooling? Hot-aisle vs Cold-aisle? Raised floor vs concrete? Bricks and mortar vs containers? New building vs existing? UPS as part of HPC? Rack density? Feed from above or below? 1st cost or TCO? Reliability level – Tier 1 To Tier IV?





HPC data centers; many hurdles

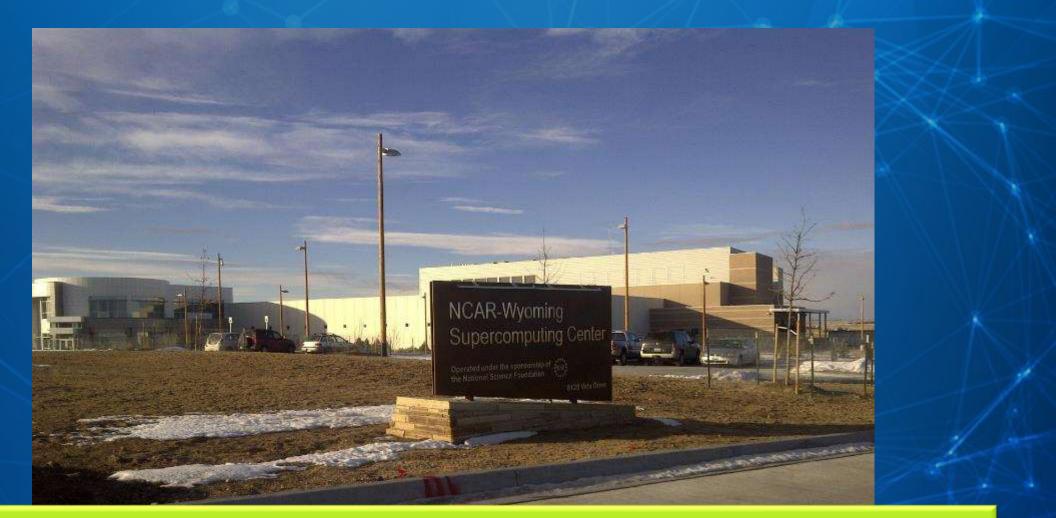
- Power and performance challenges exist to get to Exascale
- *Preparing for Exascale?* Aren't we a little early?
- The key facts...
 - Data Center life cycle 10-15 years
 - HPC cluster life cycle 3-5 years
- Leads to interesting results...

Projected Performance Development

CP 500







NCAR - Home to an Exaflop SuperComputer



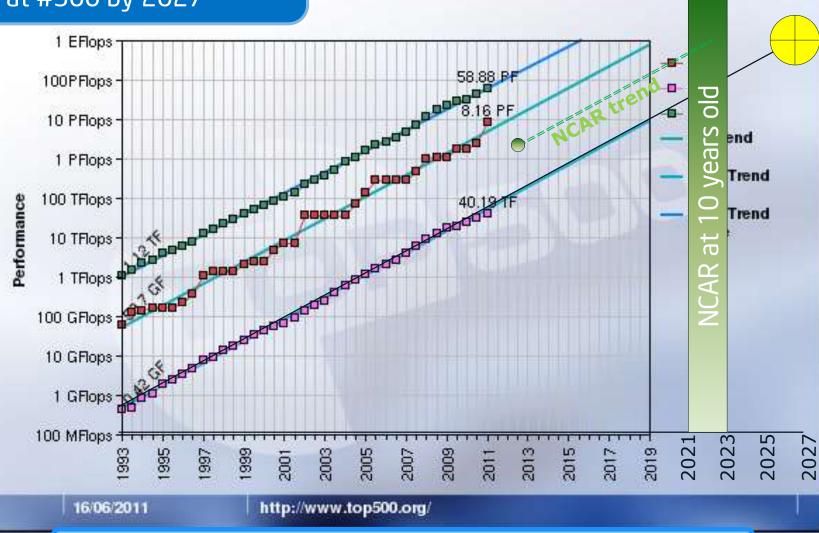
NCAR Yellowstone - New supercomputing center in Wyoming





Exascale at #1 by 2020 NCAR will be 10 years old in 2022 Exascale at #500 by 2027

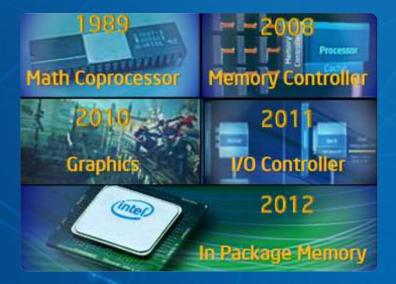
ted Performance Development



Data Centers should be built to last 10-15 years

intel

Integration Enabled by leading edge process technologies





Integrated Today

Possible Tomorrow**

System level benefits in cost, power, density, scalability & performance

**Future options are forecasts and subject to change without notice.



Intel's Scalable System Framework

A Configurable Design Path Customizable for a Wide Range of HPC & Big Data Workloads

Compute

Memory/Storage

Software

Software

Software

Diffuence

Software
Diffuence

Intel[®] Xeon[®] Processors Intel[®] Xeon Phi[™] Coprocessors Intel[®] Xeon Phi[™] Processors

owe

Intel® True Scale Fabric Intel® Omni-Path Architecture Intel® Ethernet

Intel[®] SSDs

Intel[®] Lustre-based Solutions Intel[®] Silicon Photonics Technology Intel® Software Tools HPC Scalable Software Stack Intel® Cluster Ready Program

Intel SSF enables Higher Performance & Density

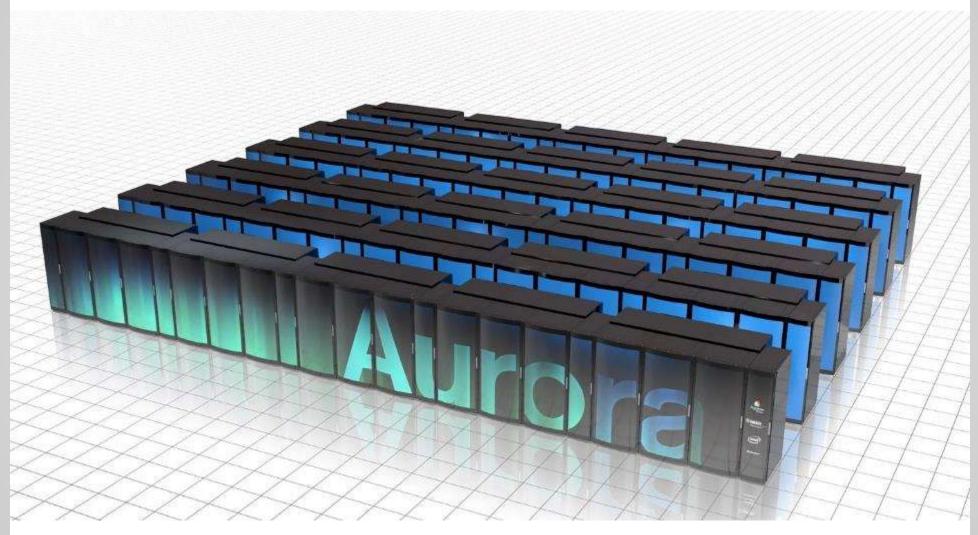
A formula for more performance....

advancements in CPU architecture advancements in process technology integrated in-package memory integrated fabrics with higher speeds switch and CPU packaging under one roof all tied together with silicon photonics much higher performance & density

12



THE FUTURE





The Most Advanced Supercomputer Ever Built An Intel-led collaboration with ANL and Cray to accelerate discovery & innovation

(DOCTOR)

ENLINGY

intel

>180 PFLOPS

(option to increase up to 450 PF)

>50,000 nodes 13MW 2018 _{delivery} 18X higher performance*

>6X more energy efficient* Argonne NATIONAL LABORATORY



Prime Contractor



Subcontractor

Source: Argonne National Laboratory and Intel. *Versus ANL's current biggest system named MIRA (10PFs and 4.8MW) Other names and brands may be claimed as the property of others.

14

Aurora | Built on a Powerful Foundation Breakthrough technologies that deliver massive benefits

Compute

>17X performance[†]

FLOPS per node

>12X memory bandwidth†

in-package memory bandwidth

>30PB/s aggregate

(intel)

inside"

XEON PHI

3rd Generation

Intel[®] Xeon Phi™

Interconnect

2nd Generation Intel[®] Omni-Path

>20X faster[†]

>500 TB/s bi-section bandwidth

>2.5 PB/s aggregate node link bandwidth

File System

Intel®

·l·u·s·t·r·e·

>3X faster[†] >1 TB/s file system throughput

>5X capacity[†]

>150TB file system capacity

Integrated Intel[®] Omni-Path Fabric

Processor code name: Knights Hill

Source: Argonne National Laboratory and Intel *Other names and brands may be claimed as the property of others. [†] Comparisons are versus Mira—Argonne National Laboratory's current largest HPC system, Mira. See Aurora Fact Sheet for details

Intel Confidential — Do Not Forward

Aurora Fact Sheet

System Feature	The Aurora Details	Comparison to Mira
Paak System Performance (R. DPvs)	10C - 47C Paral - 12Pa	OPAN 265
Processor	fung Gernanden, die Pilkern Kritte Kinsesser Die teinensteinen die	Prwei-PC-M 10019, a processes
Kumber of Nodes	(c. 60)	48 1-9
Compute Platform	and system masse on Large Study and generation in	The Cherology
Aggregate High Bandwidth Dn-Peckage Nemory, local Manory and Persistent Nemory	- 5-7 (10) feeding etc.	28° maist
Appreparie High Bendwidth Dh-Package Nemory Bandwidth	. 141.0 "Solverglassic	cate indicarytheories
Bystem Inscreament	24 Serution Fruktimi Fur Aktrices with a seriel-context	BM SD tares in a connect with 2020 pretentes
Interconnect Appregate Node Une Dentwich	KSA Petaloyistis	2 =cm 3,456/5
interconnect Risection Randwidth	settinet 01%	Se Inclusion
intersonne of Interface	vitaj and	magazet
lunst Fuffer Storage	oldF7971r, udity bein 14 and Pri Generaten moR Counciliete Aver Bedane	Som.
Die System	nodel tracine (de Lastier	Landa B. (114), Andrein
Rie System Capacity	• Whather	76 Pohlovas
Rie System Throughput	a Tanhacin	tar Algentan
intel Architecture (Intel® GC) Compatibility	3 %	55
Peak Power Consumption	13 Milliowetts	4.5 Vogewate
RLOP/s Per Watt	· S BLOPS of with	kS GigaRLORisiportuat
Delvery Timeline	2) 9	20-2
Facility Area for Compute Clusters	\$CX x.f.	1.036 (x).0



For further information on Aurora, visit: Intel.com/Aurora.

Because the Because holds on an elementation and the analysis of the Because metal and the determinant of the the system in the second se

	Aurora	
Processor	Xeon Phi [™] Knights Hill	
Nodes	>50,000	
Performance	180 PF Peak	
Power	13 MW	
Space	~3000 sq ft (~280 m²)	
Cooling	Direct Liquid Cooling	
Efficiency	>13 GF/w	

All the details: Aurora Fact Sheet at intel.com

http://www.intel.com/content/www/us/en/high-performancecomputing/aurora-fact-sheet.html?wapkw=aurora

intel

How did we do this?

- In package memory
 - Closer to CPU, stacked memory
- Fabric Integration
 - Package connectivity
- Advanced Switches with higher radix and higher speeds
 - Closer integration of compute and switch
- Silicon Photonics
 - Low cost, outstanding performance but thermal challenges do exist
- All this drives changes



So what have we learned over the last three years? Todays focus is on Power, Packaging, and Cooling (PPC) Metrics

How do we measure and compare?

Power

400Vac, 3ph, >100 kW / cabinet for the very high end

Packaging

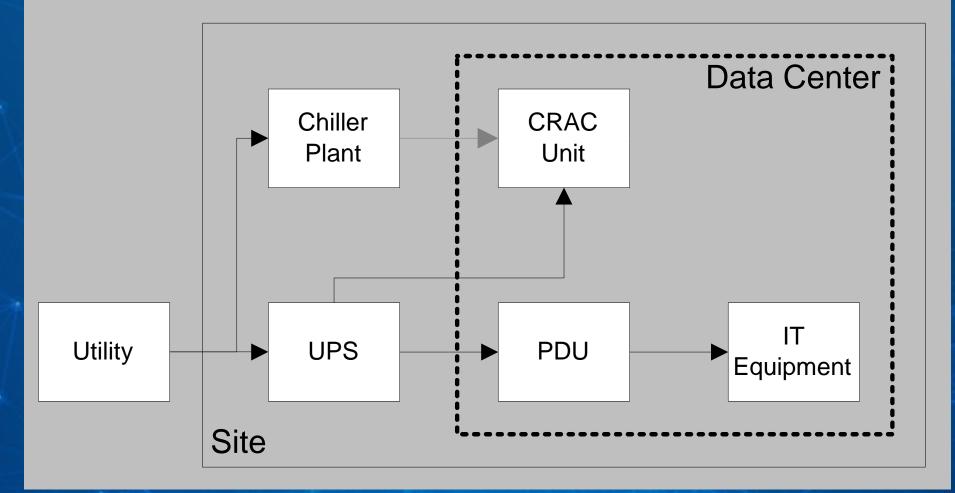
- High density computing significant computing in a small package
- Weight becomes a key design parameter

Cooling

- Liquid cooling; good for some. Cooler is better, to a point
- Aurora ~100% liquid cooled
- Air cooling still very core to HPC



The Data center





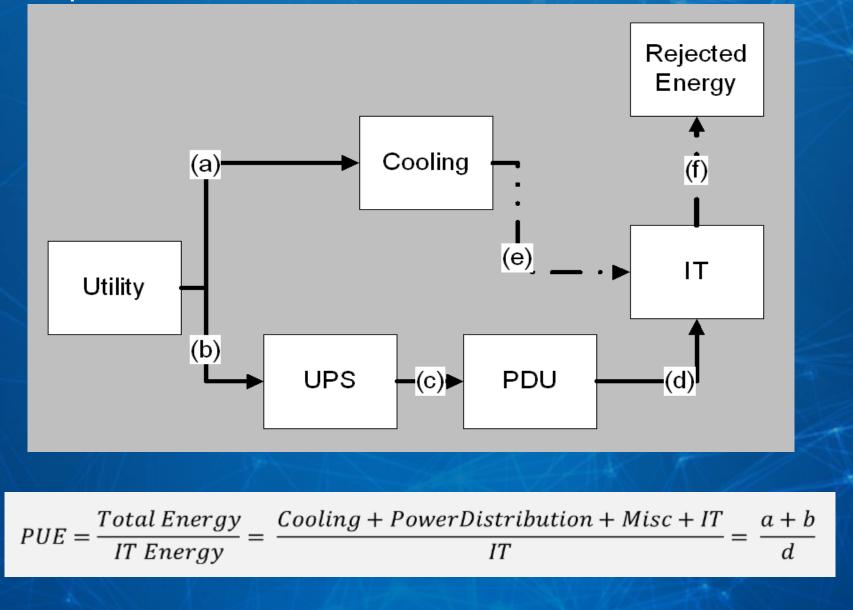
 $PUE = \frac{Total \ Data \ Center \ Annual \ Energy}{Total \ IT \ Annual \ Energy}$

- Introduced in 2006 by Malone and Belady
- Developed and agreed to by EU Code of Conduct, DOE, EPA, Green Grid, ASHRAE, etc...
- Has led Energy Efficiency drive in Data Centers
 - PUE Average in 2007 ~ 2.5
 - Best in Class 2016:

NREL= 1.06, LRZ= 1.15, NCAR~1.2, ORNL= 1.25, TU Dresden < 1.3



PUE – simple and effective



(intel)

PUEs: Reported and Calculated

	PUE
Global bank's best data center (of more than 100)	2.25
EPA Energy Star Average	1.91
Intel average	>1.80
Intel Jones Farm, Hillsboro	1.41
ORNL	1.25
T-Systems & Intel DC2020 Test Lab, Munich	1.24
Google	1.16
Leibniz Supercomputing Centre (LRZ)	1.15
Containers	1.1-1.6
National Center for Atmospheric Research (NCAR)	1.10
Yahoo, Lockport	1.08
Facebook, Prineville	1.07
National Renewable Energy Laboratory (NREL)	1.06



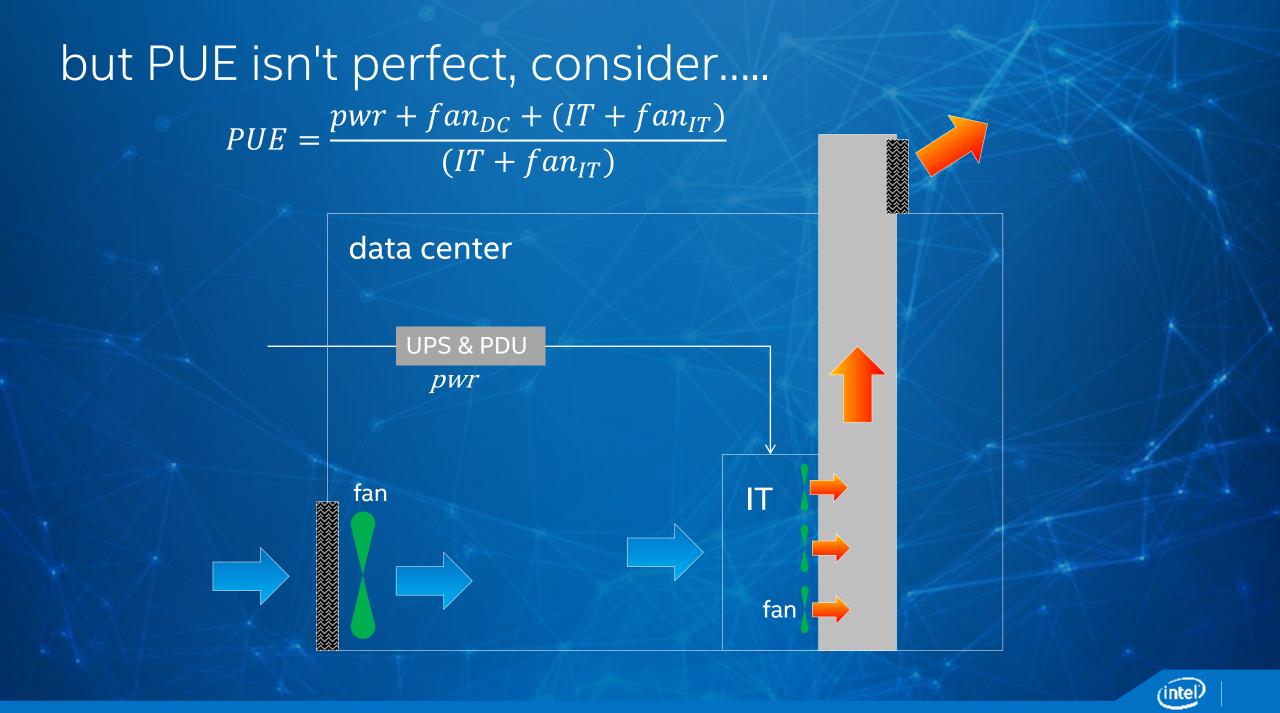
PUEs: Reported and Calculated

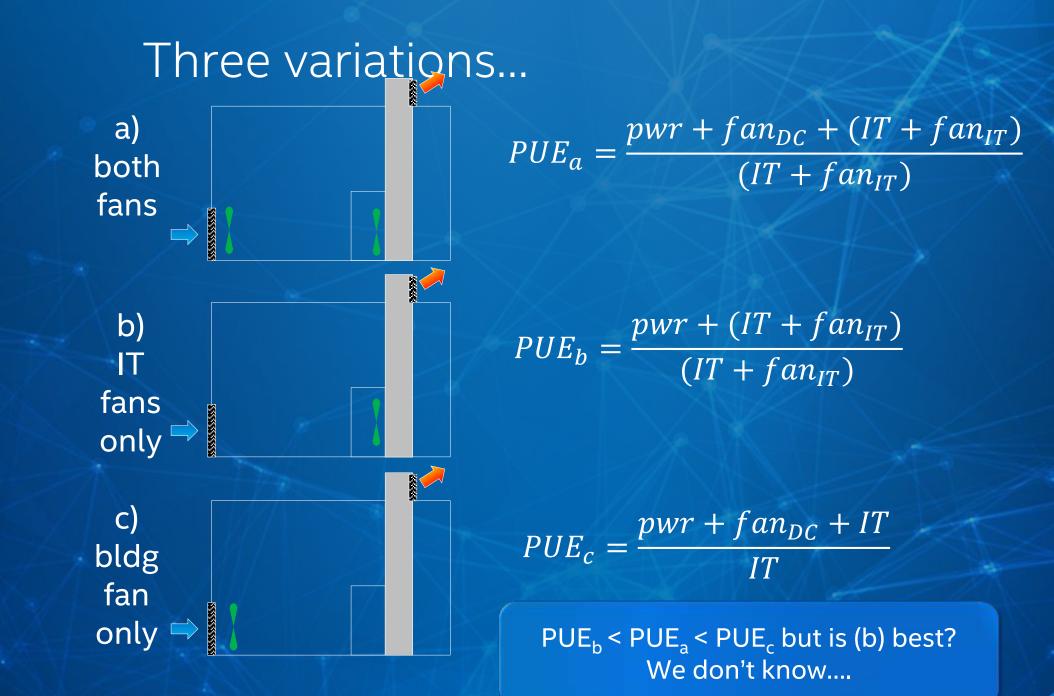
Global bank's best data center (of more than 100)

Liquid cooling is required for density, but not necessarily for efficiency

effi		ficiency
EPA Energy Star Average		,
Intel average	>1.80	
Intel Jones Farm, Hillsboro	1.41	A-FC
ORNL	1.25	LC
T-Systems & Intel DC2020 Test Lab, Munich	1.24	A-FC
Google	1.16	A-FC
Leibniz Supercomputing Centre (LRZ)	1.15	LC
Containers	1.1-1.6	
National Center for Atmospheric Research (NCAR)	1.10	LC
Yahoo, Lockport	1.08	A-FC
Facebook, Prineville	1.07	A-FC
National Renewable Energy Laboratory (NREL)	1.06	LC





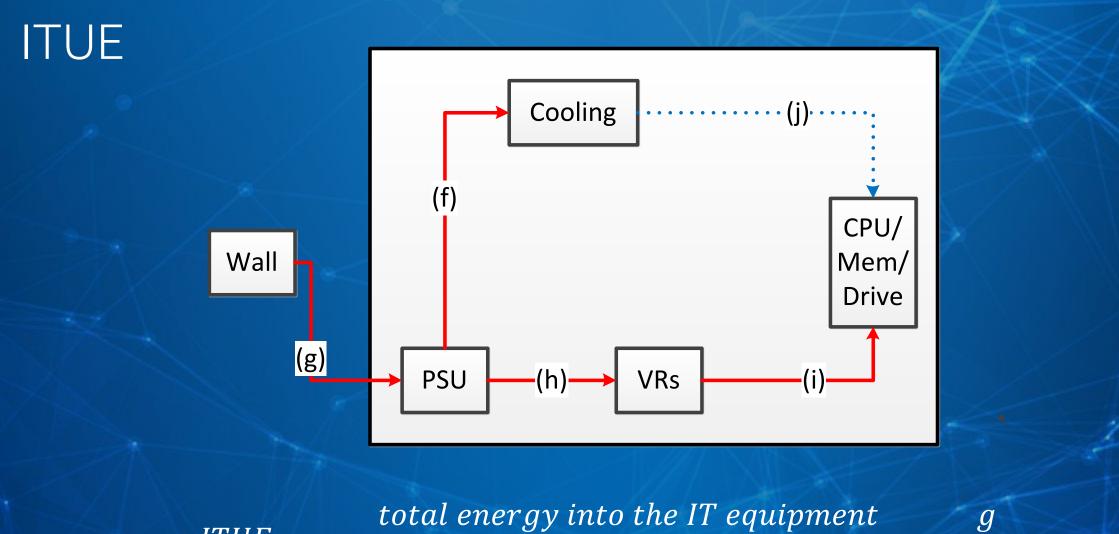


(intel)

Can we define a "server-PUE"? Maybe ITUE?

$PUE = \frac{Total \ Energy}{IT \ Energy} = \frac{Pwr + Cooling + Misc + IT}{IT} = \frac{Infrastructure \ Burden + IT}{IT}$				
I OL – IT Energ	y = IT	IT		
	Data Center	Server		
	Data Center	Server		
Power dist losses	UPS, line losses, PDUs	PSU, VRs, board losses		
Cooling losses	Chiller, CRAC, Pumps, Fans	Fans, Pumps		
Misc losses	Security, Lighting, Building Control	Indicators, Platform Control		
IT	Servers, Storage, Network	Processor, Memory, Disk		
$ITUE = \frac{Infrastructure \ Burden + Compute}{Compute} = \frac{Pwr + Cooling + Misc + Compute}{Compute}$				
$ITUE = rac{Total Energy into the IT Equipment}{Total Energy into the Compute Components}$				
Total Energy into the Compute Components				





 $ITUE = \frac{total \ energy \ into \ the \ IT \ equipment}{total \ energy \ into \ the \ compute \ components}$



The next step...

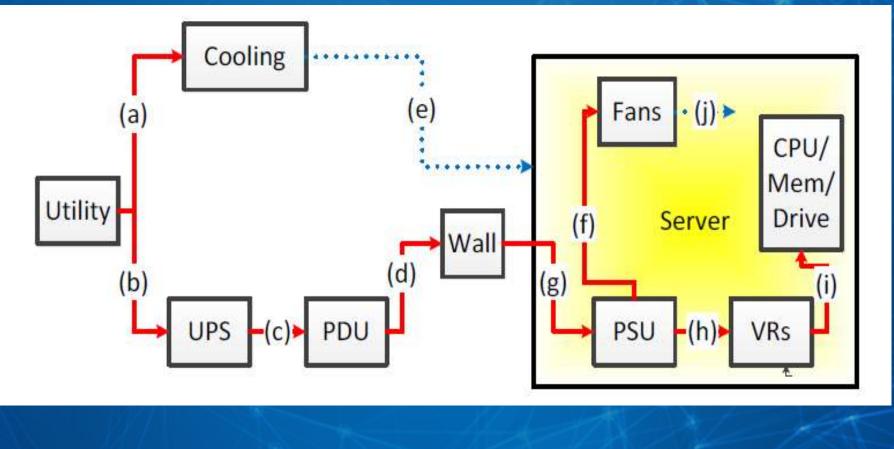
PUE and ITUE are both:

- dimensionless ratios
- Represent the burden or "tax" of infrastructure
- "1" is ideal, values larger than 1 are worse
- Values less than 1 are not allowed
- So why not:

$TUE = PUE \ x \ ITUE$

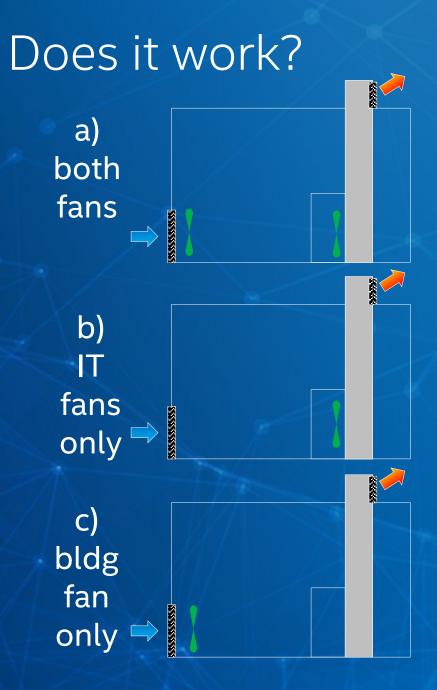


TUE



$$PUE = \frac{Total \ Energy}{IT \ Energy} = \frac{a+b}{d} \qquad ITUE = \frac{Total \ Energy}{Compute \ Energy} = \frac{g}{i}$$
$$TUE = ITUE \times PUE = \frac{a+b}{i}$$

(intel)



 $TUE_{a} = \frac{pwr + fan_{DC} + fan_{IT} + compute}{compute}$

 $TUE_b = \frac{pwr + fan_{IT} + compute}{compute}$

 $TUE_{c} = \frac{pwr + fan_{DC} + compute}{compute}$

The lowest TUE yields the lowest energy use. <u>Yes, it works!</u>

ITUE / TUE

TUE, a new energy-efficiency metric applied at ORNL's Jaguar

Michael K. Patterson^{1,4}, Snephen W. Poole^{1,4}, Chung-Haing Hua^{1,4}, Don Maravell¹, William Tichnah^{1,4}, Henry Coles^{1,4}, David J Martiner^{1,4}, Nardie Estes¹

¹Intel Architecture George Dated Corporation, Duports, Washington, URA and Howell, N., performanced in Acad. 2009 Disk Right National Linkowsey, Oak King, Terranous, USA, ¹Jarrennon, Berlaufer, National Laboratory, Bookeley, Colliberata, URA ¹Stando Havinonal Laboratory, Altogrampic, Now Mexico, URA ¹Stando Havinonal Laboratory, Altogrampic, Now Mexico, URA ¹Stando Herico Barding, Group, Andrones Inland, Washington, URA ¹Stando PRC Working Group, Andrones Inland, Washington, URA

Abstracts. The sensity, Posser Usage Efficationswa (FUR), has been momentar in improving mergy officiency of data minim, but it is not particle. This shall beings to that FUE does not account for the proceed statistication and cooling losans made TT apapteent. This is particularly problematic in the HPC doubt performance mengating space where sprints appliers are moving coolings, and power independent of the channer. This paper proposes two new mericits (TUE 03 power many difficultiences), which we FUE has "mainted" the FT and TUE inside power many effectivenessi, which we FUE has "mainted" the FT and TUE inside power many effectivenessi, which we fuels the result of the state of the channer. This paper proposes two new mericits (TUE inside power many effectivenessi, which we fuels the transfer owney picture. We conclude with a demonstration. The provides a state of state range (instant) and minimal support nearing main suffice specific mergy sum is the INC. TUE can also be a summaring in COSA's in the C on the IC and the specific means for comparing IMC of our in the C on

Keywards: HPC, snngs-efficiency, nettia, data contri

1 Introduction

This Wairepaper is a collaboration effort of the Matrice name of the Energy Efficient BPC Webbarg Group (2223)PC Webbarg end to be a source and insues with Power Usage Efficiences (PR2) and explores source of the group to the matrix. It discoverables the matrix, applies the same imple logic to the IT, and fase to the utakis, including the IT and Informations. This methodology is shown to produce two new metrics, with the logics is lower being a combination of POE and F-power usage affectiveness (TTE), yielding totic power mage effectiveness (TTE). These new matrix can be used to understand the series energy use from the utility to the liftic start or the starts of the two starts of the start of the starts of the start of the starts of the starts of the start of the starts of

atla p. 1, 2011 E foroger Veing Dette Vasieberg 2011

- Paper available
 email me or from ISC 13
 Best Paper Award at ISC
- Use the metric!
 Ask for projected ITUE in future procurements
 - Good cluster to cluster efficiency comparison
 - Begin to develop monitoring strategy
- Be aware of limits
 - Does not include workload / output
 - Difficult to use on older machines
 - Don't ask for everything; likely to expensive



Power

- Trends in the very high end....
- Power now 480 Vac 3ph (400 Vac in Europe)
- >100 kW / cabinet
- In-cabinet 380 Vdc for optimized delivery
- Power management and power monitoring allows optimized performance and efficiency
- More typical HPC
 - 400 Vac 3ph, 230Vac 1ph
 - 48 Vdc in the rack can reduce weight, cost, and size

HVDC (380 Vdc) is an option; primary reasons why are 1st cost and renewables



Power Delivery Challenges in the horizon

Variable Power Cap

- Several reasons
 - Peak Shedding
 - Reduction in renewable energy

Power rate of change

 Ex: Hourly or Fifteen minute average in platform power should not exceed by X MW.

Controlled Power Ramp up/down – economic or technical issues

 Challenge to do this at a reasonable cost and with energy efficient mechanisms



Power

Europe primary power

- 400 Vac 3ph
- High density racks could use 3ph, 1ph if not high power; better options for PSUs (PUE/ITUE)
- Likely that most storage and system racks would do well on 230 Vac 1ph
- Consider rating schemes for equipment (PSU): Platinum, Gold, Silver, etc... (ITUE)
- Board power: same direction, higher cost components very often have a good ROI (ITUE)

UPS (Uninterruptable power supply)

- Generally HPC would rather spend money on compute than UPS, generally European power quality is good enough without
- Please don't use UPS for power quality reasons. 😕 Also they waste 2-5%. (PUE)
- Do use UPS and redundant feeds for fabric and storage and service nodes Power Management
- Tools available, must be built for the site needs



Packaging

Rack and cluster weight and density

- Strong correlation between weight and power
 - Some studies have shown kg/kW is ~constant across rack size
 - Goal is to reduce this ratio

Packaging

 High density computing – network topology optimization and high node count per rack (lots of power) make for dense cabinets

Rack weight density

■ Design limit: Floor tiles at 500 lbs/sf ~ 2500 kg/m2 for high end. 🙁 …more than many DCs

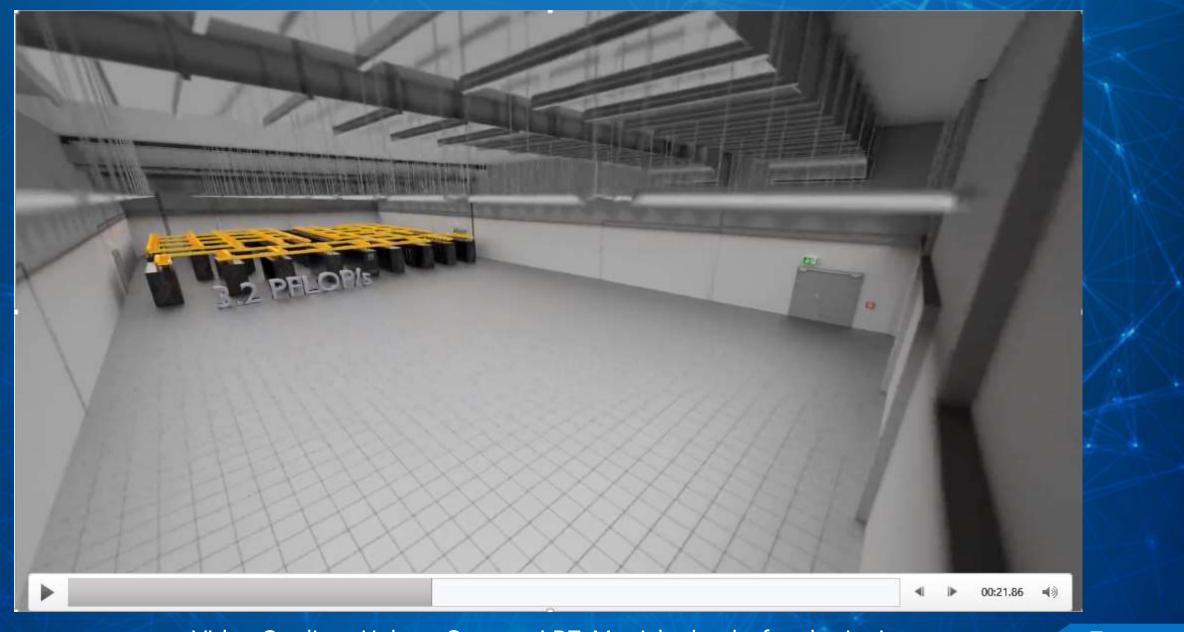
White space vs utility space

- Compute density increasing, infrastructure support equipment is not
- What's the trend for machine room area?



I must need a huge data center for PetaScale and ExaScale computing – Right?





Video Credit to Helmut Satzger, LRZ, Munich, thanks for sharing!

(intel



Do I need a huge data center?



- Facility area for Compute Cluster does not have to be huge. Significant compute density in small packages
 - At Aurora density, the 3.2 LRZ PF fits in 5 m²
- Don't forget:
 - If Storage is going to be large then you will need additional floor space.
 - If you are going to be using Xeon instead of Xeon Phi then you may need additional floor space
 - Utility & infrastructure space continues to grow

Rack density (kW/rack & kg/m2) have a wide range of choices, but the local data center may restrict these





Why liquid? Why Air? Power per node continues to rise Rack density limits airflow path But air-cooling can cost less Increased thermal performance of liquid (vs air) allows more free-cooling Thermal resistance from chip to liquid in a cold plate is smaller than chip to air over a heat sink

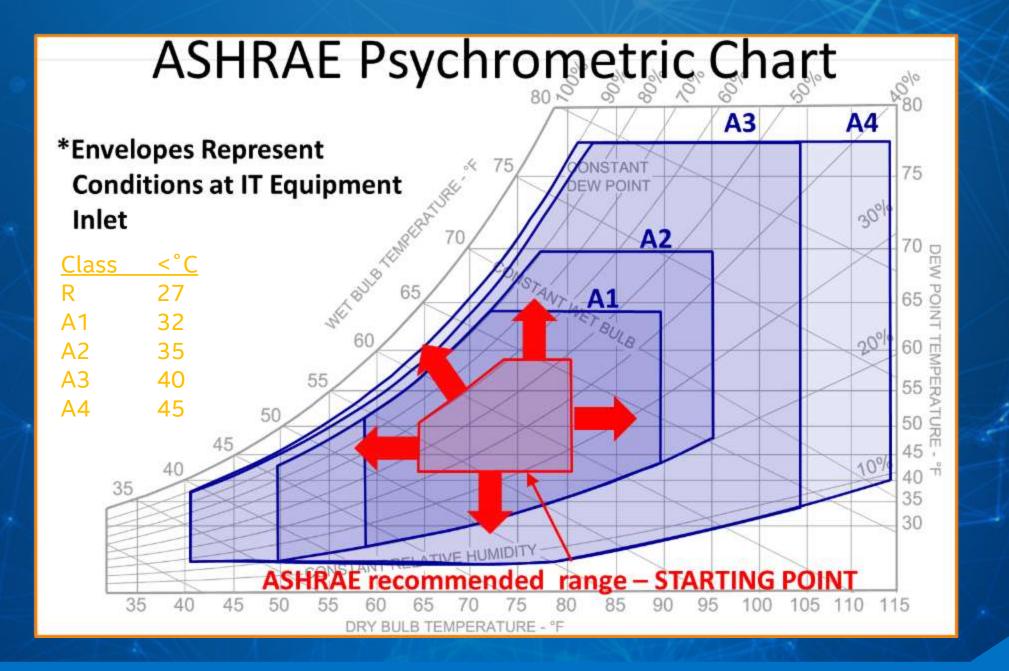


Cooling

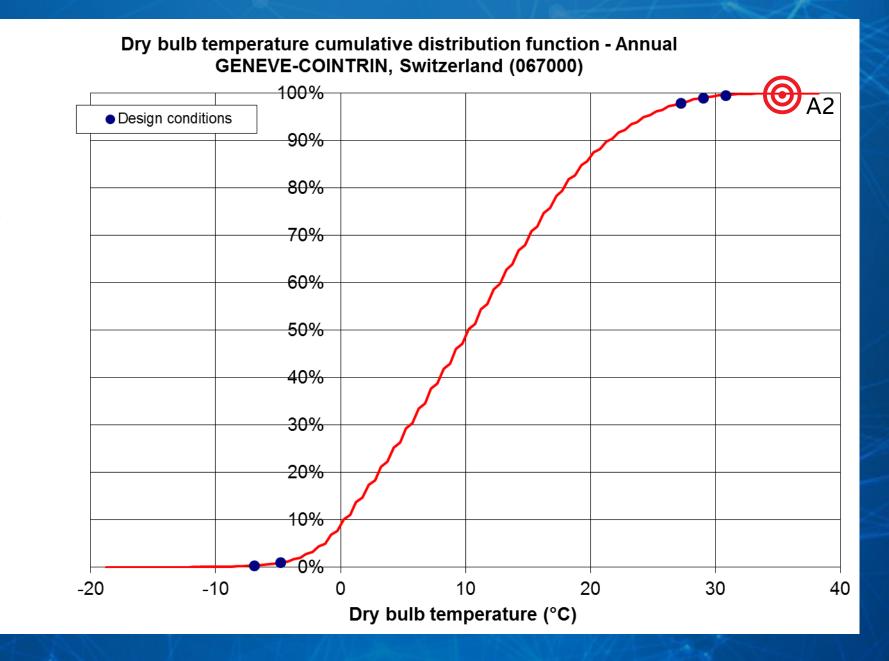
Air Cooling

- ASHRAE A1 thru A4
- Containment a "must" for good PUE and low TCO
- Hot Aisle and Cold Aisle an operational choice, not an efficiency choice
- Free –air cooling should always be checked for applicability
 - Corrosion a real issue depending on air-quality
- Air-Cooling limits rack density, but good performance density can still be had
- If you do air-cooling in a new data center; the VERY FIRST MOST IMPORTANT consideration is to design the building around the airflow path. Get that done, then bring in the building architects. ⁽²⁾





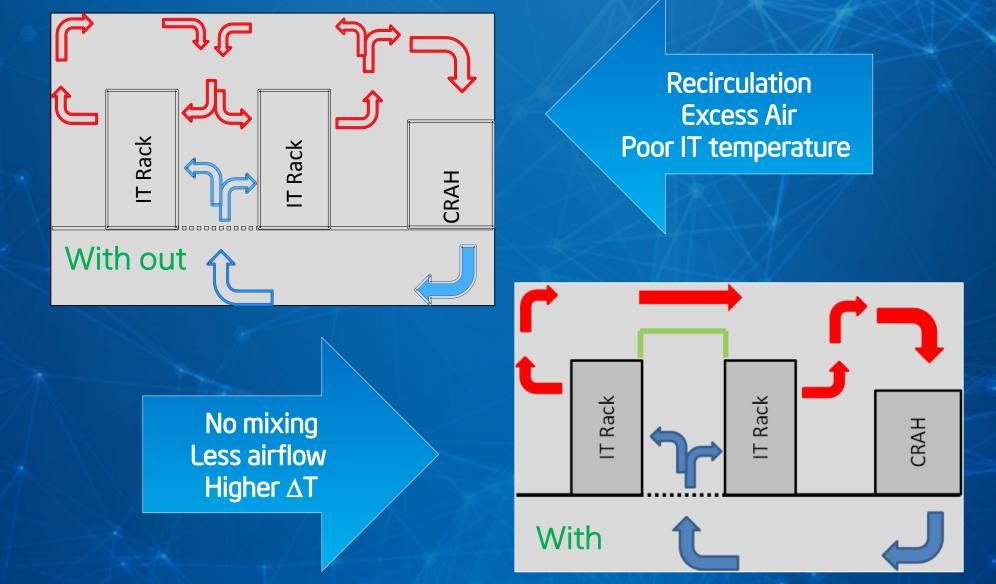




Cumulative distribution function (fraction)



Why containment?





Airflow management is the number one tool in your toolbox for data center improvement – it can solve more problems than any other tool!

CERN cold aisle containment

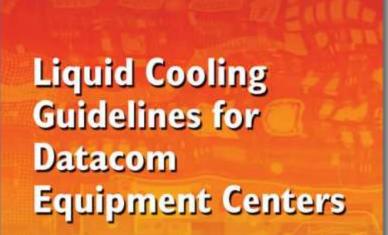


Cooling

Liquid Cooling

- ASHRAE W1 thru W4
- Many different varieties, they have VERY different performance, cost, and efficiency results
- Water quality is an important issue
 - Consult ASHRAE guide; monitor!
- Immersion cooling is not on our roadmap, we still keep current but issues exist
 - Oil immersion
 - Two-phase immersion
- Liquid cooling can offer better performance, better reliability
 - High density systems (Aurora, etc, are fully liquid cooled)





ASHRAE Datacom Series

American Society of Heating, Refrigerating and Air-Conditioning Engineers, Inc.

All ASHRAE work has been incorporated into the 2nd Edition.

Tip: 2nd Edition now available for purchase in the ASHRAE bookstore.

More important tip: Chap 5 covers Facility water (FWS) Chap 6 covers IT loop water (TCS) These are very different! Specify the right water.

intel

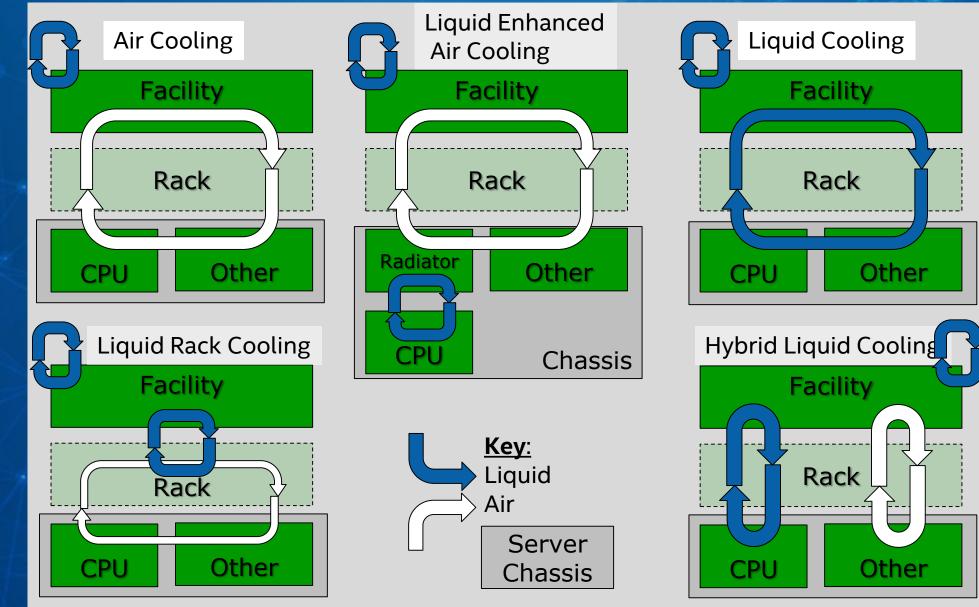
2011 ASHRAE Liquid-Cooled Thermal Guidelines

	Classes	Typical Infrastructure Design		Facility Cumply	IT Faulinment
0		Main Cooling Equipment	Supplemental Cooling Equipment	Facility Supply Water Temp (C)	IT Equipment Availability
	W1 Chille	Chiller/Cooling	Water-side	2 – 17	Now available
	W2	Tower	Economizer Chiller	2 – 27	
	W3	Cooling Tower	Chiller	2 – 32	Becoming
	W4	Water-side Economizer (with drycooler or cooling tower)	Nothing	2 – 45	available, dependent on future demand
	W5	Building Heating System	Cooling Tower	> 45	Not for HPC

Required Cooling Infrastructure: Balance of Silicon/Datacenter



System Definitions – all different, all about how close the liquid gets to the components



(intel)

Liquid Cooling Technologies

Local Coldplate Node-Level Pumpwith Remote Coldplate Coldplate Pump Degree of change from our air-cooled mind-set Ability of the solution to pick up all the energy





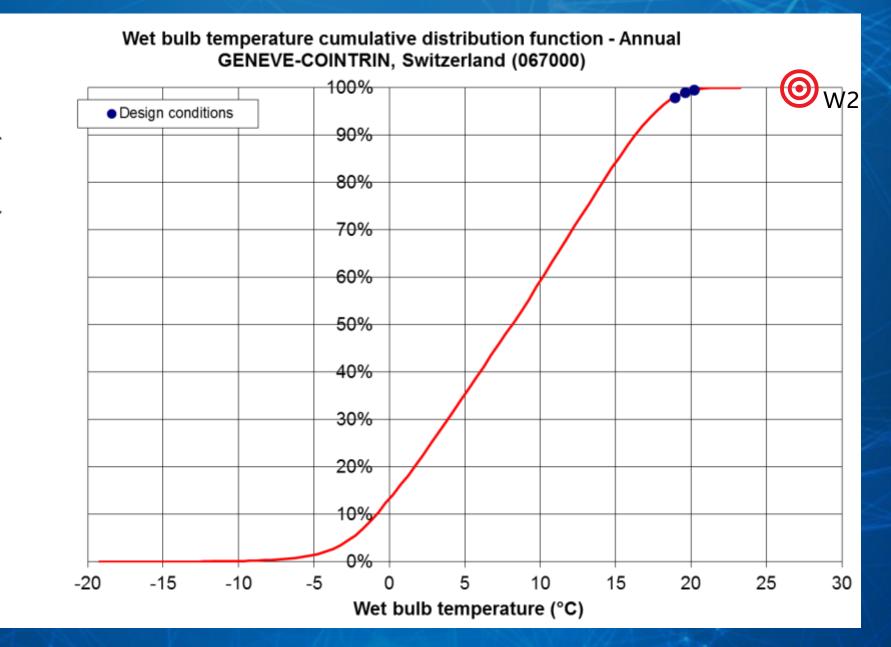


A proposal....

- As a starting point, use the coolest water you can make without a chiller
- Always be above the dewpoint (to prevent condensation in the machine)
- Cooler temperatures promote:
 - Lower leakage
 - More turbo frequencies
 - Higher stability
 - More time to recover in an upset condition
 - Better reliability
 - Reduced flow rates

Note - May consume more water, not applicable if after heat recovery





Cumulative distribution function (fraction)

(intel)

ASHRAE

TC 9.9 Committee http://tc99.ashraetcs.org/

Books

https://www.ashrae.org/resources-publications/bookstore/datacom-series

EE HPC WG

http://eehpcwg.llnl.gov/

Hot for Warm Water Cooling

http://eetd.lbl.gov/sites/all/files/publications/lbnl-5128e.pdf

The Green Grid

http://www.thegreengrid.org/

http://www.thegreengrid.org/en/Global/Content/Tools/NAme ricanFreeCoolingTool

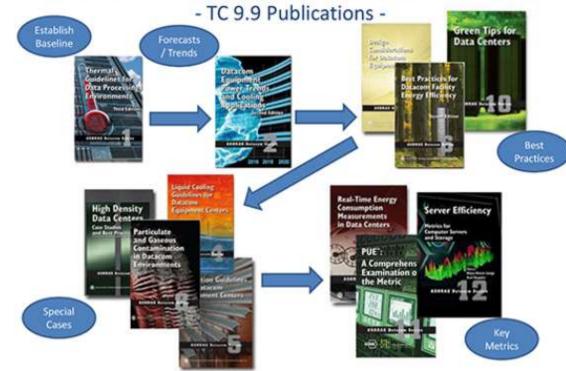
EU Code of Conduct for Data Centres

http://iet.jrc.ec.europa.eu/energyefficiency/ict-codesconduct/data-centres-energy-efficiency

Datacom Series

The Datacom Series provides a comprehensive treatment of data center cooling and related subjects, authored by <u>ASHRAE Technical Committee 9.9</u>, Mission Critical Facilities, Data Centers, Technology Spaces and Electronic Equipment.

A Roadmap for Improving Data Center Energy Efficiency



Summary

- Data Center Design is straightforward, but can be daunting if not fully understood, unfortunately still very site-dependent
- Resources are available!
- Modular build out is best; plan for the end state, provision just for today
- PPC for HPC
 - Power delivery at higher voltages with less redundancy than Enterprise
 - Density has value, but Packaging can challenge most data centers
 - Air and Liquid Cooling have their place, choose the right one for performance and value





Thanks for your attention

Questions?

michael.k.patterson@intel.com



Intel®

