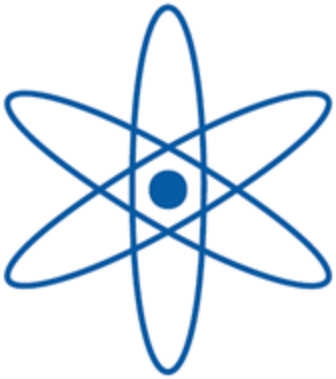
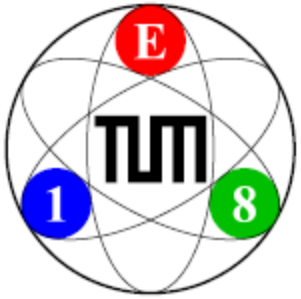





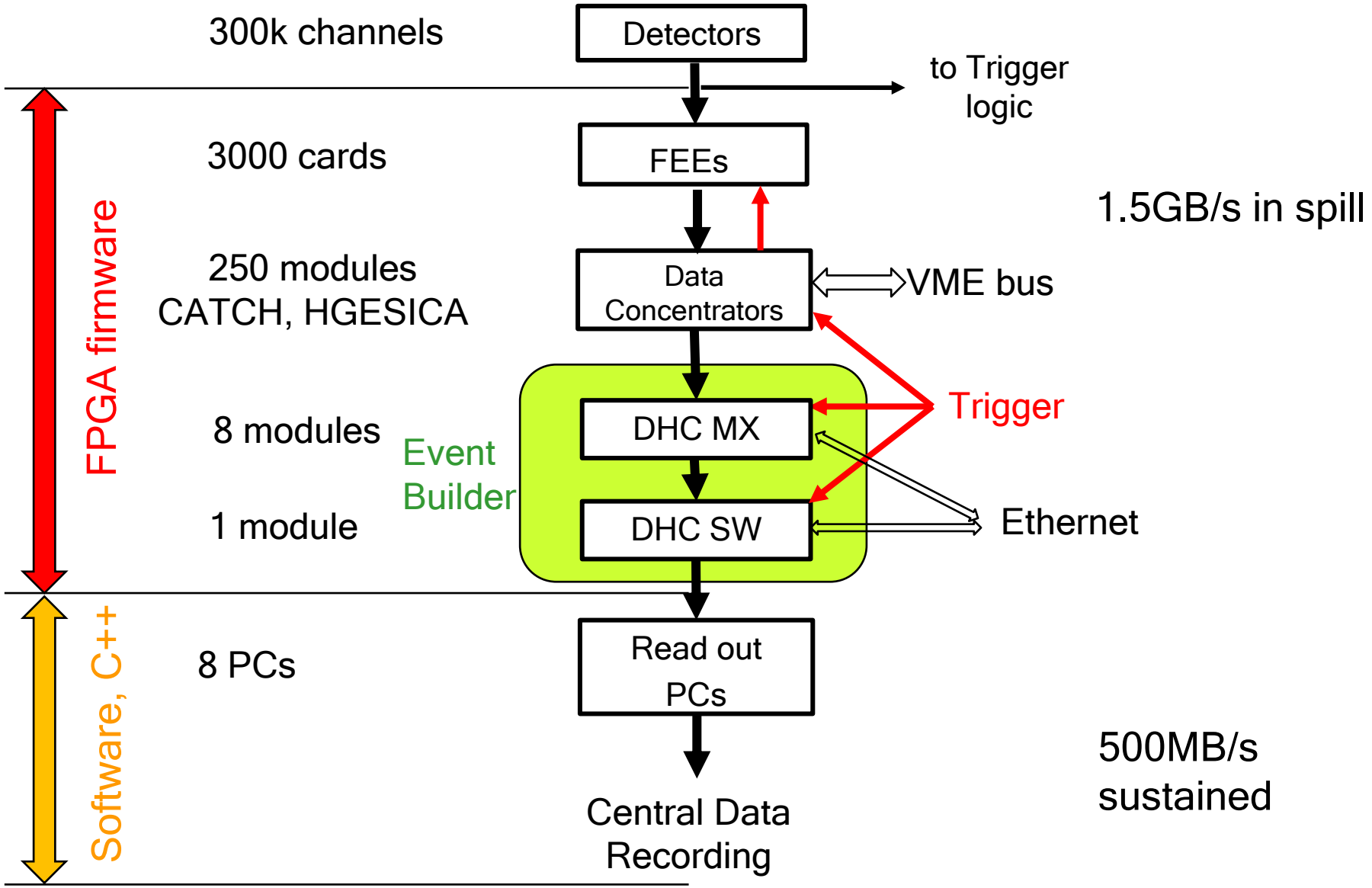

# FEEs and DAQ options for COMPASS after 2020

Igor Konorov

**Workshop**

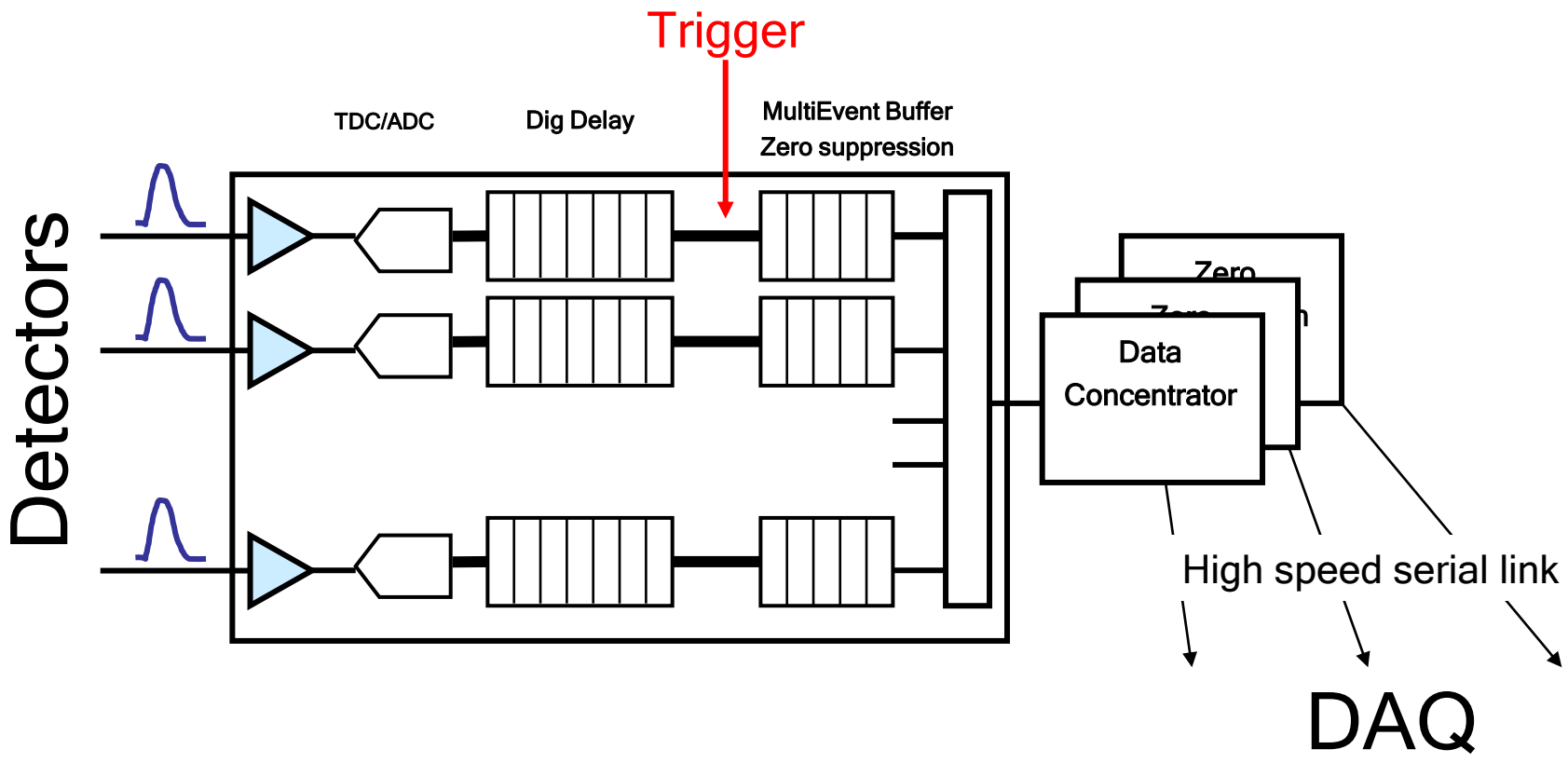
Geneva, March 21-t 2016

# COMPASS DAQ


300k channels
Detectors
to Trigger logic
3000 cards
FEEs
1.5GB/s in spill
250 modules
CATCH, HGESICA
Data Concentrators
VME bus
FPGA firmware
Trigger
8 modules
Event Builder
DHC MX
1 module
DHC SW
Ethernet
Software, C++
8 PCs
Read out PCs
500MB/s sustained
Central Data Recording

# Front-End architecture

First run : 2002

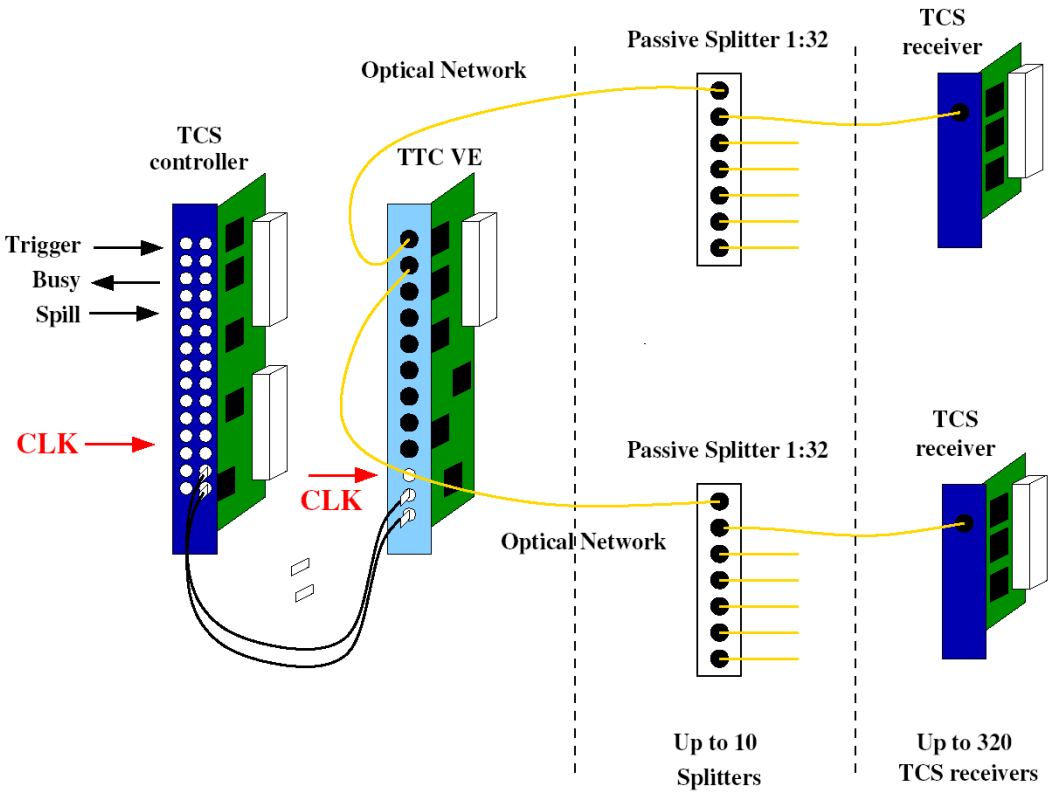



FEE Performance :

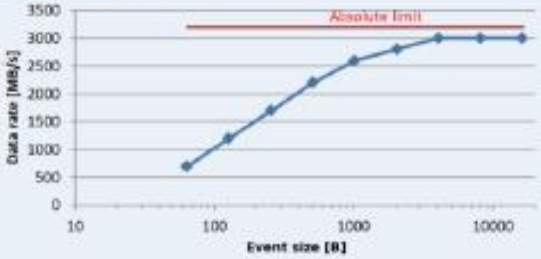
- Trigger rate 40kHz
- Maximum trigger latency 2 us
- 2 % dead time due limited size of derandomization buffer

# Trigger Control System

- Passive Optical Network
- 38.88 MHz Clock provision
- Trigger and Event ID
- 300 destinations



# DAQ modules

| AMC module | |
|---|---|
| ○ form factor: | AMC standard → ATCA compatible |
| ○ FPGA: | Virtex6 XC6VLX130T |
| ○ memory: | 4 GB DDR3 SDRAM |
| ○ firmware: | • DHCmx 12:1 multiplexer<br>• DHCsw 8x8-switch<br>• DHCsb PCIe spillbuffer |
| ○ data rate: |  |



| VME carrier card | |
|---|---|
| ○ form factor: | 6 U VME |
| ○ interfaces: | • TCS (Trigger Control System) receiver<br>• 1 Gb Ethernet for control network (IPbus)<br>• 16 serial data links (SLINK)<br>• JTAG for backup programming of FLASH |

| PCIe carrier card | |
|---|---|
| ○ interfaces: | • TCS receiver<br>• 1 Gb Ethernet for control network (IPbus)<br>• serial data link (SLINK)<br>• PCIe for DMA |

# Detector Summary table

| Detector type | # of channels | Required out electronics | |
|---|---|---|---|
| Calorimeters ECAL0, ECAL2 | 4.800 | 12b ADC@80MHz | |
| Calorimeters HCALs, ECAL1 | 2.200 | 10b ADC@80MHz | |
| Micropattern detectors | ~100.000 | APV ASIC | |
| RICH, MWPC | 60.000 | APV ASIC | |
| RICH, MAPMT | 12.000 | F1 TDC | |
| SciFi | ~2.600<br>? | F1 TDC<br>GANDALF TDC | |
| Beam Momentum Station | 640 | F1 TDC | |
| Hodoscopes, VETO | 500 | F1 TDC | |
| Wire Chambers | ~60.000 | F1+FPGA TDC | |
| Recoil Detector | 96 | 14b ADC@0.5(1.0)GHz | |

# FEE&DAQ features and limitations

- VME bus used for FEE configuration (30 VME crates)
- Time, Trigger and event identification information distributed via Passive Optical Network – Star topology (1-> 300)
- Event size 50k Bytes
- maximum trigger rate of 40kHz limited by FEE buffer sizes and links' bandwidth
- 2us maximum trigger latency limited by TDC multi-event buffer
- Analogue trigger logic
- 32GB of memory in Event Builder allows to store entire spill and average data rate over whole SPS cycle
- In spill data rate of 1.5 GB/s
- Average data rate 500 MB/s
- Event Builder performance up to 3GB/s sustained
- Readout speed of online computers 120 MB/s/pc => 1GB/s

# Upgrade requirements

- Digital trigger using FPGAs or online PC farm
- Front-ends with additional data stream to trigger logic
  - Any detector can be included in the TRIGGER
- Trigger latency > 4 us
- Trigger rate > 80kHz
- Or trigger less readout with Software High Level Trigger
- Migration from VME bus to Ethernet⇔FPGA interfaces

# Upgrade scenario 1

## Scenario I, 80kHz trigger rate

- Digital Trigger : hodoscopes, VETO, BMS, SciFi, ECALs (optional)
- New TDC FE cards with trigger data streams => exchange F1 FEEs
- TDC cards compatible with existing preamplifier and discriminator cards – no need to change Preamplifier-Discriminator cards
- Keep APV readout but upgrade ADCs to 80kHz trigger rate (GEM, Silicon)
- New Sampling ADCs for ECAL1, HCAL1 and HCAL2 SADC
  - Two links for DAQ and TRIGGER
- Remove CATCH and HGESICA,
- FEE connected directly to DHCmx (Event builder)

## Data rate

1.5GB/s in spill => 3 GB/s in spill

No hardware upgrade of DAQ needed

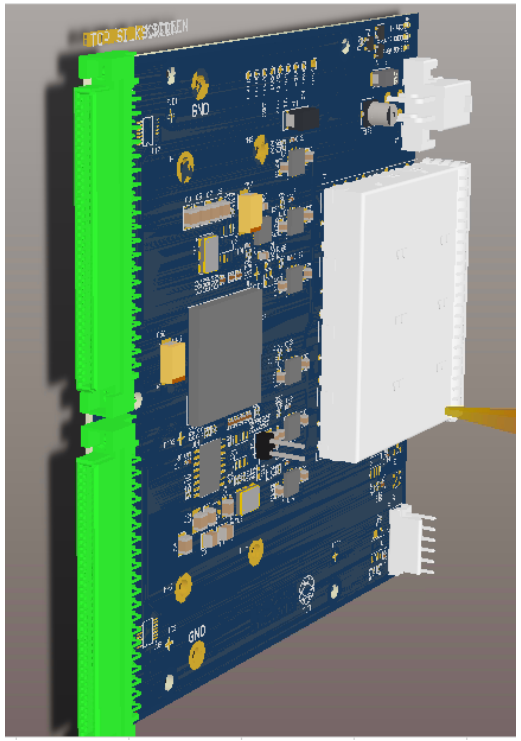
May require upgrade of Online Computers

## Advantage:

Flexible approach of continuous upgrade

# New TDC card development

- 64 LVDS channels
- ARTIX 50 FPGA
- Time bin 800 ps
- Optional Scaler for every channel
- 4 high speed links 3Gb/s



3 flavors:

- MWPC
- DC
- SciFi
  - 32 channel
  - 200-400ps bin
  - down to 70 ps resolution

Cost optimized:

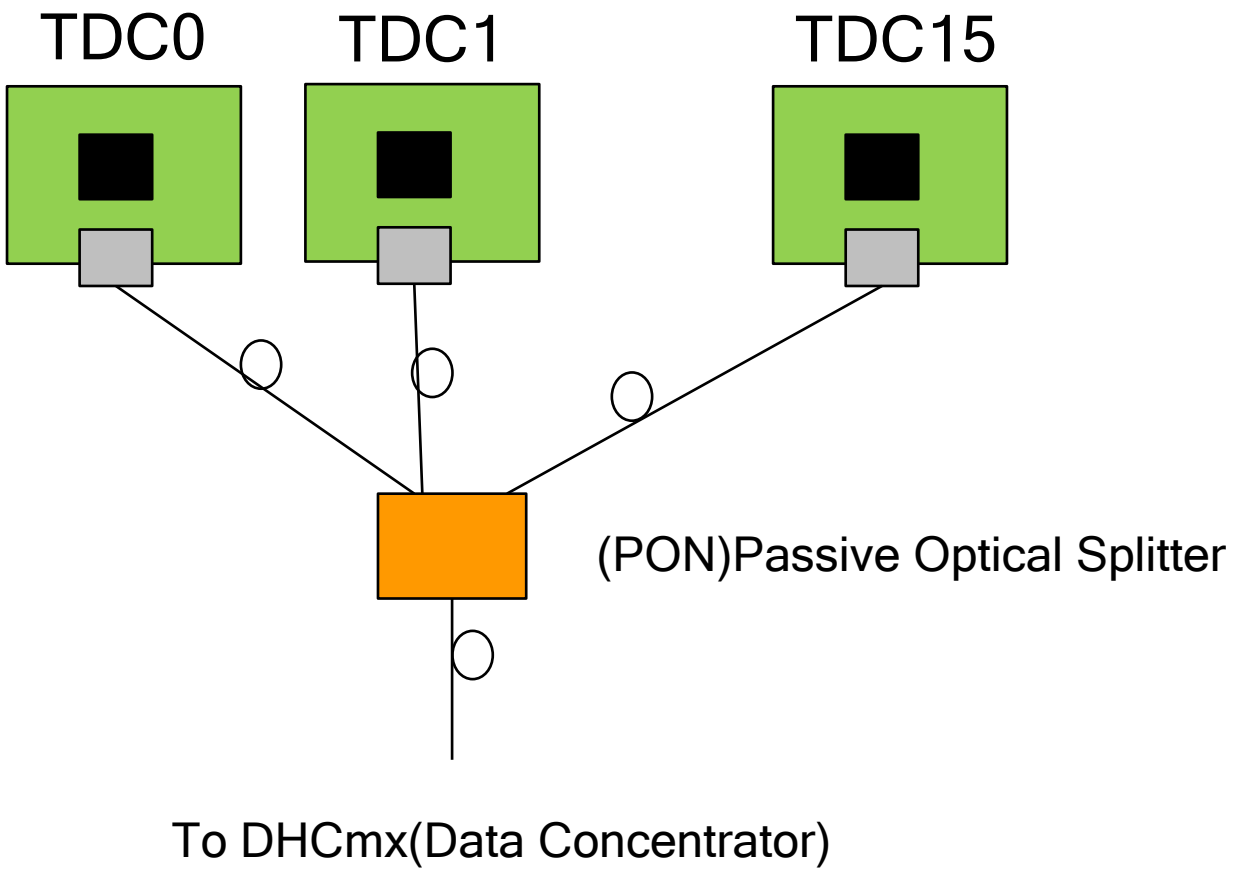
- 5 €/channel for wire chambers
- Up 20 €/channel for SciFi, BMS, Hodoscopes

Readout features:

- Expected maximum data rate of 3MB/s @100kHz and 20% occupancy
- Compatible with trigger less read out

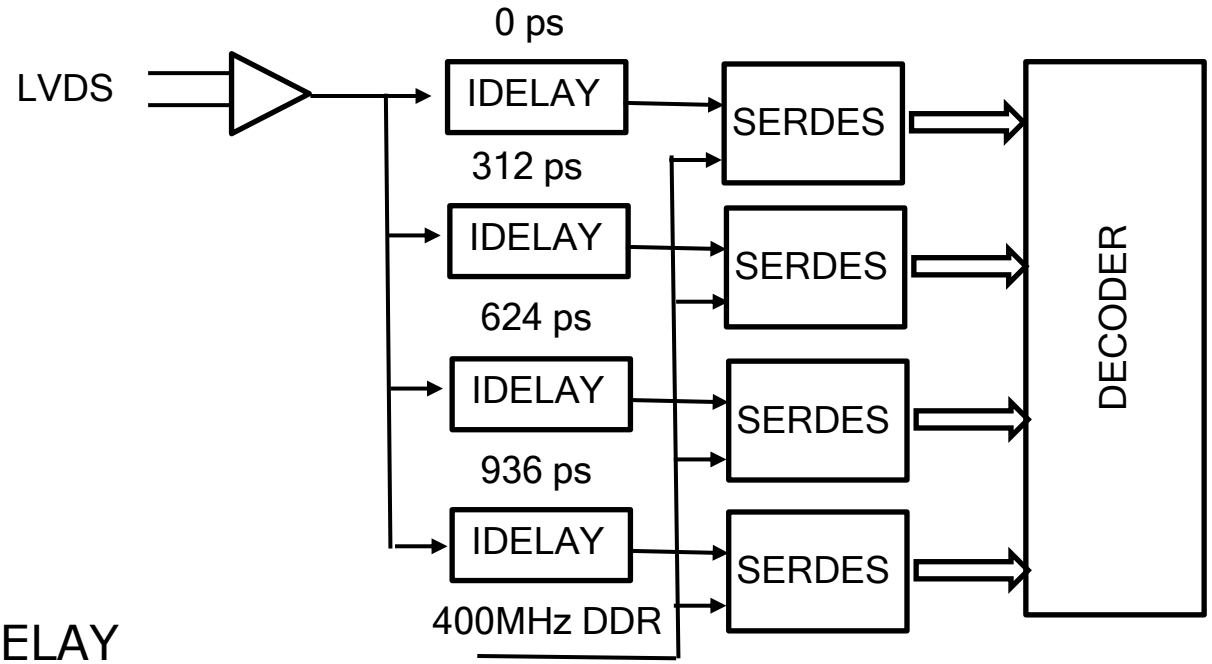
# TDC readout architecture

- Time division readout
- Single fiber : TCS , Ethernet, Data transmission => UCF protocol



# TDC prototype tests(Virtex 5)

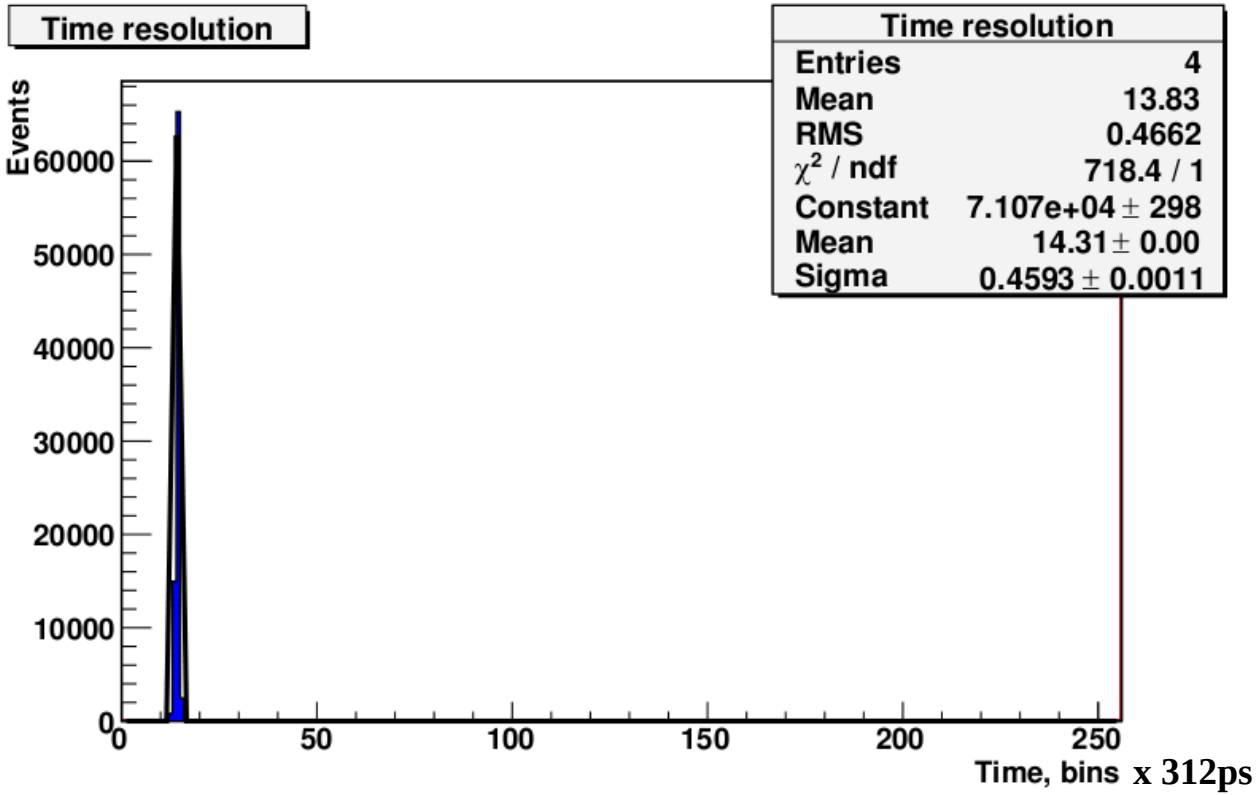
- TDC design using built-in SERDES hardware cores




- IDELAY
  - 64 taps, 78 ps/tap
  - Calibrated and independent from process, temperature and voltages
- Bin size 312 ps
- Auto calibration at power up – tuning IDELAY

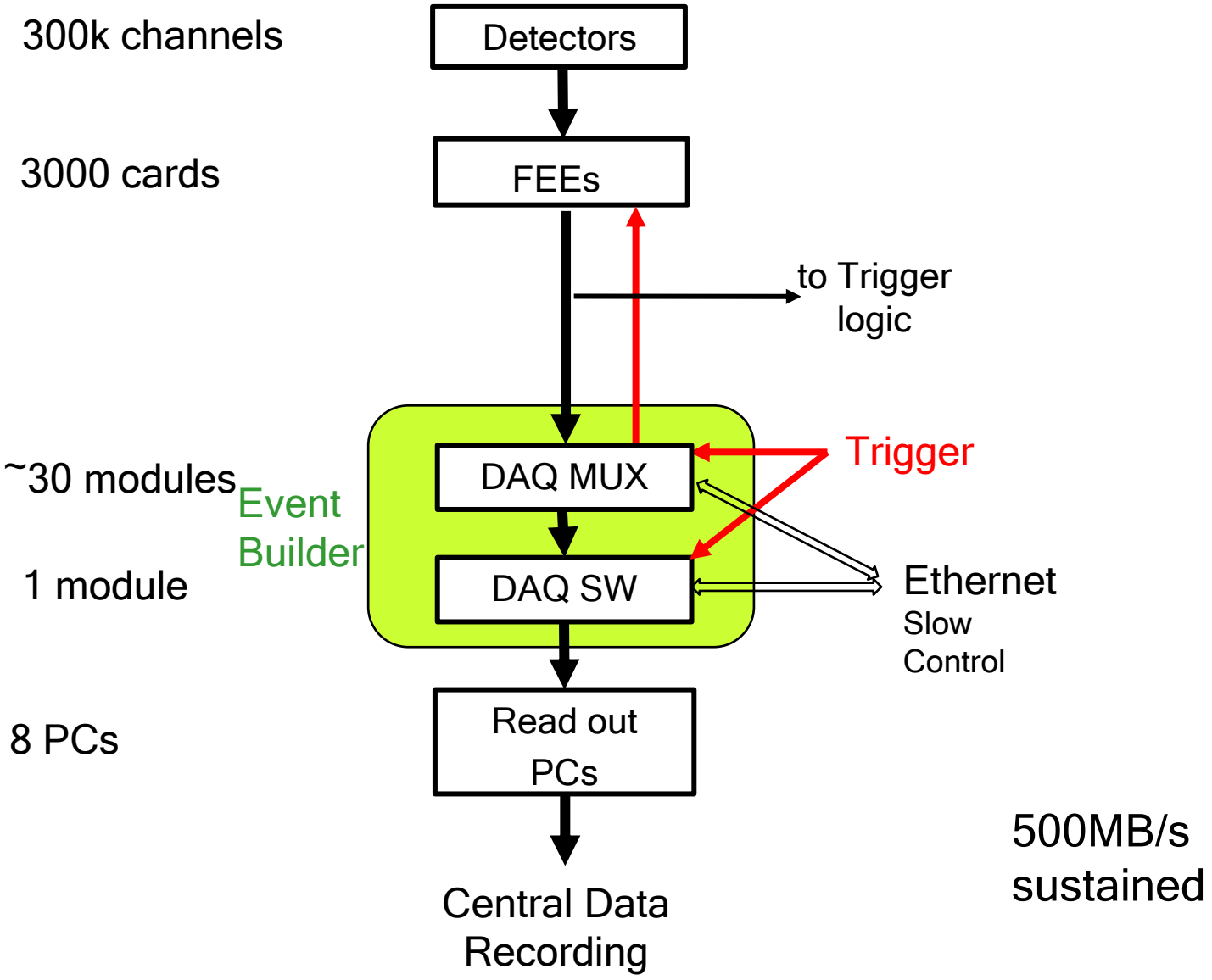
# TDC resolution

Time difference between two signals




$\sigma$ = 0.46 * 312/SQRT(2) = 101 ps

# Ultimate goal for Upgrade I



# Constants for cost estimation

- Wire chamber readout : 5 Euro/channel
- Calorimeter read out I: 50 Euro/channel (12b@80MHz)
- Calorimeter read out II: 150 Euro/channel (12b@250MHz)

# Cost estimate for absolute minimum upgrade

| Detector type | # of channels | Required out electronics | Cost kEuro |
|---|---|---|---|
| Calorimeters ECAL0, ECAL2 | 4.800 | 12b ADC@80MHz | |
| Calorimeters HCALs, ECAL1 | 2.200 | 10b ADC@80MHz | 110 |
| Micropattern detectors | ~100.000 | APV ASIC | |
| RICH, MWPC | 60.000 | APV ASIC | |
| RICH, MAPMT | 12.000 | F1 TDC | |
| SciFi | ~2.600<br>? | FPGA TDC<br>GANDALF TDC | 43 |
| Beam Momentum Station | 640 | FPGA TDC | 13 |
| Hodoscopes, VETO | 500 | FPGA TDC | 10 |
| Wire Chambers | ~60.000 | F1+FPGA TDC | |
| MWPC | 26.000 | FPGA TDC | 130+50 |
| Recoil Detector | 96 | 14b ADC@0.5(1.0)GHz | |
| Digital Trigger | ? | ? | ? |
| VME crates | 15 | | 75 |
| DHCmx | 20 | | 40 |
| DAQ | | | 50 |
| TOTAL | | | 520+? |

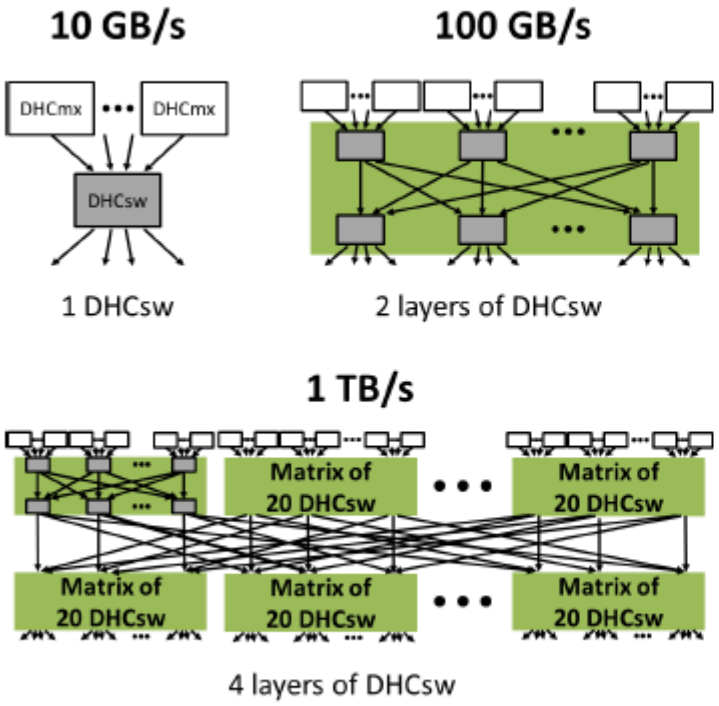
# Upgrade Scenario II

- Trigger less read out
- All data transferred to Online Computer Farm
- Online data processing
- FEE
  - All front-ends to be exchanged
  - TDC based readout : new TDC cards compatible
  - Calorimeter read out : new ADC modules compatible, requires development of firmware for feature extraction
  - Micro-pattern detectors require new ASICs, one of ASICs being developed for LHC upgrade :
    - SALT(LHCb), SAMPO(ALICE) …
    - Require active cooling and special infrastructure => high cost
- Data rate :
  - 50kB/event -> one event covers about 200 ns gate
  - 250GB/s in spill => 100 GB/s average

# Upgrade Scenario II

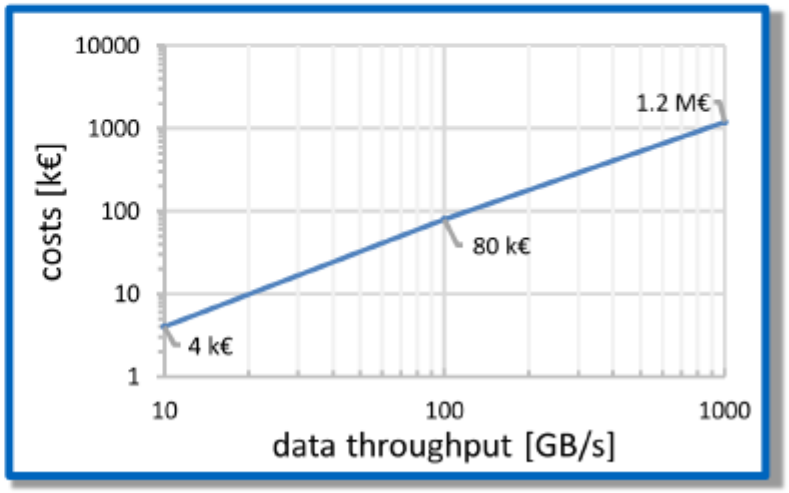
- Data processing without event definition
  - Time slice of 10us => “event”
  - 400 ns time overlap to avoid hit losses in event boundary regions

- Event Builder




**Scenario for:**

- Xilinx **7-series FPGA**
- SLINK interfaces replaced by **Aurora**



# Upgrade scenario II

- Challenges
  - DAQ – very challenging but feasible, requires significant man power
  - Real time data processing without event definition – new task, no expertize within COMPASS
  - Online farm -?

- Intermediate scenario
  - Trigger less FEE
  - Split data flow
    - Buffer main data for 1 ms
    - Process selected detectors by FPGA DIGITAL TRIGGER and define T0
  - Distribute Trigger via TCS and select corresponding data
  - If we filter out 95 % of data => 5GB/s average data rate

# Summary

- Development of new TDC FE started
- Development of new ADC for Micro-pattern detectors will start for 2017 upgrade
- Both development are compatible with COMPASS upgrade
- Scenario I upgrade
  - Digital trigger
  - AOV readout
  - 80kHz trigger rate
  - Starting cost : 500 kEuro

- Scenario II upgrade, trigger less readout
  - Full upgrade of FEE , cost the same as for scenario I
  - New ASIC for Silicon, GEM, MM, RICH -> significant increase of cost
  - DAQ upgrade feasible
  - Not enough information for Real cost estimate

THANK YOU

# COMPASS Detectors

| Detector type | # of channels | FEE type | |
|---|---|---|---|
| ECAL0 Calorimeter | 6.300 | 12b ADC@80Mhz | |
| ECAL1 Calorimeter | 1.500 | 10b ADC@80MHz | |
| ECAL2 Calorimeter | 3.000 | 12b ADC@80MHz | |
| HCAL1 Calorimeter | 480 | 10b ADC@80MHz | |
| HCAL2 Calorimeter | 220 | 10b ADC@80MHz | |
| Silicon detectors | 25.000 | APV ASIC | |
| GEM | 33.000 | APV ASIC | |
| PixelGEM | 10.000 | APV ASIC | |
| Pixel MicroMega | 30.000 | APV ASIC | |
| RICH, MWPC | 60.000 | APV ASIC | |
| RICH, MAPMT | 12.000 | CMAD+F1 TDC | |
| BeamMomentumStation | 640 | Disc+F1 TDC | |
| SciFi | 2.600 | Disc.+F1 TDC | |
| Hodoscopes,Veto | 500 | Disc.+F1 TDC | |

# COMPASS Detectors

| Detector type | # of channels | Required out electronics | |
|---|---|---|---|
| MWPC | 26.000 | CMAD+F1TDC | |
| Muon Wall 1 | 10.000 | Custom Disc.+F1 TDC | |
| Muon Wall 2 | 2.000 | ASD8+F1 TDC | |
| DC0-4 | 6.500 | ASD8+F1 TDC | |
| DC5 | 2.300 | CMAD+FPGA TDC | |
| Straw | 9.000 | ASD8+F1 TDC | |
| W45 | 3.000 | ASD8+F1 TDC | |
| Recoil Detector | 96 | 14bADC@0.5(1.0)GHz | |