FPGA based data processing in the ALICE High-Level Trigger in LHC Run 2

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13.10.2016, CHEP

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in der Informationsverarbeitung
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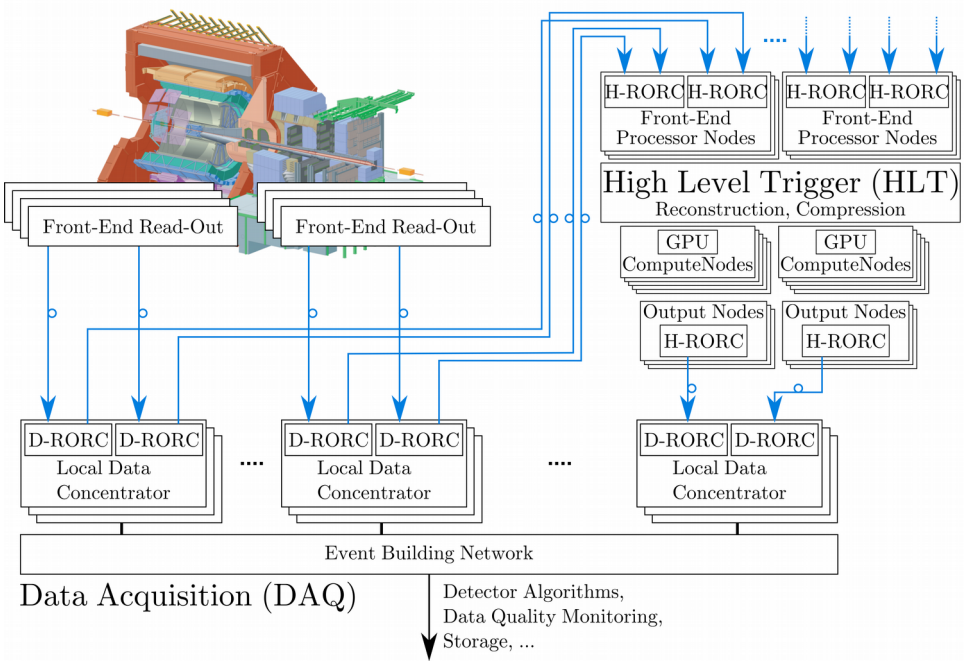
05P15RFCA1

ALICE

Outline

- ALICE online architecture
- Hardware overview
- Implementation in the ALICE High-Level Trigger
- Hardware cluster finding in the HLT
- Summary & outlook

ALICE Online Architecture



Run 1

- ~500 optical Detector Data Links (DDL) from Front-End Electronics to Data Acquisition (DAQ)
- Copy of detector data to High-Level Trigger (HLT)
- HLT results back to DAQ via DDL
- Independent Read-Out Receiver Card (RORC) projects for
  DAQ (PCI-X/PCIe, Stratix II) and
  HLT (PCI-X, Virtex-4)

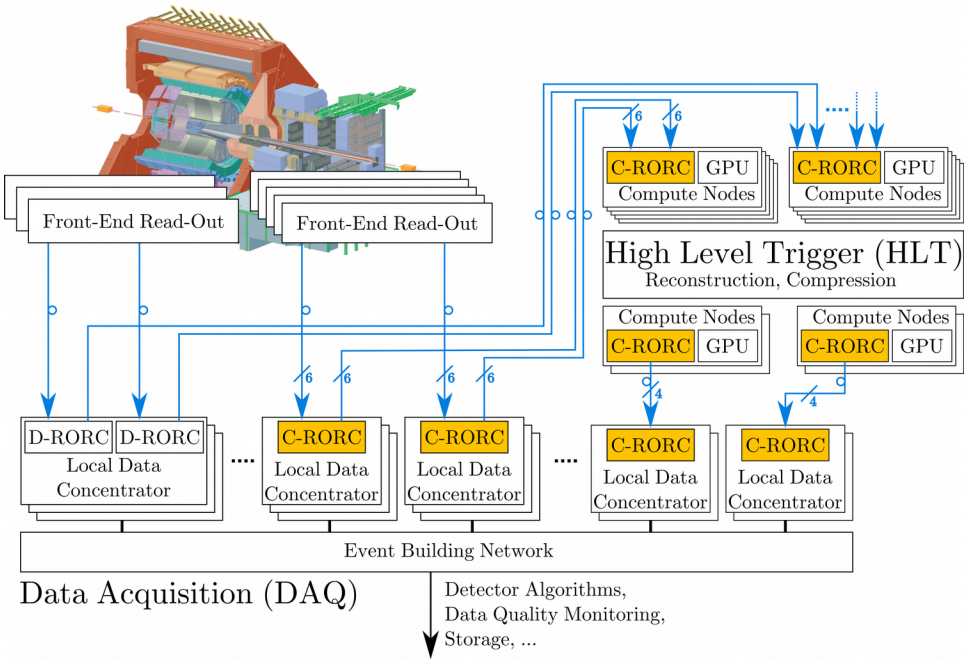
ALICE Online Architecture

Run 2:

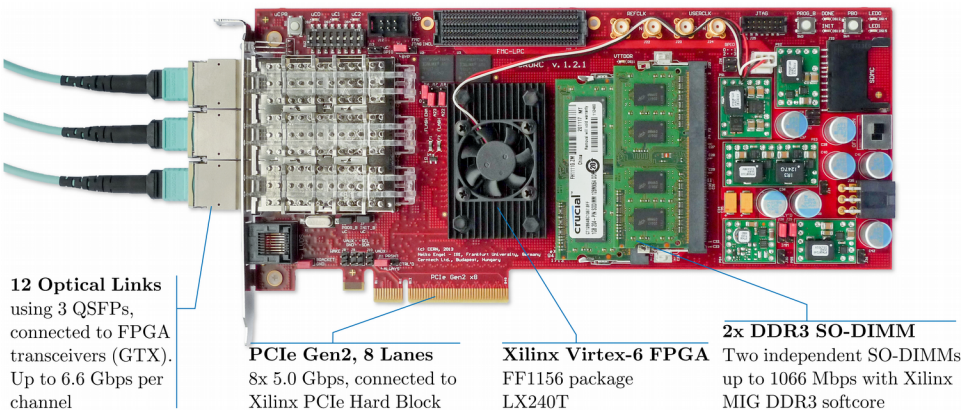
General architecture remains the same.

Common Read-Out Receiver Card (C-RORC) for Data Acquisition and High-Level Trigger

- Support for higher link rates
- Up-to-date interfaces and form factor
- Increased link density
- Requirements made custom development unavoidable at that time



C-RORC Hardware Overview

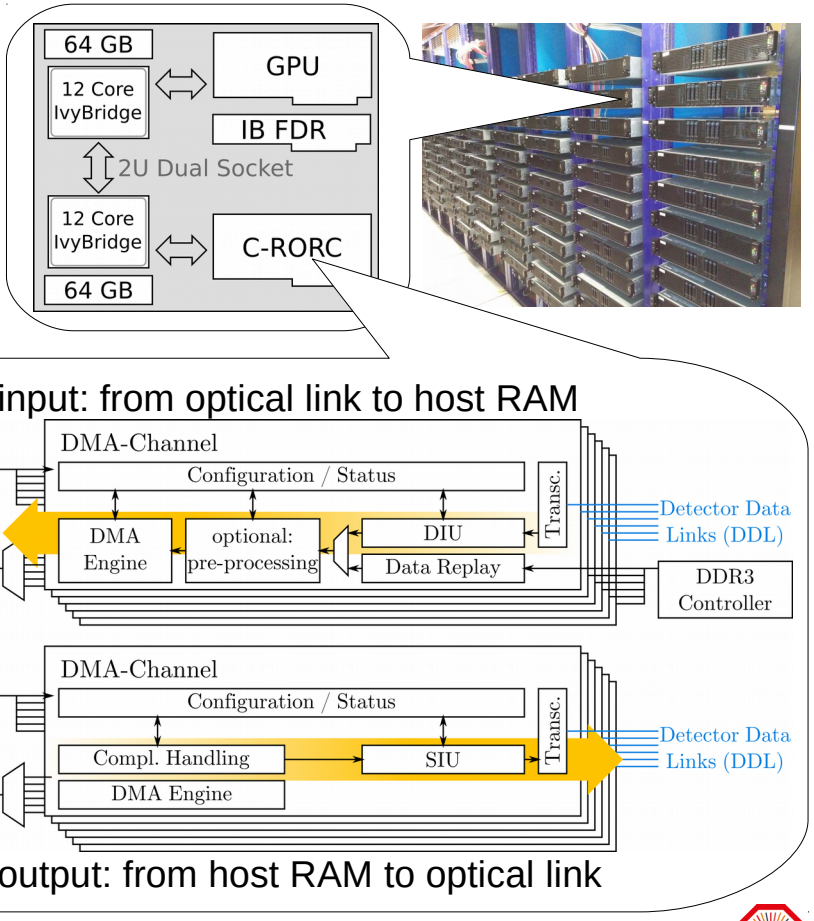


- Common Read-Out Receiver Card
- 4 applications
  - ALICE Data Acquisition
  - ALICE High-Level Trigger
  - ATLAS TDAQ Readout System
  - ATLAS TDAQ RoI-Builder
- Around 400 boards produced
- Running in production systems of ALICE & ATLAS since start of Run 2
- Development platform for ALICE Run 3

C-RORC in the ALICE High-Level Trigger

- ALICE High Level Trigger (HLT) — M. Krzewicki Mon. 11:45
  - Online reconstruction, -compression & -calibration — M. Krzewicki Mon. 14:30
  - 180 server nodes with GPUs — J. Lehrbach Mon. 12:00
  - 74 C-RORCs as main HLT data input and output interfaces
  - Custom data transport framework — D. Rohr Mon. 12:00
  - Tracking with GPUs — D. Rohr Mi. 13:15
  - Cluster finding with FPGAs

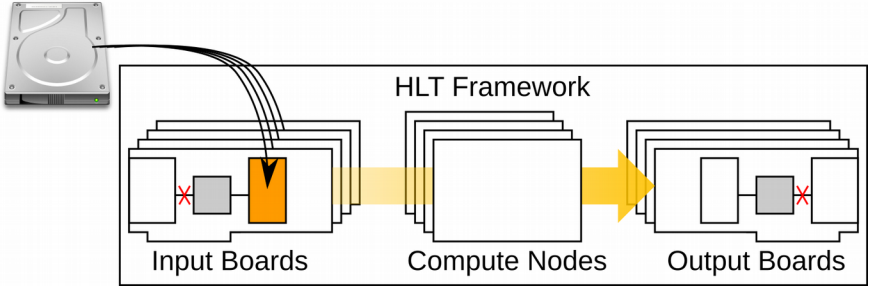
Firmware Variant	#DDLs	Link speed [Gbps]	Hardware pre-processing
HLT_IN	up to 12	up to 5.3125	-
HLT_IN_FCF	6	2.125 or 3.125	TPC cluster finder
HLT_OUT	4	5.3125	-



HLT Standalone Testing with C-RORC Data Replay

- Input Side: Data Replay
  - Load event data into C-RORC on-board memory
    - From previous run, simulated, generated, incomplete, noise, …
  - Let all boards in the HLT replay their data with a selectable rate & duration
- Output Side:
  - discard data in FPGA just before sending it to DAQ

- Benchmarking the limits of the full system – from input to output
- Tune configuration
- Induce errors
- Analyze component behavior
- Fully independent from LHC, DAQ or any detector state



HLT Hardware Cluster Finding

- Processing of raw TPC data already in the FPGA
- *FastClusterFinder* (T. Alt) RT2010
  - Locate clusters in time and pad direction
  - Calculate cluster properties
  - Merge candidates from neighboring pads
  - Separate overlapping clusters
- Significantly faster than the CPU equivalent
- Already essential part of HLT in Run 1

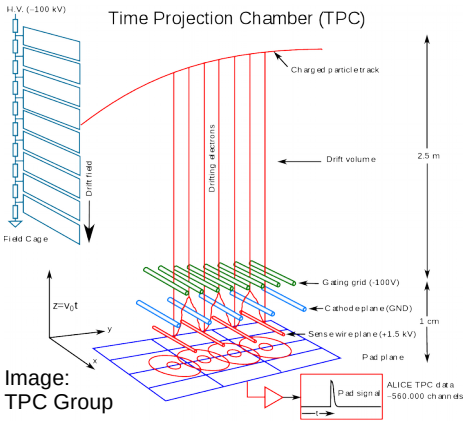


Image: TPC Group

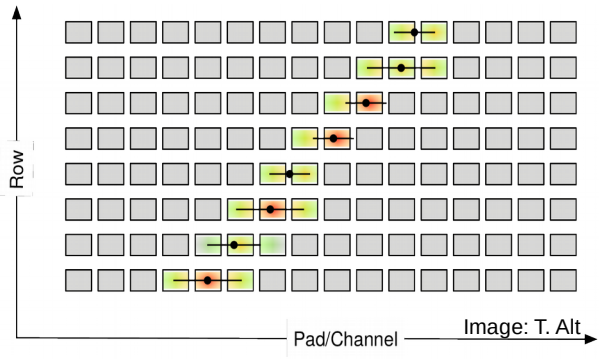
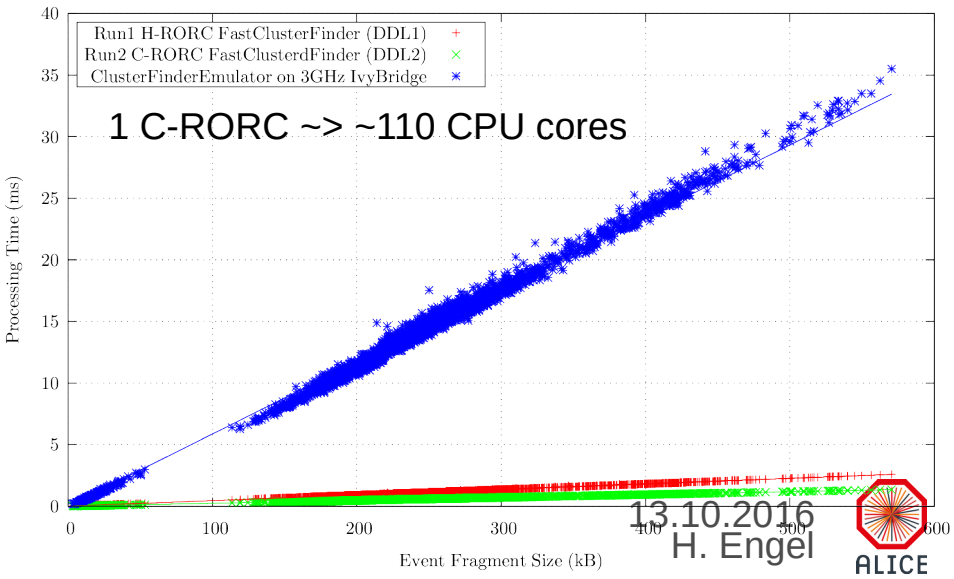
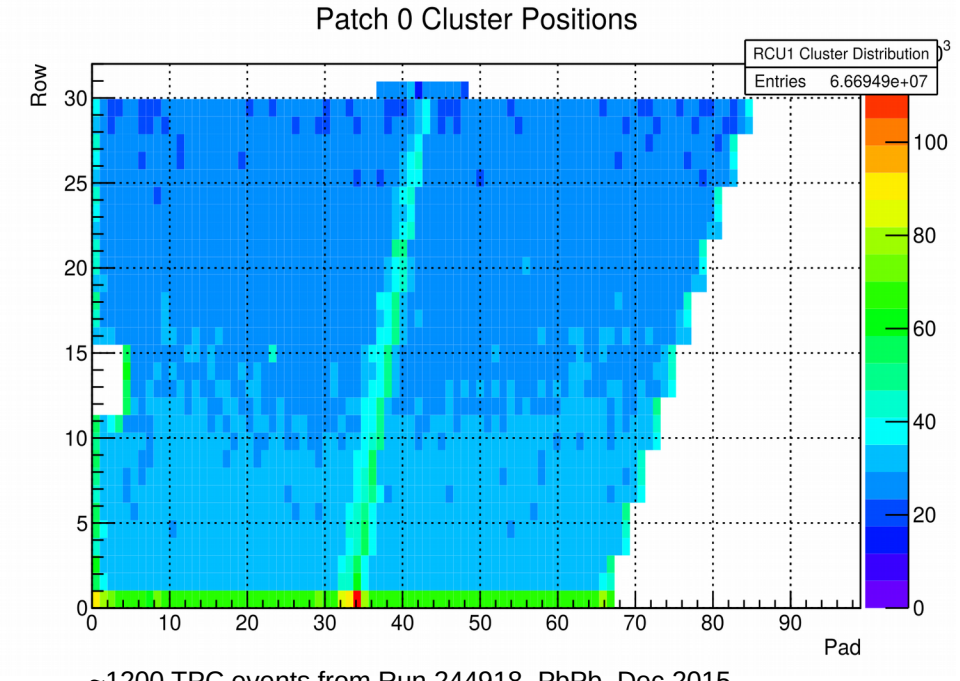


Image: T. Alt



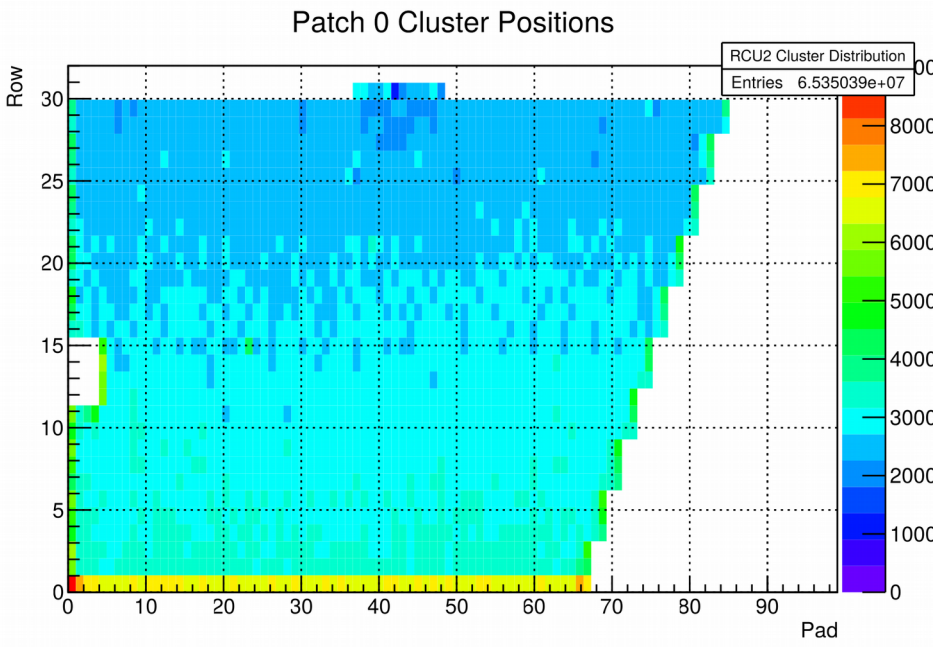
HLT Readout of the TPC Readout Control Unit 1

- TPC Readout Control Unit 1 (RCU1) since Run 1
  - Readout with 2.125 Gbps
  - Full time sequence above threshold for each pad, one pad after the other, one row after the other
    - Cannot use typical image processing algorithms
  - Two branches per row, interleaved readout
    - Creates artificially split clusters at branch boundary



~1200 TPC events from Run 244918, PbPb, Dec.2015, run through RCU1 cluster finder

HLT Readout of the new TPC Readout Control Unit 2



Same set of ~1200 TPC events from Run 244918, PbPb, Dec.2015, converted to RCU2 data format, run through RCU2 cluster finder

- TPC Readout Control Unit 2 (RCU2) installed Q1/2016
- Increased link rate: 3.125 Gbps
- 4 branches internally
- Branch merging already in RCU2
  - Improved HLT cluster finding performance
  - ~2-3% less (fake-border) clusters

HLT Readout of the new TPC Readout Control Unit 2

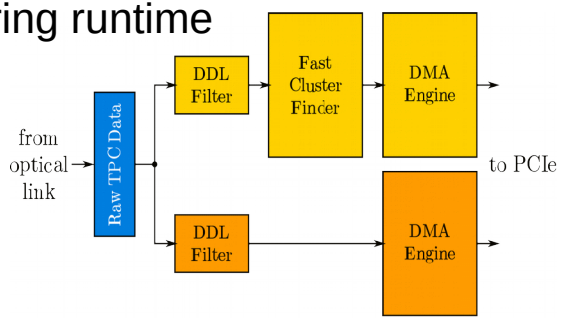
- Required adjustments to the HLT cluster finder
  - Scaling with DDL bandwidth was not sufficient due to increased noise from TPC
  - Over-proportional increase of clock frequency and buffer depth was necessary
  - Tweaks, register stages, rewrites, ...
- Combined firmware with RCU1 & RCU2 support
  - Supports data replay of any event since start of Run 1

Clock frequencies	DDL speed	DDL clock	Cluster finder clock
RCU1 cluster finder	2.125 Gbps	53 MHz	159 MHz (3x DDL clock)
RCU1+2 cluster finder	3.125 Gbps	78 MHz	312 MHz (**4x** DDL clock)

Post-SYN Resource Usage	LUTs	FFs	DSPs	BRAMs
RCU1 cluster finder	4545	5169	8	19
RCU1+2 cluster finder	4521	8745	8	24

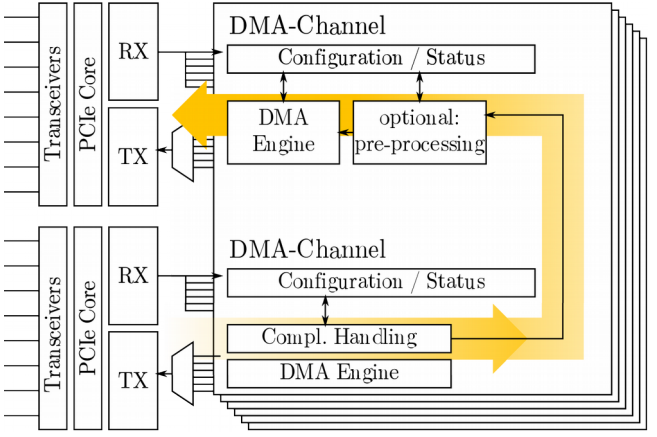
RCU2 Cluster Finder Verification

- Verification of input data:
  - properly ordered data required for FCF
    - Ordering information get lost during processing
    - FW provides secondary readout channel for raw data before FCF
    - Attach/detach verification process during runtime



  - Payload protocol error detection & reporting in firmware

- Implementation verification
  - Testing with data replay works, but is cumbersome for big data sets
  - Co-processor implementation allows batch-testing of raw data
  - Same building blocks as input/output firmware images



Summary / Outlook

- C-RORC hardware platform is in use in several production systems
- Main data input/output interface of the ALICE High-Level Trigger
- Data replay from on-board storage allows standalone full system tests
- HLT does online cluster finding in FPGAs, saving lots of CPU cores
- Upgrade of TPC Readout Control Unit required adjustments to HLT cluster finder
- Improved cluster finding performance coming with RCU2 branch merging
- Common HLT firmware supports both RCU versions
- Verification of cluster finder input and output
- Improved error detection & reporting
- Cluster finder improvements being evaluated:
  - Split cluster tagging
  - Noise reduction for peak finding