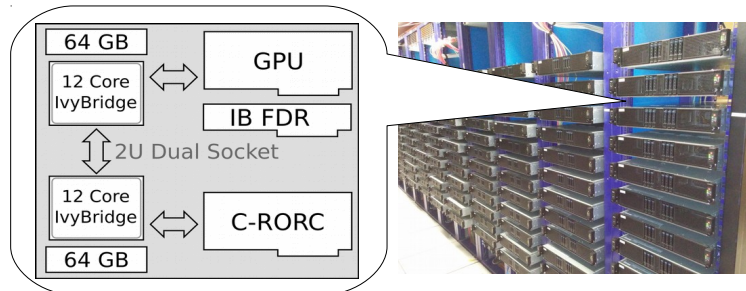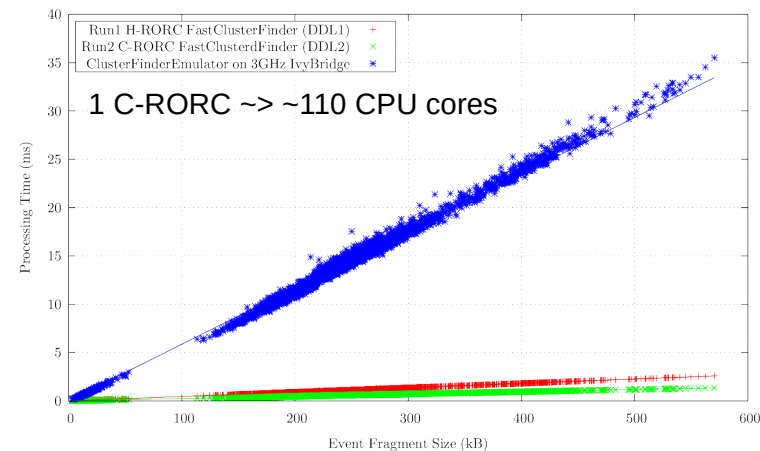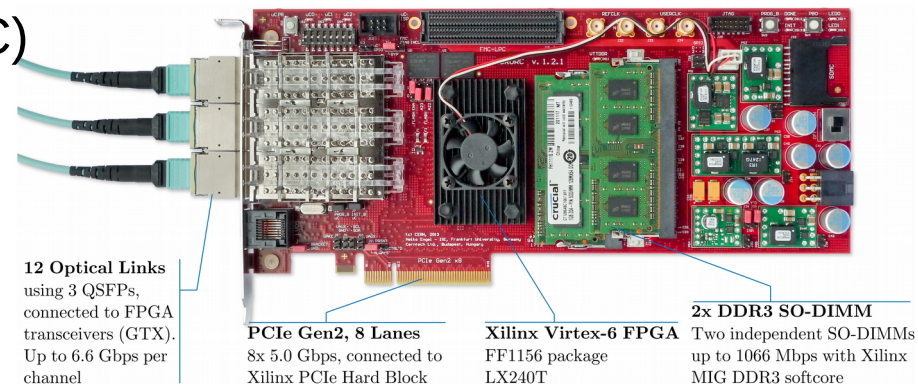# FPGA based data processing in the ALICE HLT in LHC Run 2

- Common Read-Out Receiver Card (C-RORC) is the main data input/output interface of the ALICE High-Level Trigger (HLT)

12 Optical Links using 3 QSFPs, connected to FPGA transceivers (GTX). Up to 6.6 Gbps per channel

PCIe Gen2, 8 Lanes 8x 5.0 Gbps, connected to Xilinx PCIe Hard Block

Xilinx Virtex-6 FPGA FF1156 package LX240T

2x DDR3 SO-DIMM Two independent SO-DIMMs up to 1066 Mbps with Xilinx MIG DDR3 softcore

- Among raw readout, HLT performs cluster finding of TPC data already inside the FPGA

  - Significantly faster than CPU-based cluster finding

1 C-RORC ~> ~110 CPU cores

Infrastruktur und Rechnersysteme
in der Informationsverarbeitung
Goethe-Universität Frankfurt am Main

Heiko Engel, Torsten Alt,
for the ALICE Collaboration

FPGA based data processing in the ALICE HLT in LHC Run 2

- C-RORC hardware platform is in use in several production systems

- Data replay from on-board storage allows standalone full system tests

- Upgrade of TPC Readout Control Unit (RCU2) required adjustments to HLT cluster finder

- Improved cluster finding performance coming with RCU2 branch merging

- Common HLT firmware supports both RCU versions

- Verification of cluster finder input and output

- Improved error detection & reporting

- Cluster finder improvements being evaluated:

  - Split cluster tagging

  - Noise reduction for peak finding

IRI Infrastruktur und Rechnersysteme
in der Informationsverarbeitung
Goethe-Universität Frankfurt am Main

2

13.10.2016
H. Engel

ALICE