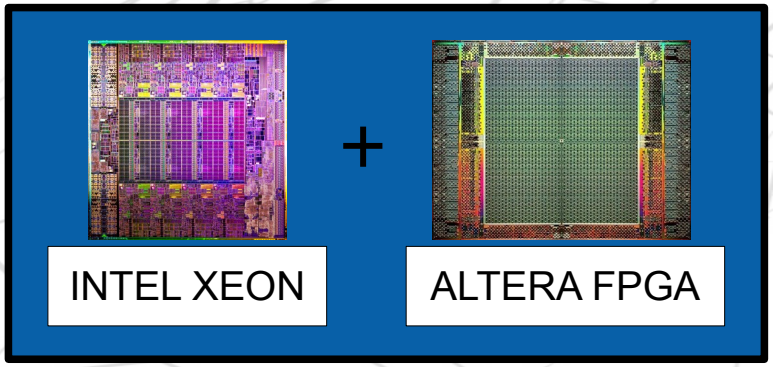
# Highlights Oral-312 (1/2)

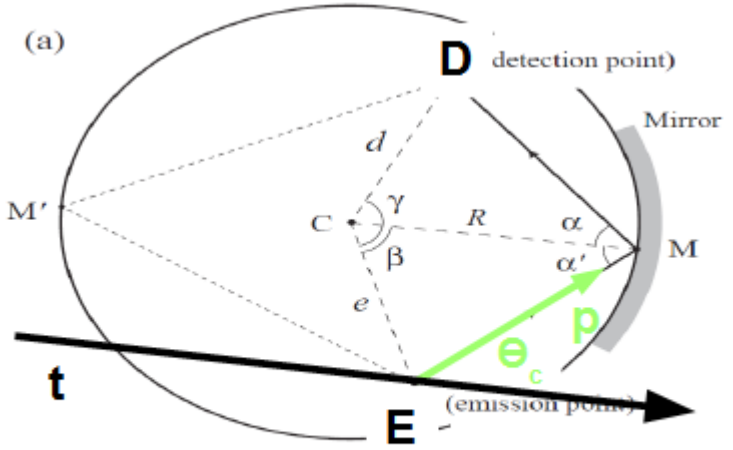
## Hardware




- Two socket system:
  First : Intel® Xeon® E5-2680 v2
  Second : Altera Stratix V GX A7 FPGA

- Host Interface: QPI
- Memory: Cache-coherent access to main memory
- Programming model : Verilog now also OpenCL

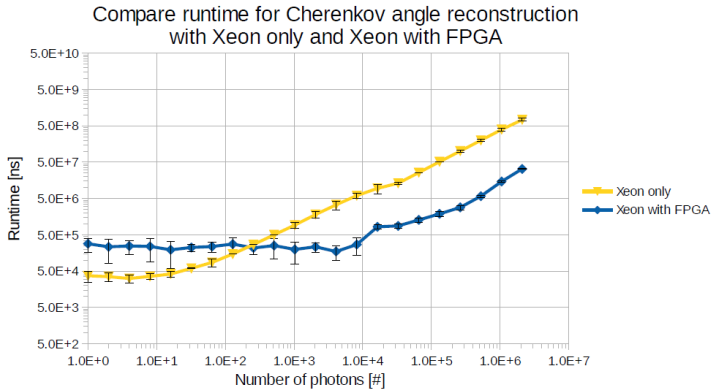
## Cherenkov angle reconstruction




Reference: LHCb Note LHCb-98-040

- Calculate Cherenkov angle $\Theta_c$ for each track **t** and detection point **D**
- RICH PID is not processed for every event so far, processing time too long!

# Highlights Oral-312 (2/2)




- Acceleration of factor up to 35 with Intel® Xeon/FPGA with respect to single Intel® Xeon thread
- Theoretical limit of photon pipeline: a factor 64 with respect to single Intel® Xeon thread
- Bottleneck: Data transfer bandwidth to FPGA

## Compare Verilog – OpenCL

- Faster and easier
- Comparable performance
- Similar resource usage

## Compare QPI – PCIe Interface

- Hardware Nallatech vs. Intel® Xeon/FPGA
- Same Stratix V FPGA in both devices

RICH Kernel

Compare Nallatech 385 and Intel Xeon/FPGA acceleration