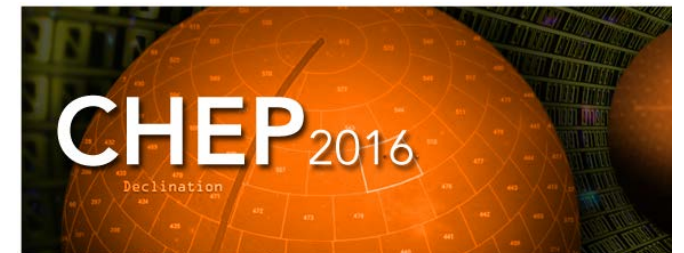# ATLAS Trigger and Data Acquisition Upgrades for High Luminosity LHC

CHEP 2016, San Francisco (USA), 10-14 October 2016
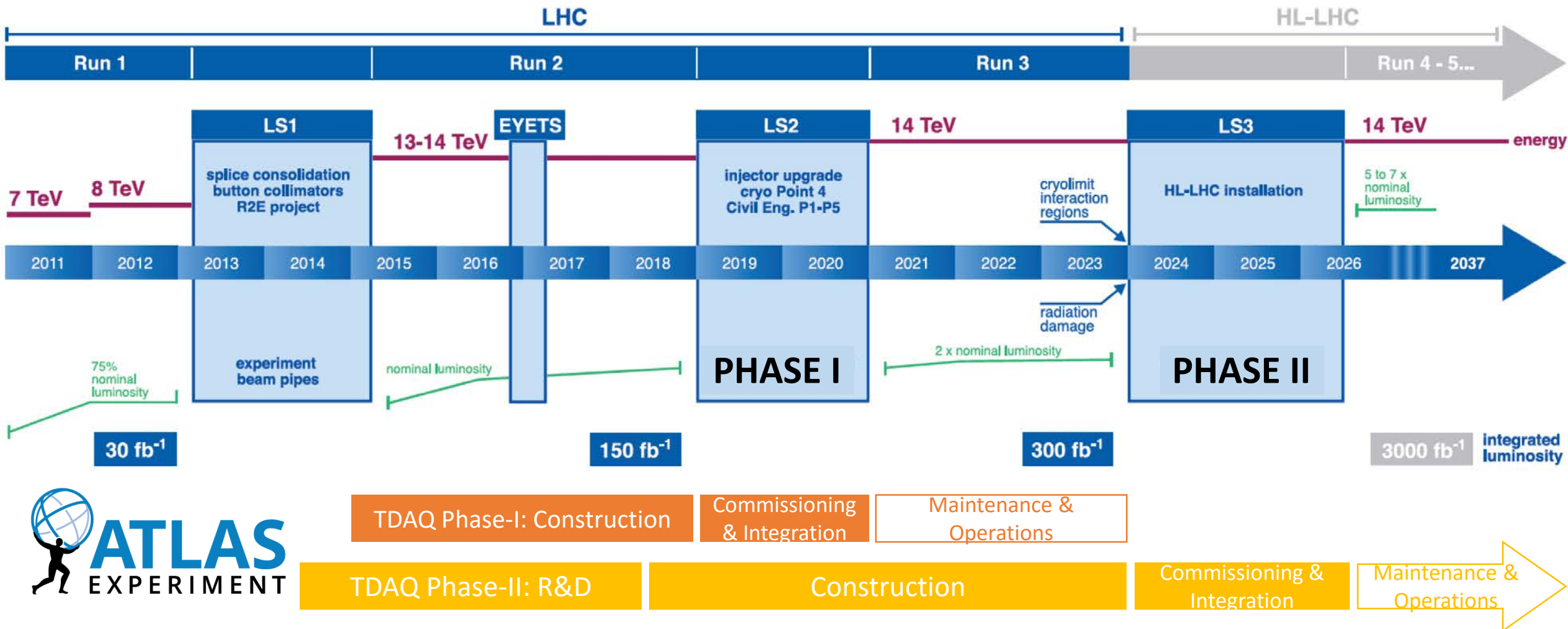
Simon George

Royal Holloway, University of London

On behalf of the ATLAS Collaboration

High Luminosity LHC

ATLAS upgrade for High Luminosity LHC

- Motivation: high luminosity $\Rightarrow$ high pile up*, increased radiation and readout bandwidth

- New Inner TracKer – silicon strips and pixels

- New Trigger & Data AcQuisition system

- Upgraded calorimeter and muon detectors

- Upgraded computing and software

HL-LHC tt̄ event in ATLAS ITK at <μ>=200
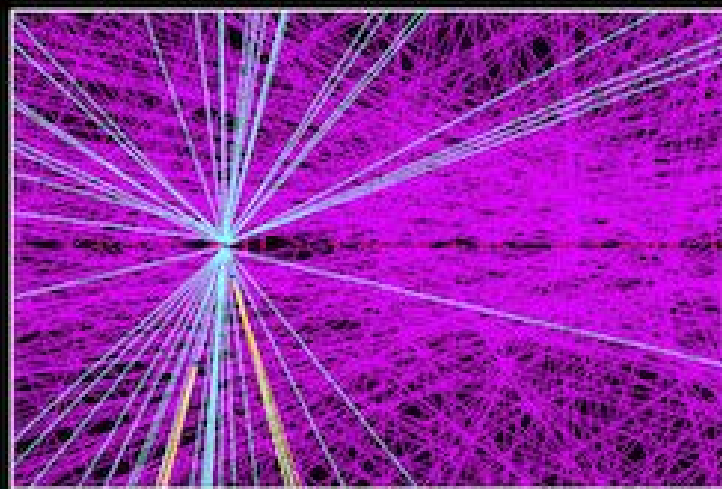
* Multiple interactions per bunch crossing

https://twiki.cern.ch/twiki/bin/view/AtlasPublic/UpgradeEventDisplays

TDAQ System Design
Overview of one of the two design options

- Level-0 Muon & Calo used to make initial fast rejection and identify Regions of Interest
- Level-1 hardware track trigger and high resolution calo data provide further rejection
- DAQ comprises readout, regional requests, data handling and storage
- Storage Handler decouples Event Filter from DAQ so it can work continuously, between fills
- Event Filter combines commodity processor farm and hardware tracking
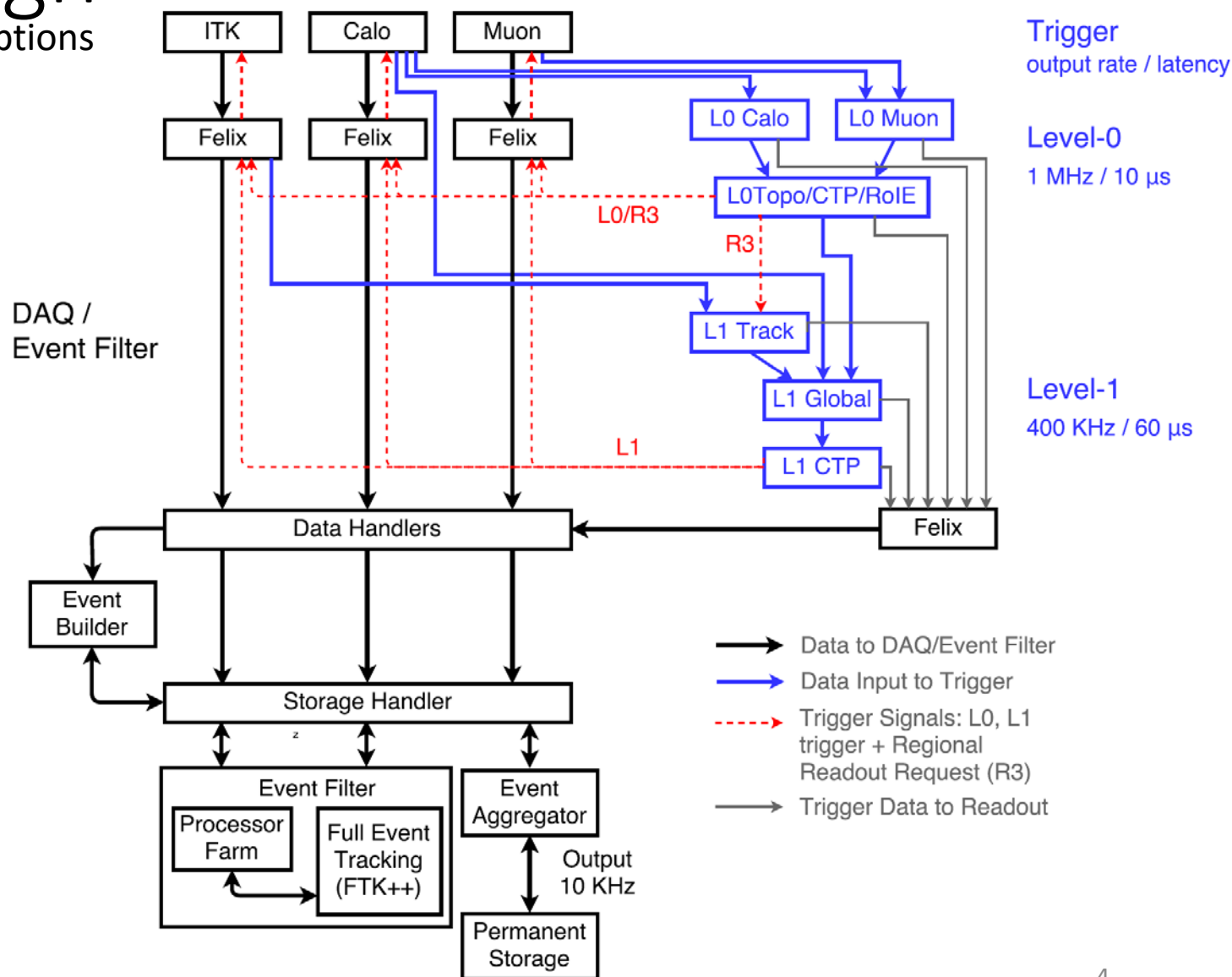
Trigger strategy for HL upgrade

- High rate of low threshold inclusive single lepton triggers to maximize electroweak physics. **Higher thresholds would significantly limit physics potential.**

- Lower rate triggers for multiple low-p_T leptons, taus, jets and missing transverse energy

- Robustness against pileup through early use of high granularity calorimeter information and hardware tracking

- Upgrades to improve muon efficiency

- Trigger as close as possible to offline selection, to improve efficiency and minimise systematics

- Note: Level-1 rates projected to HL **far exceed 100 kHz limit of Run 3 system**

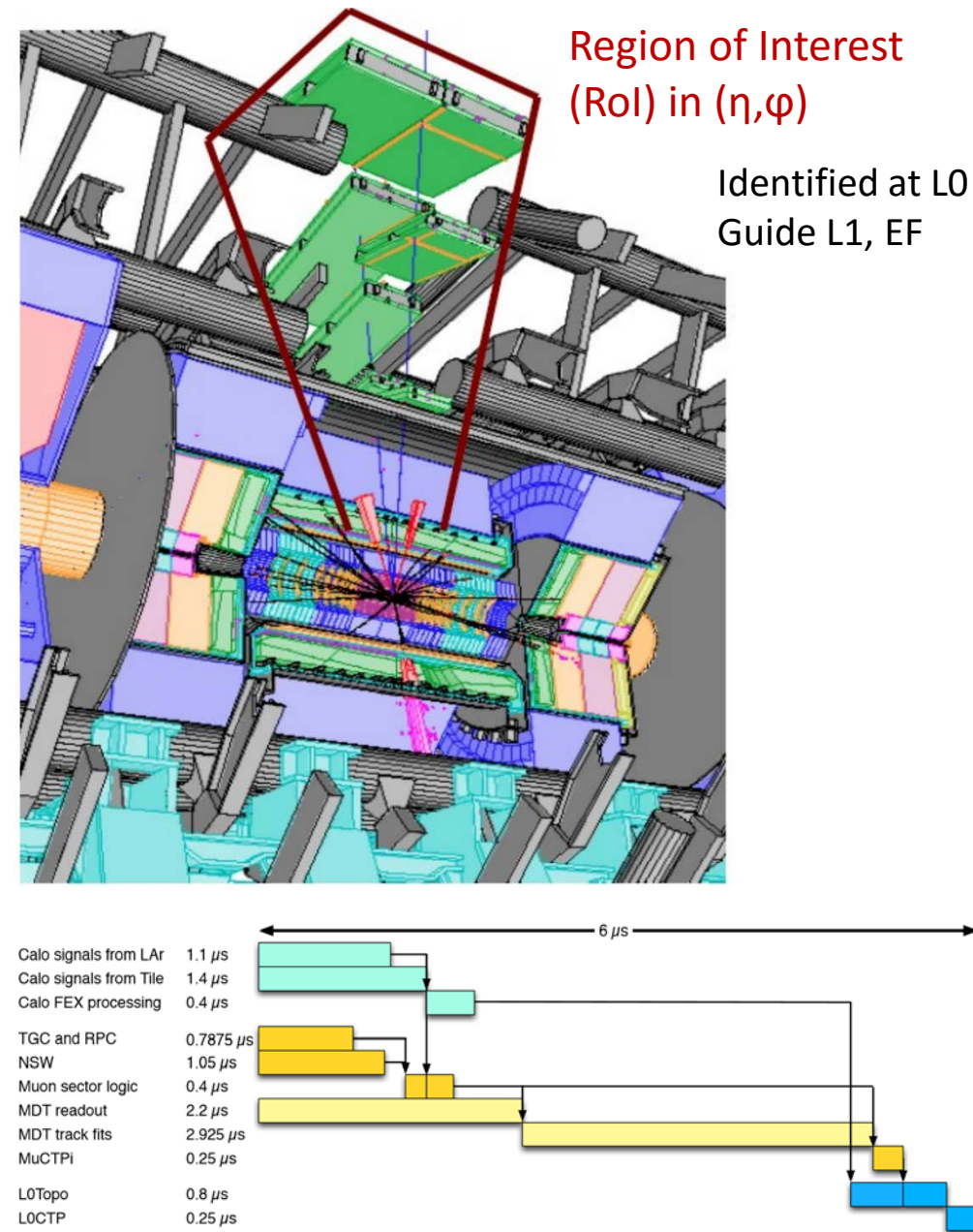Estimated rates and thresholds for architectures described on following pages

Item	Offline p_T Threshold [GeV]	Offline $|\eta|$	L0 Rate [kHz]	L1 Rate [kHz]	EF Rate [kHz]
isolated single e	22	< 2.5	200	40	2.20
forward e	35	2.4 − 4.0	40	8	0.23
single γ	120	< 2.4	66	33	0.27
single μ	20	< 2.4	40	40	2.20
di-γ	25	< 2.4	8	4	0.18
di-e	15	< 2.5	90	10	0.08
di-μ	11	< 2.4	20	20	0.25
$e - \mu$	15	< 2.4	65	10	0.08
single τ	150	< 2.5	20	10	0.13
di-τ	40,30	< 2.5	200	30	0.08
single jet	180	< 3.2	60	30	0.60*
large-R jet	375	< 3.2	35	20	0.35*
four-jet	75	< 3.2	50	25	0.50*
H_T	500	< 3.2	60	30	0.60*
E_T^{miss}	200	< 4.9	50	25	0.50*
jet + E_T^{miss}	140,125	< 4.9	60	30	0.30*
forward jet**	180	3.2 - 4.9	30	15	0.30*
Total			~1000	~400	~10

ATLAS Phase-II Upgrade Scoping Document CERN-LHCC-2015-020

Level-0 Trigger

- **L0 Calo**
  - Coarse calorimeter data sent to three feature extractors (em/tau, jet and global) to find different types of trigger objects (TOBs)
  - Firmware upgrade; largely same hardware as Run 3

- **L0 Muon**:
  - New readout and improved coverage to increase efficiency
  - Latency now long enough to use precision MDTs for sharper turn on

- **"L0Topo/CTP/RoIEngine"**
  - Receives trigger objects from L0 Calo and L0 Muon
  - Performs complex trigger selections (invariant mass, missing transverse energy, etc.) and applies the L0 trigger menu
  - On L0 Accept, the RoIEngine calculates the Regional Readout Requests (R3) to send back to the detectors via FELIX
  - RoIs cover at most 10% of detector => 100 kHz equivalent rate for readout

Region of Interest (RoI) in (η,φ)

Identified at L0
Guide L1, EF

|	
Calo signals from LAr	1.1 μs
Calo signals from Tile	1.4 μs
Calo FEX processing	0.4 μs
TGC and RPC	0.7875 μs
NSW	1.05 μs
Muon sector logic	0.4 μs
MDT readout	2.2 μs
MDT track fits	2.925 μs
MuCTPi	0.25 μs
L0Topo	0.8 μs
L0CTP	0.25 μs

6 μs

Level-1 Trigger

L1Global

- Low latency aggregation network for calo data; time multiplexed event processing in FPGA/GPU

- Process finer-grained calo information using all cells to improve e, γ, τ, jets, E_T^{miss}

- Combine refined calo objects and L0 muons with tracks from **L1Track**

- Make topological combinations
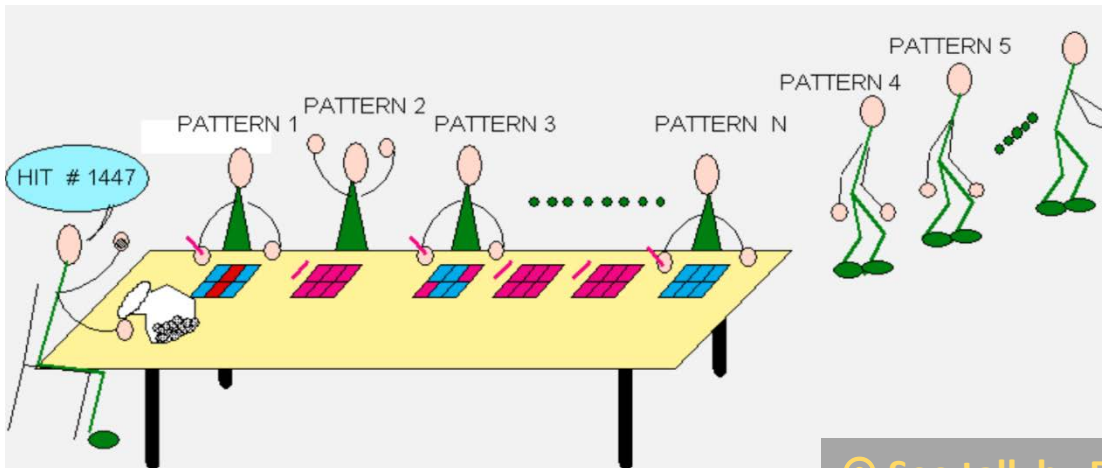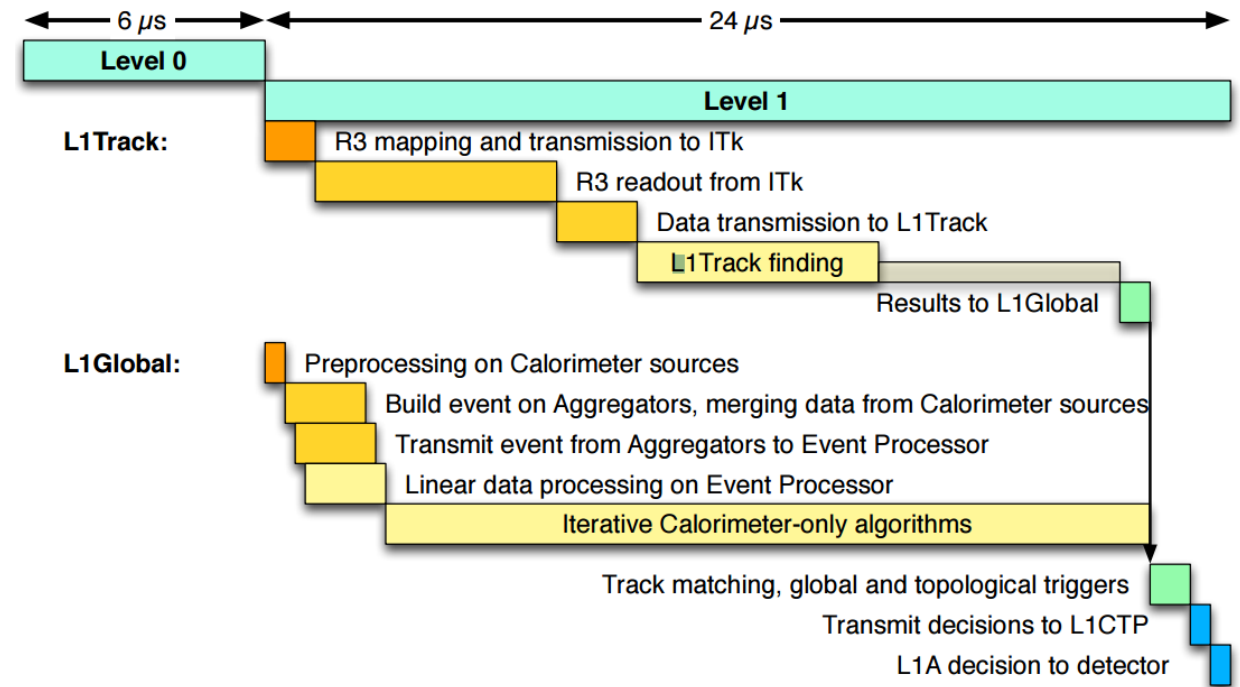
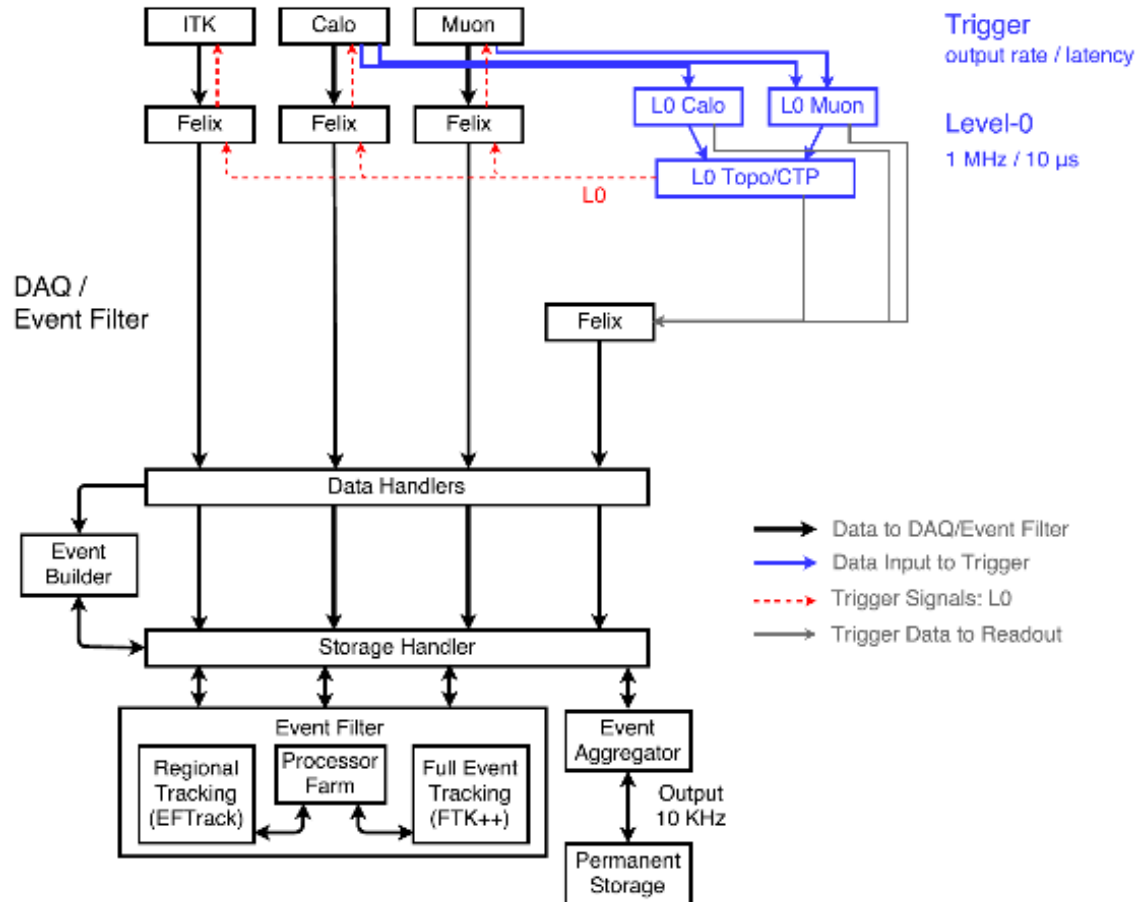**L1Track**:
- Hardware tracking using AM chips to match data to patterns
- Finds tracks with p_T > 4 GeV in RoIs at 1 MHz
- For electron identification and to reduce the pileup background to multi-object events

⊙ **See talk by B Allbrooke**
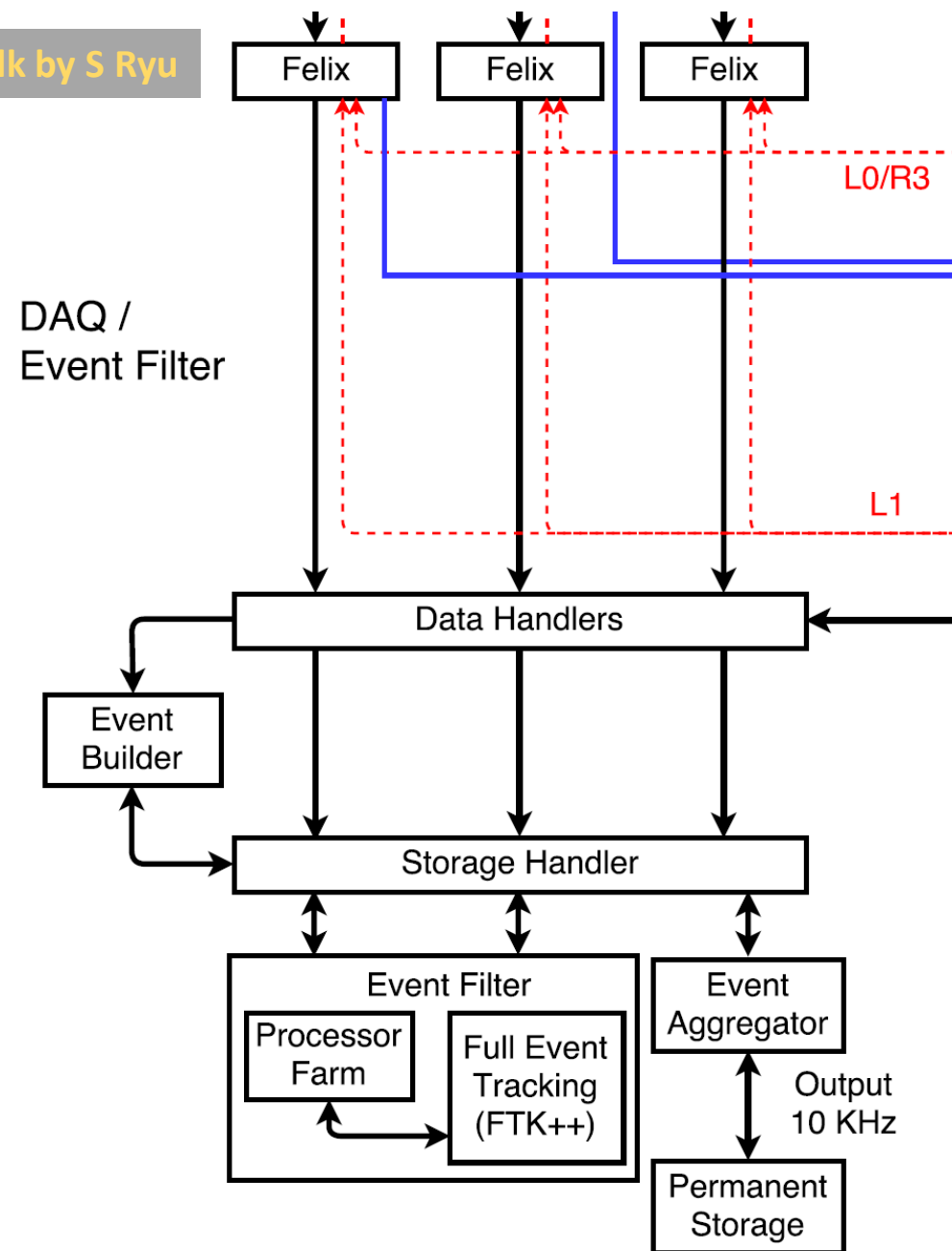
Level-0-only option

- L1 hardware trigger and RoI Engine relocated to EF hardware & software
  - Consequently no major EF CPU increase
- Readout less complex but less flexible
- DAQ scaled for 1 MHz readout from all detectors

- Also looking at L0+L1 option in which lower latency is traded for higher L0 accept rate
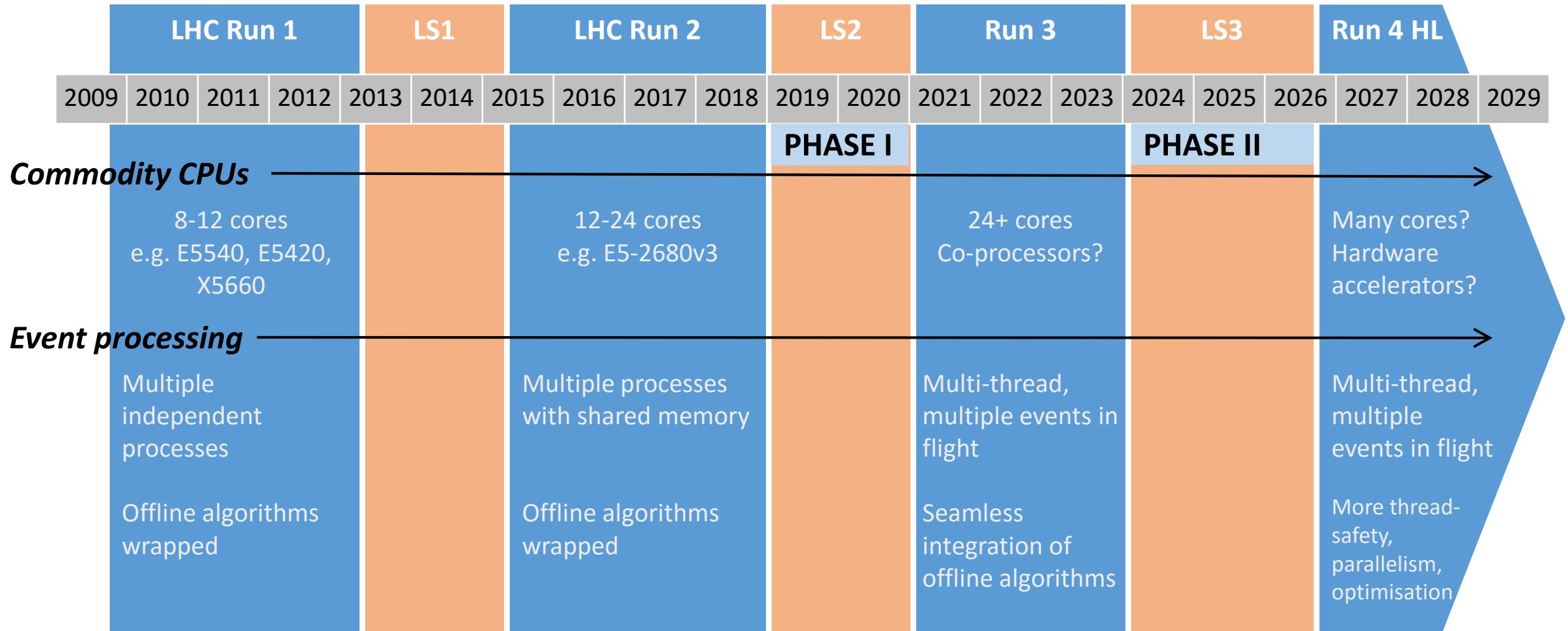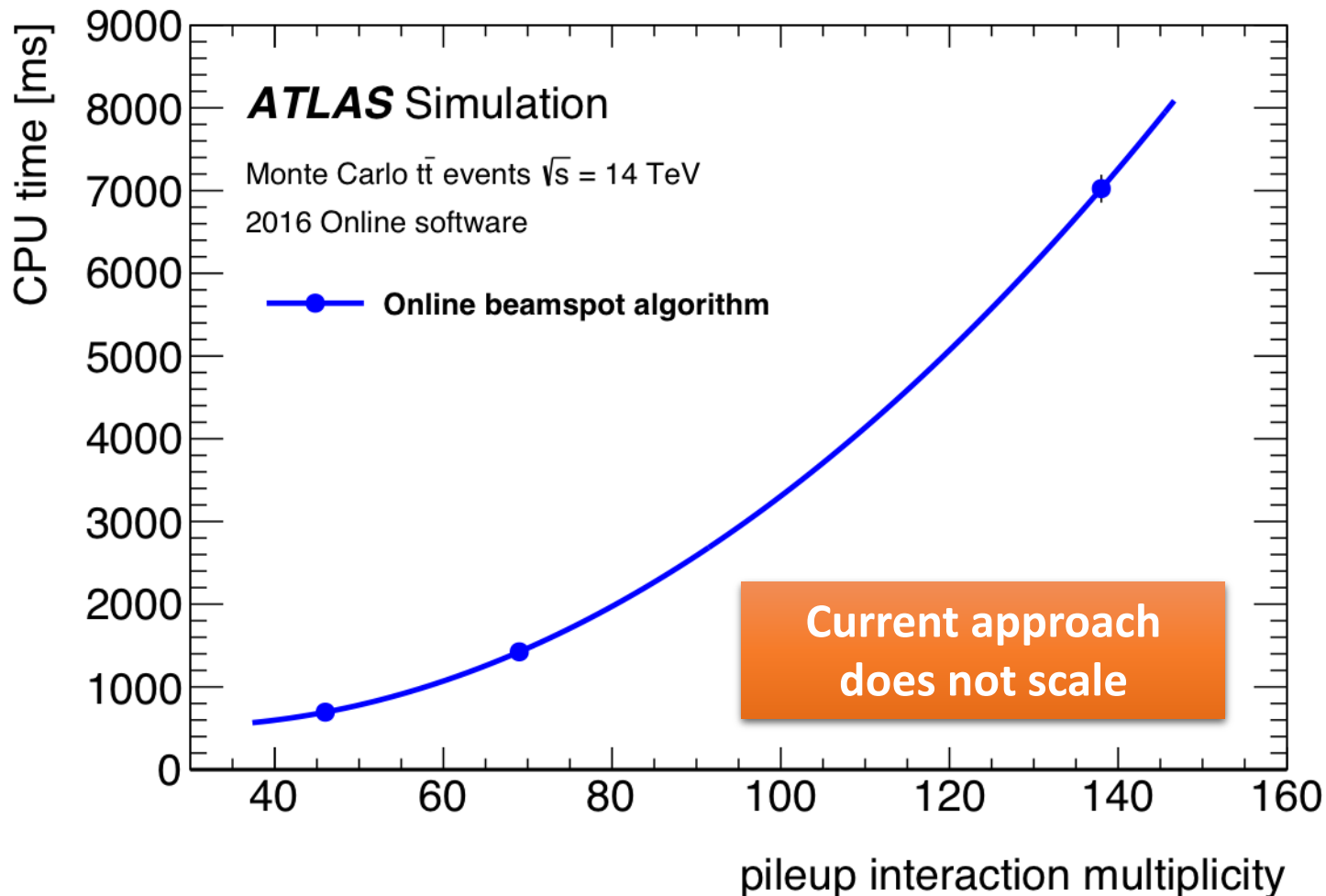
Data Acquisition

- **Trends from custom to commodity hardware, and hardware to software**

- Front End LInk eXchange (FELIX)
  - Routes between custom serial links and commodity multi-gigabit networks
  - Building on initial use in Phase-I

- Data Handler
  - Detector-specific data processing and monitoring.
  - Software toolkit and commodity computers replace custom hardware & firmware

- Event Builder
  - May be logical or physical
  - Data compression drives resources

- Storage Handler
  - Decouples Event Filter from DAQ so **EF can work continuously, between fills**
  - Requires storage volume of the order of **50 PB**, able to concurrently receive and serve a few TB/s

High Level Trigger CPU and software evolution

	LHC Run 1	LS1	LHC Run 2	LS2	Run 3	LS3	Run 4 HL

2009 2010 2011 2012 2013 2014 2015 2016 2017 2018 2019 2020 2021 2022 2023 2024 2025 2026 2027 2028 2029

PHASE I   **PHASE II**

Commodity CPUs →

8-12 cores
e.g. E5540, E5420, X5660

12-24 cores
e.g. E5-2680v3

24+ cores
Co-processors?

Many cores?
Hardware accelerators?

Event processing →

Multiple independent processes

Offline algorithms wrapped

Multiple processes with shared memory

Offline algorithms wrapped

Multi-thread, multiple events in flight

Seamless integration of offline algorithms

Multi-thread, multiple events in flight

More thread-safety, parallelism, optimisation

⊙ **See talks by B Wynne, P Conde Muino**

Event Filter: tracking expected to dominate CPU time

CPU time [ms] vs pileup interaction multiplicity

ATLAS Simulation

Monte Carlo $t\bar{t}$ events $\sqrt{s}$ = 14 TeV

2016 Online software

Online beamspot algorithm

Current approach does not scale

- Software/hardware hybrid solution
- Software for seeded precision tracking in RoIs
- Hardware for unseeded tracking
  - **FTK++:** AM chips, same board as L1Track
  - p_T > 1 GeV, for pileup suppression, b-tagging, E_T^{miss}, jet calibration, etc.
- Also studying
  - Hardware/software interplay
  - Software algorithms, parallelisation
  - Use of other hardware accelerators, e.g. GPUs

⊙ **See talk by P Conde Muino**

Summary & conclusions

- ATLAS has a TDAQ design to meet the challenges of HL-LHC

- Two-level hardware trigger based on Regions of Interest, also a single level option.

- Hardware tracking in L1 and EF used to tackle high pileup

- Trend in DAQ from custom hardware to commodity hardware and software

- Baseline will be documented in a TDR, due around the end of 2017
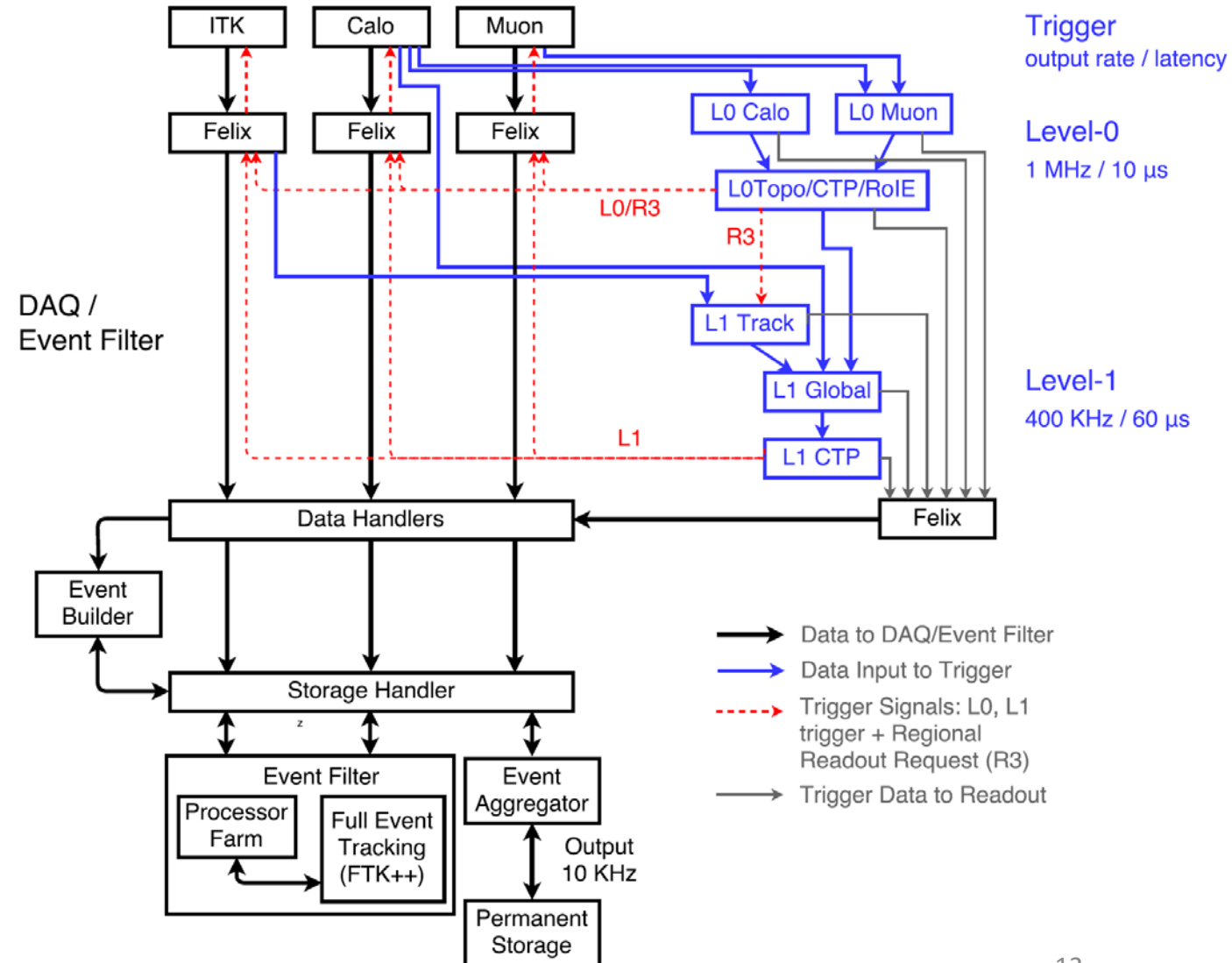
Backup material

HL-LHC physics motivation

- Studies of the light Higgs boson require precision at electroweak scale

- Precision measurement of Higgs couplings are a window into new physics (including much higher mass scales than the LHC)

- Searches for physics Beyond the Standard Model (BSM) may require low cross section processes with large backgrounds, e.g. SUSY

- Subtle BSM physics can only be found if the SM is well understood

- European Strategy report (ECFA), P5 (DOE/NSF): HL-LHC needs at least 3000 fb^{-1} (10 years at $\mathcal{L}$ = 7.5 x 10^{34} cm^{-2}s^{-1})


ATLAS Simulation Preliminary

$\sqrt{s}$ = 14 TeV: $\int$Ldt=300 fb^{-1} ; $\int$Ldt=3000 fb^{-1}
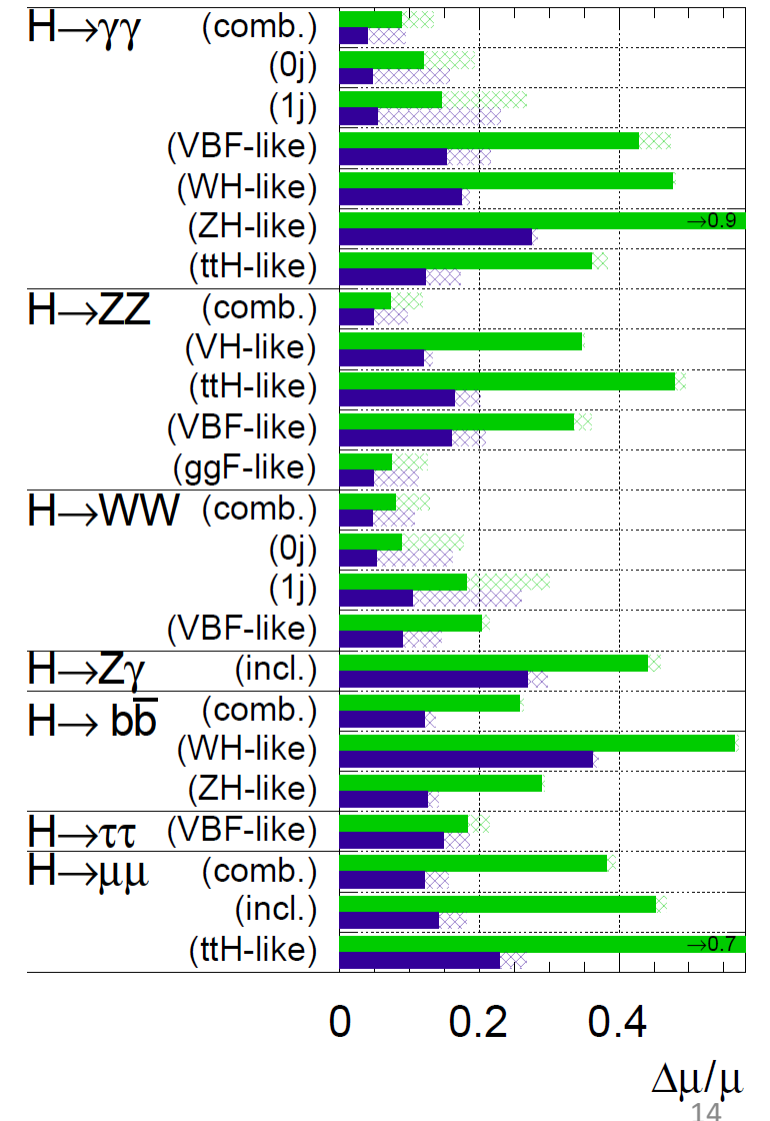
Motivation: Limitations of Run 3 TDAQ system at HL

Item	Run 1 Offline p_T Threshold [GeV]	Run 3 Level-1 system performance at $L = 7.5 \times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$	
		Offline Threshold for Phase-II Goal [GeV]	Level-1 Rate [kHz]
isolated Single e	25	22	200
single μ	25	20	80
di-γ	25	25	8
di-e	17	15	90
di-μ	12	11	10
$e - \mu$	17,6	17,12	8
single τ	100	150	20
di-τ	40,30	40,30	200
single jet	200	180	60
four-jet	55	75	50
E_T^{miss}	120	200	50
jet + E_T^{miss}	150,120	140,125	60

Level-1 rates projected to HL far exceed 100 kHz limit of Run 3 system.
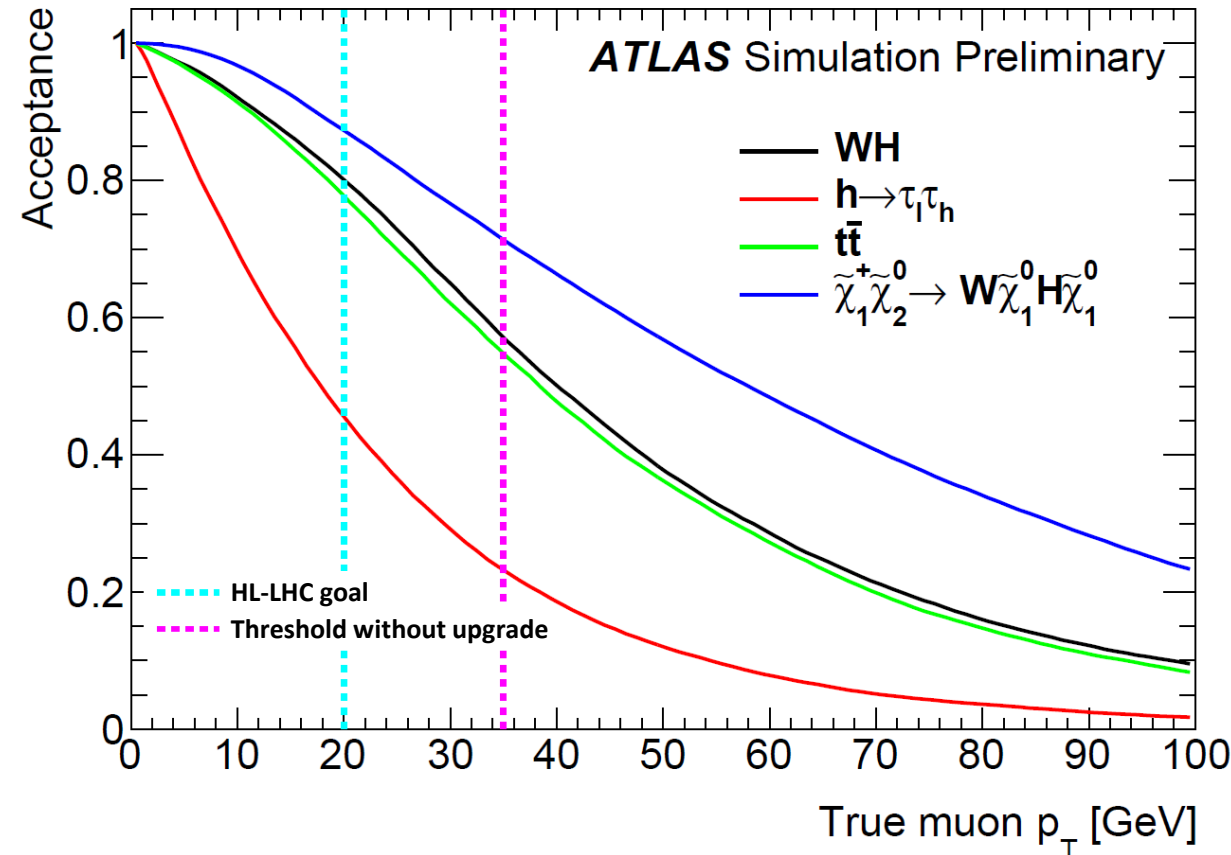
Without upgrade, higher thresholds significantly curtail physics potential.
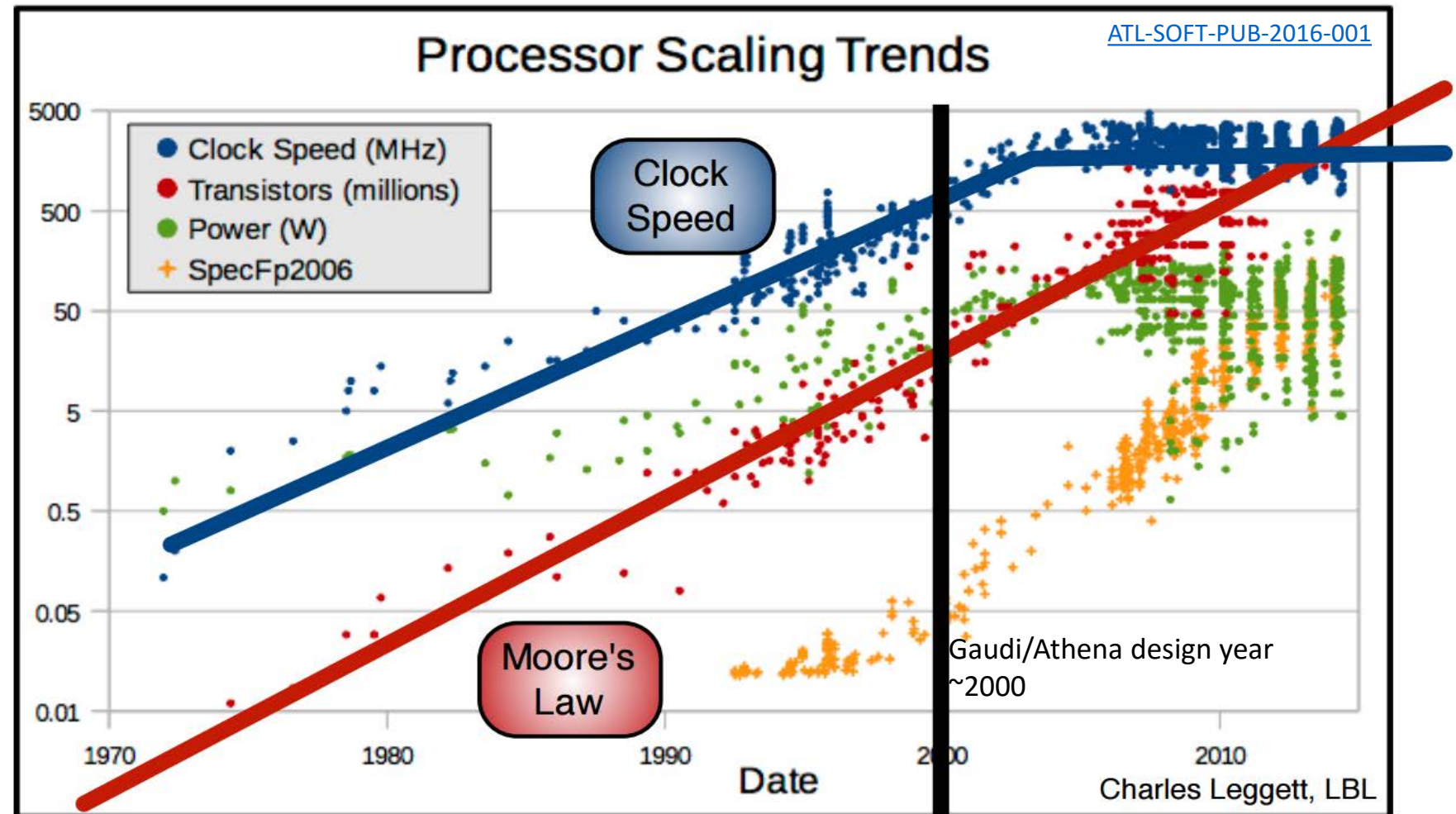
Upgrade motivation: computing evolution

Shift away from clock speed scaling to increasing numbers of cores and other parallel processing features

Commoditisation of co-processors/accelerators

Evolution in programming paradigms, tools and libraries

Computing models and software must adapt

Simon George CHEP 2016

ATL-SOFT-PUB-2016-001

Processor Scaling Trends

- Clock Speed (MHz)
- Transistors (millions)
- Power (W)
- SpecFp2006

Clock Speed

Moore's Law

Gaudi/Athena design year ~2000

Date

Charles Leggett, LBL

Read Out architecture

Front End LInk eXchange (FELIX), routes between **custom serial links** and **commodity multi-gigabit networks**

Versatile link
Low latency link
PON
Switched connection

⊙ **See talk by S Ryu**
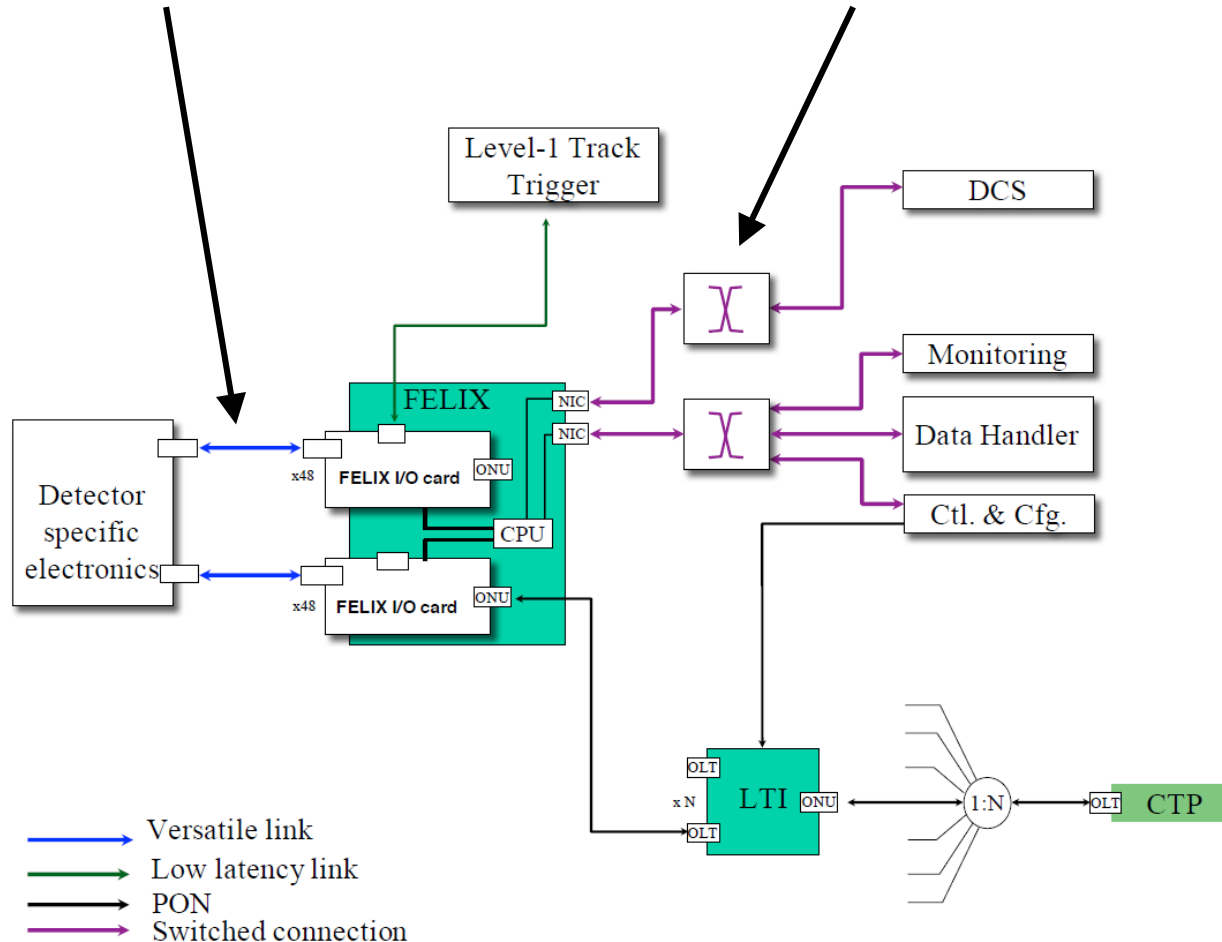
Data Handler

For detector-specific data processing and monitoring. Software toolkit and commodity computers replace custom hardware & firmware