Argonne NATIONAL LABORATORY

FELIX

The new detector readout system for the ATLAS experiment

Front End LInk eXchange

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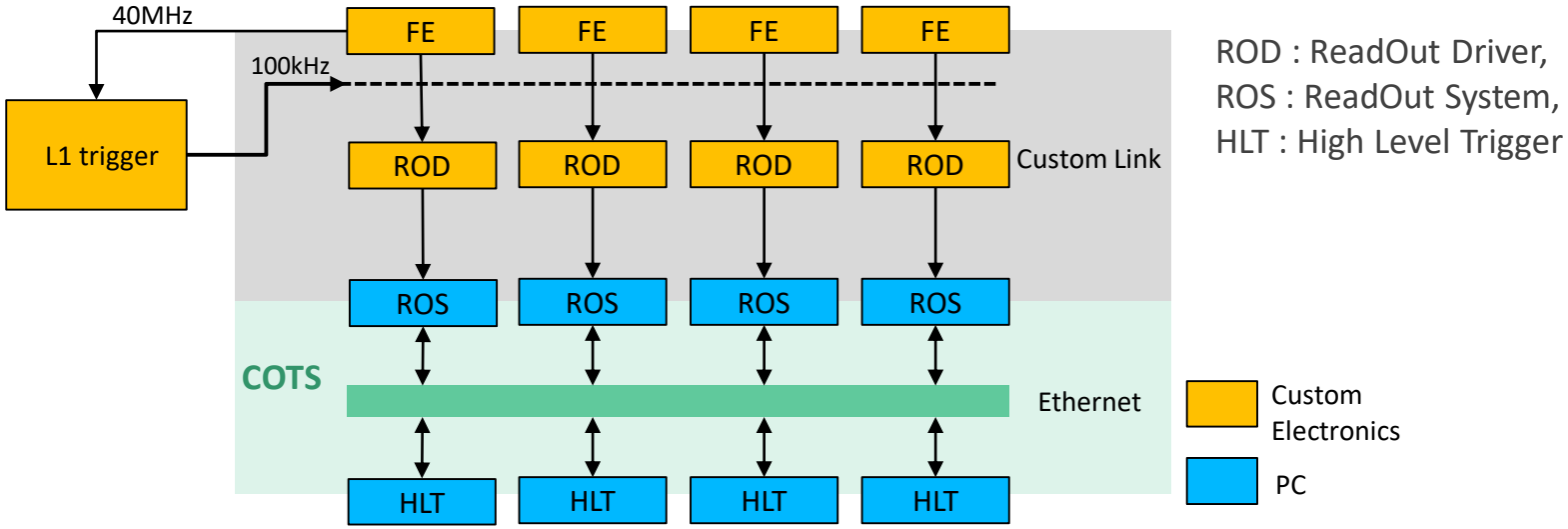
On behalf of the ATLAS Collaboration

ATLAS EXPERIMENT

U.S. DEPARTMENT OF ENERGY

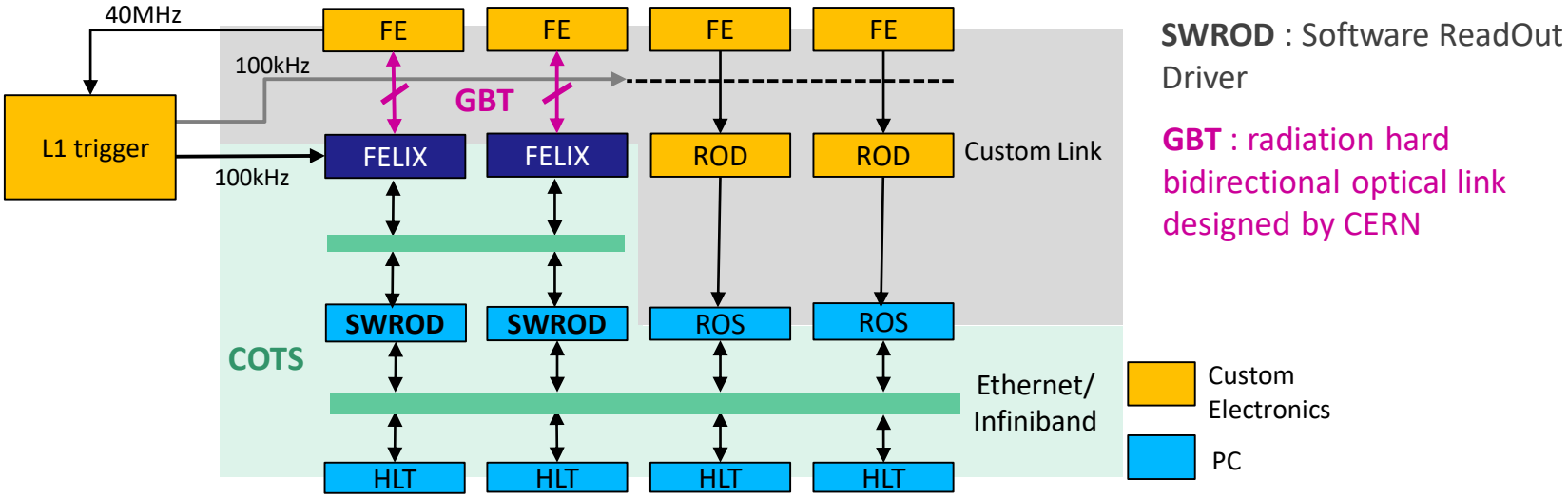
ATLAS DAQ for LHC Run2 (2015-2018)



- Custom hardware and link protocol are used for the frontend readout
  Single dedicated link is needed for each detector channel
- Trigger and LHC clock are given to both front-end and ReadOut Driver

For the next upgrade, introduce more COTS close to the FE

ATLAS DAQ for LHC Run3 (2020-2022)



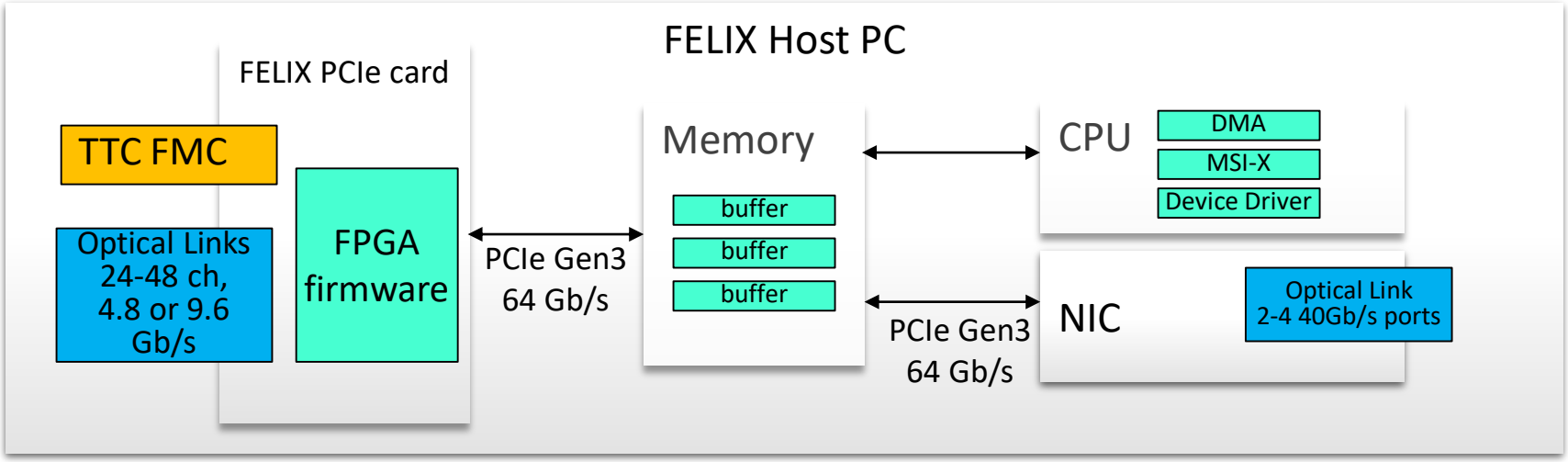
- FELIX will be interfaced to the new muon detector and calorimeter trigger electronics (Run3, 2020)
- What FELIX can do

  Bidirectional Data multiplexing (multiple FEs and multiple network hosts)

  Provisioning of trigger information and LHC clock

FELIX routes the data between FE and network hosts

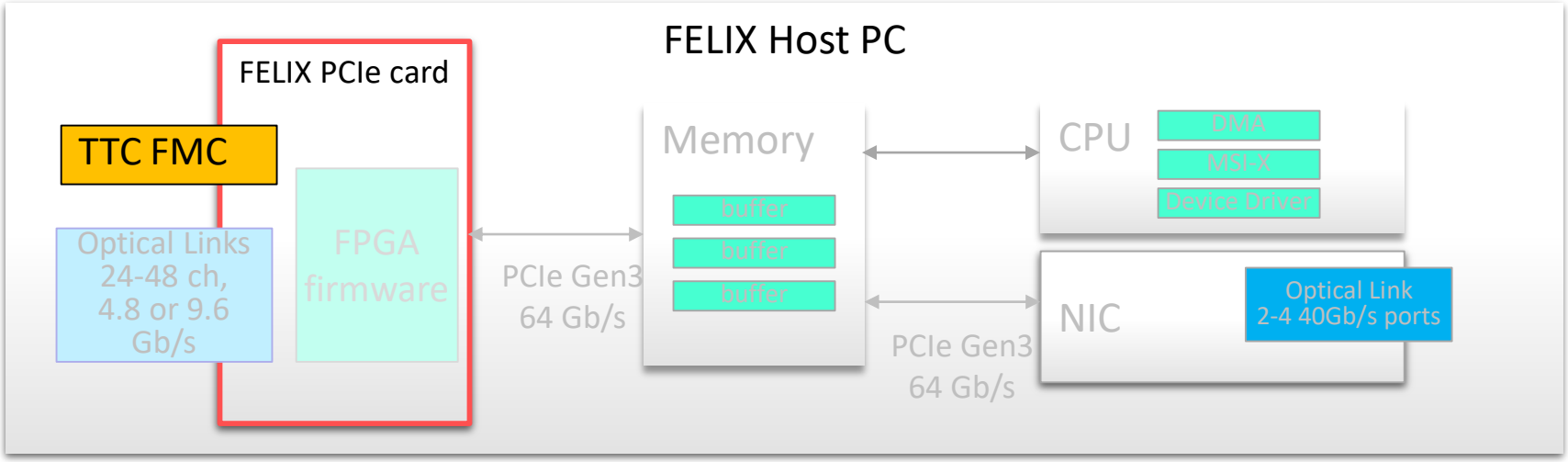
FELIX hardware platform



PCIe card with FPGA chip + Host PC + NIC

TTC (Timing, Trigger and Control) : LHC protocol used to distribute global clock (40.08MHz) and Level 1 trigger information

FELIX hardware components: Development



TTCfx

Custom FMC with TTC input
ver1: ADN2814 + CDCE62005
ver2: ADN2814 + Si5338

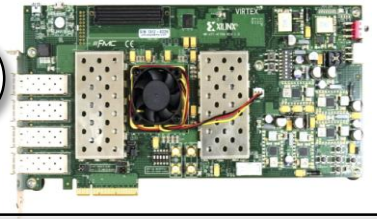
+

FLX-710: HiTech Global HTG-710

Virtex-7 X690T
2 CXP connectors : 24 Ch
PCIe Gen3 x8

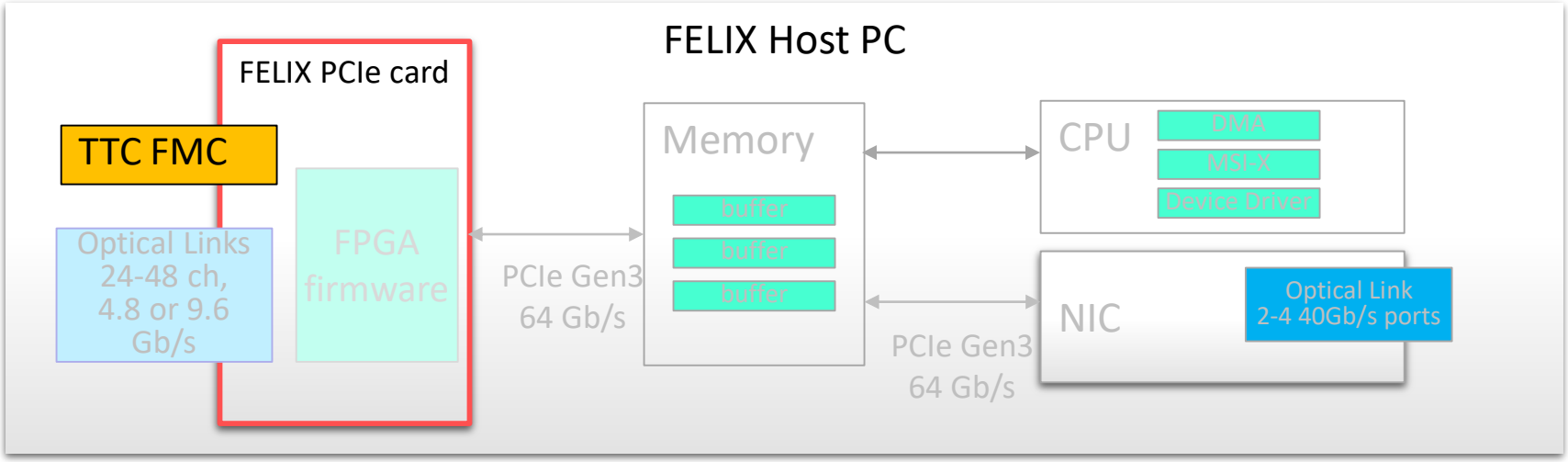
or

FLX-709: Xilinx VC-709



Intended for FE developers
Virtex-7 X690T
4 SPF+ connectors
PCIe Gen3 x8

FELIX hardware components: Production Candidate



FLX-711 from BNL

TTC input ADN2814 + Si5338

Xilinx Kintex Ultrascale XCKU115

48 duplex optical links

PCIe Gen3 x16

FELIX firmware design

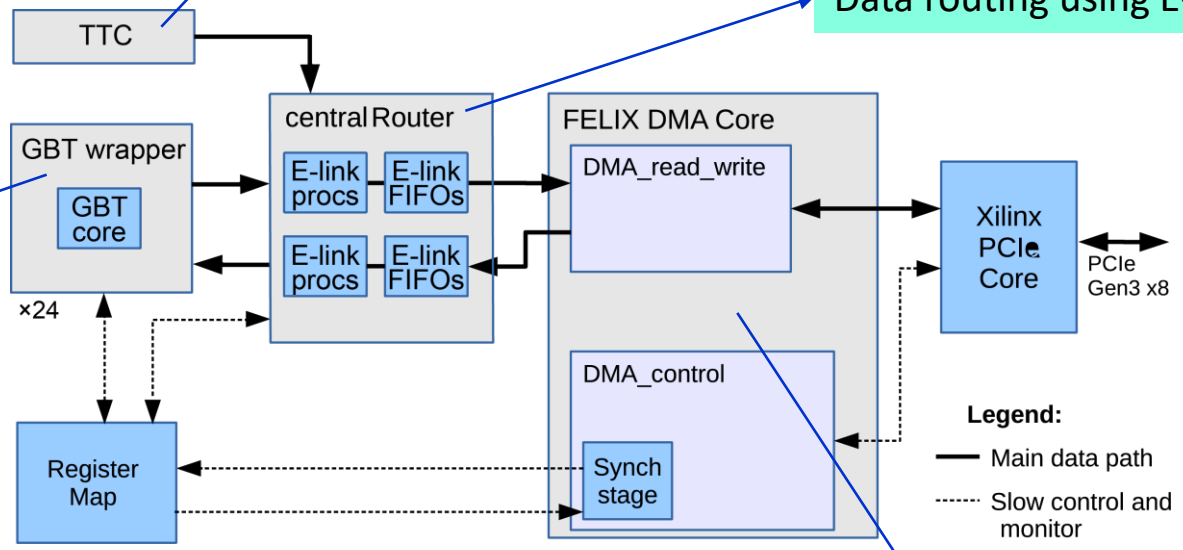
Decoding TTC information and LHC clock recovering

Data routing using E-Link

Optical Link Transceiver using GBT protocol

Two link modes:

GBT-frame mode, Full mode



PCIe DMA engine

E-Link : data multiplexing protocol designed for ATLAS

Available upto 8 GBT links

Fixed latency transmission to FE using LHC clock

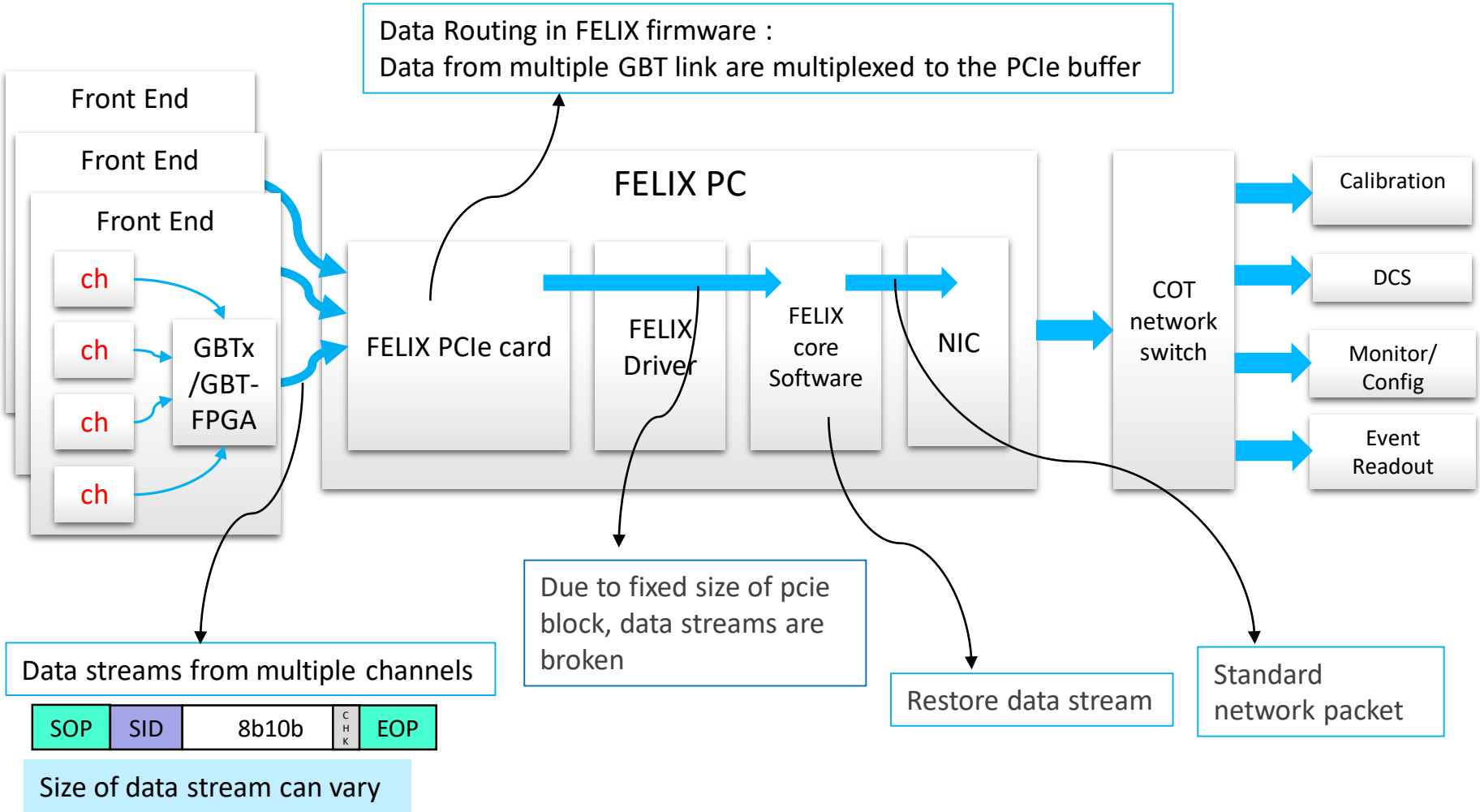
Maximum PCIe throughput to the host PC (~63 Gb/s)

FELIX software

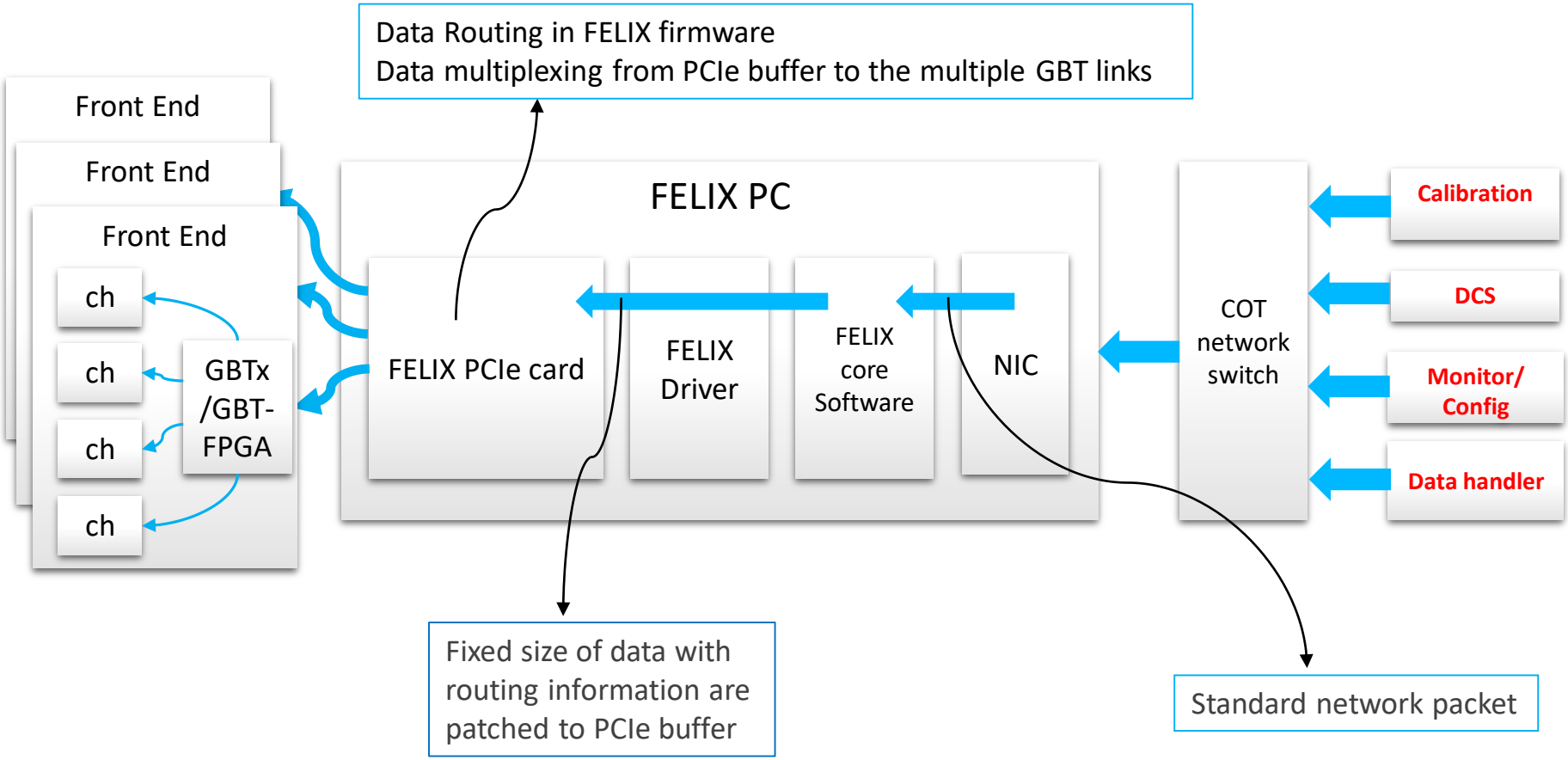
- FELIX Core Application
  Data processing pipeline from(to) the PCIe DMA buffer to(from) the NIC
  - NetIO is used for data exchanging with network hosts.
    abstracts the low level network implementation.
    POSIX and Infiniband backends are supported
    More details on : High-Speed Network Communication with NETIO
- Device Driver and API

- Various types of user tool sets are developed in order to test the FELIX firmware functionalities

FELIX data flow : Front End → Host

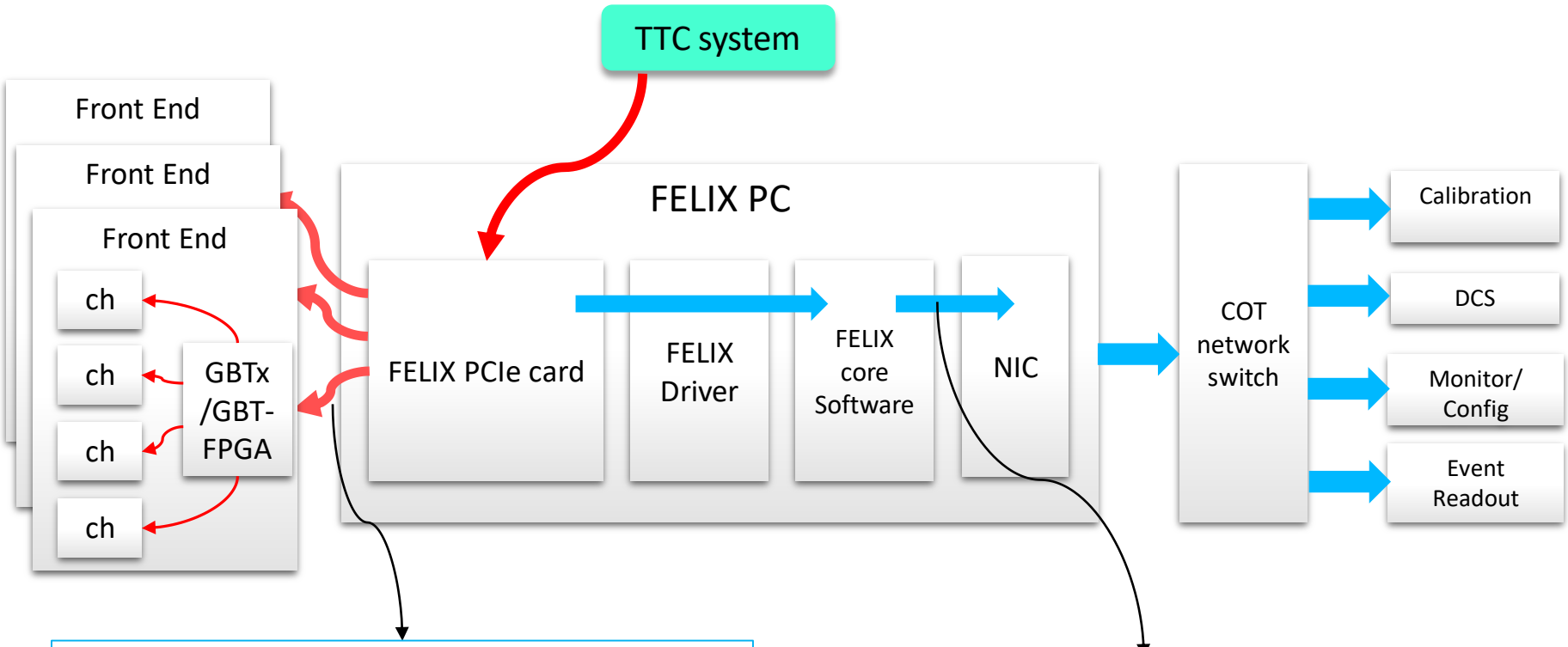


FELIX data flow : Front End ← Host



Data route for calibration, configuration, control and monitoring of detector and FE

FELIX TTC flow : To Front-End and To Host



10bits of TTC information for each GBT links
GBT-frame mode only (4.8 Gb/s)
Fixed Latency data transmission

20 bytes of TTC information to the network hosts

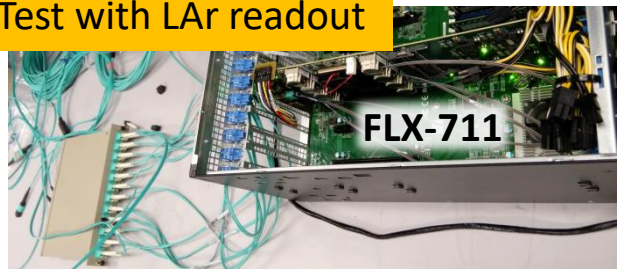
Fixed Latency data transmission
FELIX PCIe card and Front-end are in the same clock domain

FELIX integration test with frontends

- LAr Calorimeter readout (April 2016, LDTB)

  Successful TTC distribution and control and monitoring

Test with LAr readout

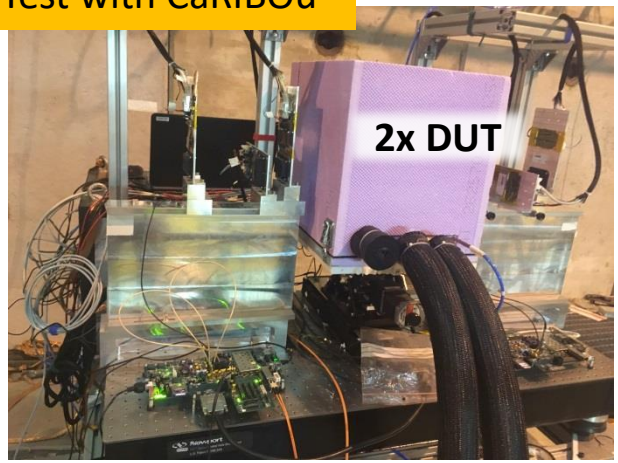


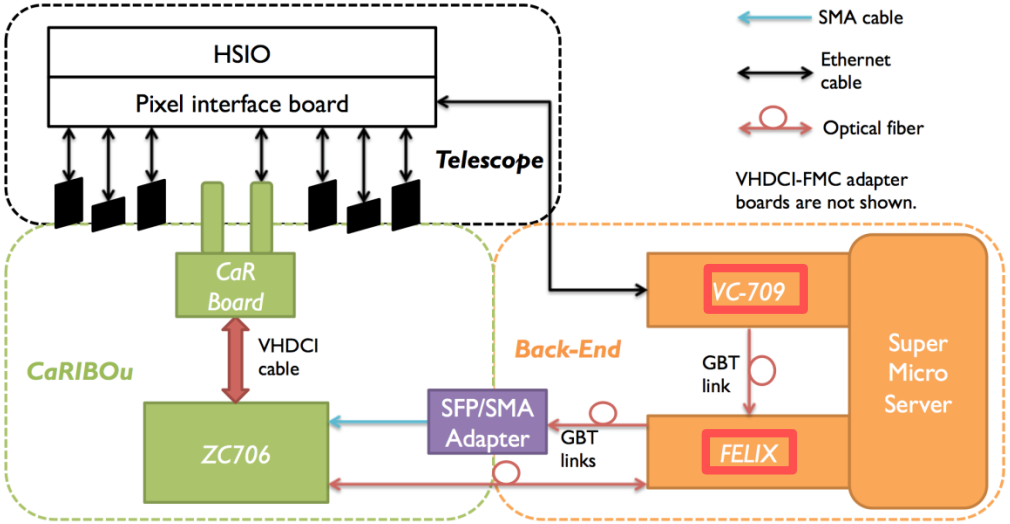
- Pixel detector readout (August 2016, CaRIBOu)

  Test under the beam condition

  Successful data taking in GBT-frame mode (4.8 Gb/s)

Test with CaRIBOu





Summary and prospects

- FELIX is a future interface to the ATLAS detector readout
  - Interface to the new muon and calorimeter trigger electronics in LHC Run 3 (2020)
  - Interface to the All detector readout (2026)
- As most of features are implemented and tested, FELIX is ready to be used for front-end users
  - Ongoing efforts : adding more features, increasing channels to support, bug fix
- Integration tests are on-going