Contribution ID: 485

Type: Oral

## The ATLAS Level-1 Topological Trigger Performance in Run 2

Monday, 10 October 2016 11:30 (15 minutes)

The LHC will collide protons in the ATLAS detector with increasing luminosity through 2016, placing stringent operational and physical requirements to the ATLAS trigger system in order to reduce the 40 MHz collision rate to a manageable event storage rate of about 1 kHz, while not rejecting interesting physics events. The Level-1 trigger is the first rate-reducing step in the ATLAS trigger system with an output rate of up to 100 kHz and decision latency smaller than 2.5 µs. It consists of a calorimeter trigger, muon trigger and a central trigger processor.

During the LHC shutdown after the Run 1 finished in 2013, the Level-1 trigger system was upgraded at hardware, firmware and software levels. In particular, a new electronics sub-system was introduced in the real-time data processing path: the Topological Processor System (L1Topo). It consists of a single AdvancedCTA shelf equipped with two Level-1 topological processor blades. They receive real-time information from the Level-1 calorimeter and muon triggers, which is processed by four individual state-of-the-art FPGAs. It needs to deal with a large input bandwidth of up to 6 Tb/s, optical connectivity and low processing latency on the real-time data path. The L1Topo firmware includes measurements of angles between jets and/or leptons and determination of kinematic variables based on lists of selected or sorted trigger objects. All these complex calculations are executed in hardware within 200 ns. Over one hundred VHDL algorithms are producing trigger outputs that are incorporated into the logic of the central trigger processor, responsible of generating the Level-1 acceptance signal. The detailed additional information provided by L1Topo, will improve the ATLAS physics reach in a harsher collisions environment.

The system has been installed and commissioning started during 2015 and continued during 2016. As part of the firmware commissioning, the physics output from individual algorithms needs to be simulated and compared with the hardware response. An overview of the design, commissioning process and early impact on physics results of the new L1Topo system will be illustrated.

## **Tertiary Keyword (Optional)**

Processor architectures

## Secondary Keyword (Optional)

Algorithms

## **Primary Keyword (Mandatory)**

Trigger

Primary author: PANDURO VAZQUEZ, Jose Guillermo (Royal Holloway, University of London)

Co-author: RIU, Imma (IFAE Barcelona (ES))

Presenter: RIU, Imma (IFAE Barcelona (ES))

Session Classification: Track 1: Online Computing

Track Classification: Track 1: Online Computing