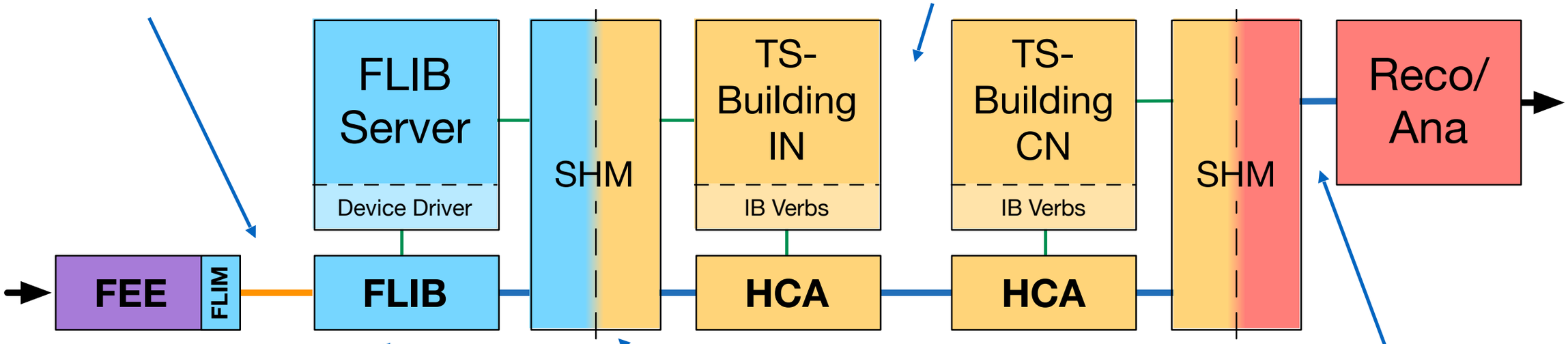
FLES Data Flow

- 10 GBit/s custom optical link
- Common front-end interface module

- Timeslice building
- InfiniBand RDMA, true zero-copy

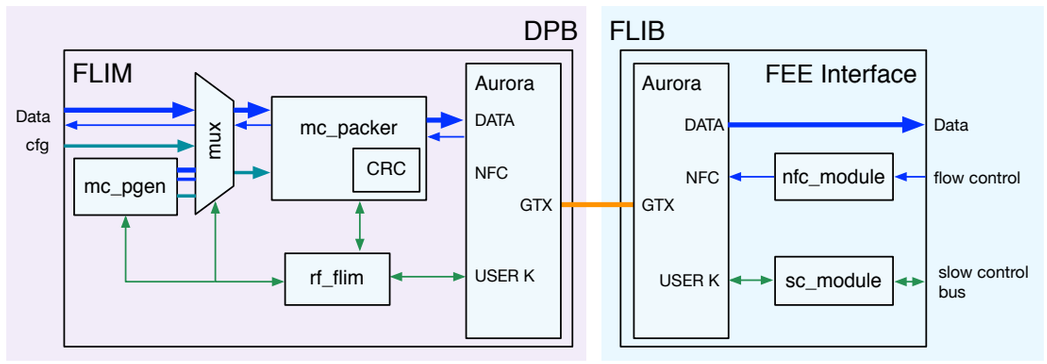


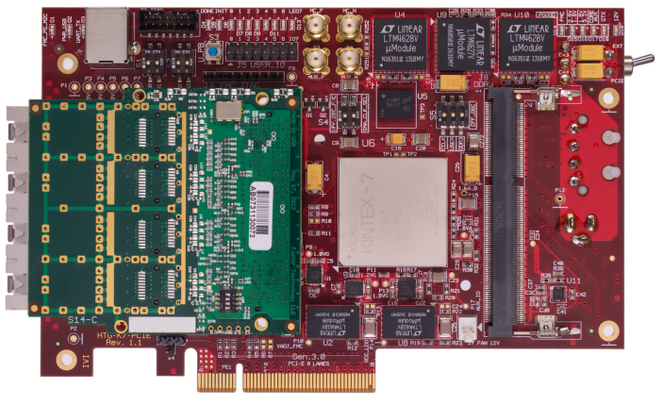
- Data preprocessing for timeslice building
- Full offload PCIe DMA engine

- Direct DMA to InfiniBand send buffers
- Shared memory interface

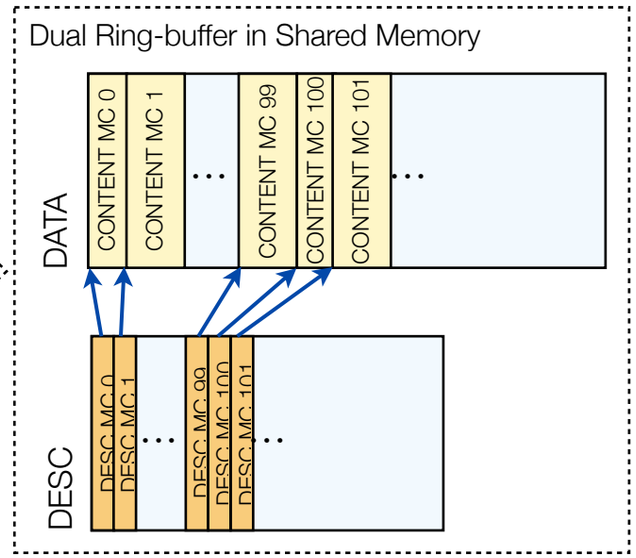
- Indexed access to timeslice data

FLES Input Interface





FLES Interface Board (FLIB)



- PCIe FPGA board with custom HDL design
- 10 Gbit/s optical link to front-end electronics
- Full offload DMA engine manages dual ring buffer structure
  - Buffer for data content & Buffer for index table and meta data
- Posix shared memory DMA buffers
  - Data access via shared memory interface, no linking to device driver
  - Usable by other DMA applications w/o extra copy, e.g. InfiniBand RDMA