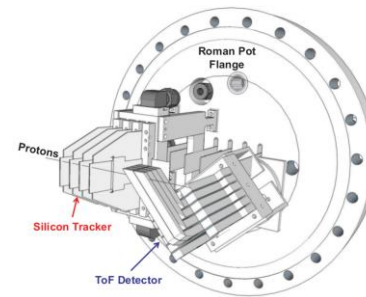
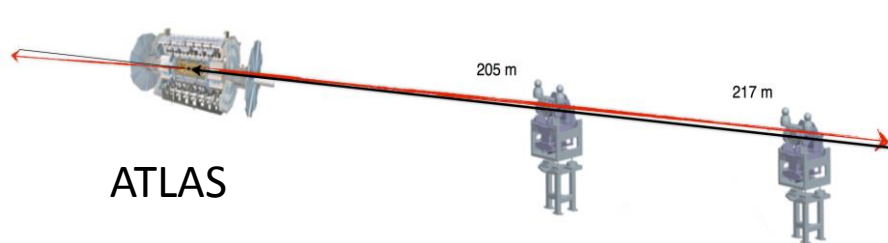


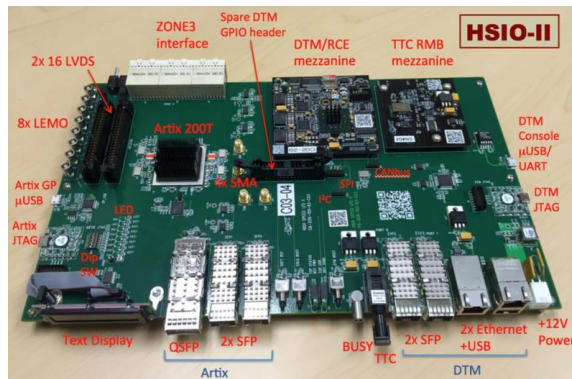
Readout and Trigger for the AFP detector at the ATLAS experiment at LHC



Two sets of 4 Si modules at 205 and 217 m from ATLAS IP

- trigger signals from modules are locally ANDed, synchronized with LHC clock and sent over air-core cables to reach ATLAS Central Trigger Processor (CTP) within the first trigger level latency limit (85 BCXs).
- in counting house signals are split for standalone and for ATLAS CTP in combined runs.
- readout of accepted events goes over fiber ribbons at 160 Mbps.

All functionality required in for the integration with the ATLAS TDAQ is contained in a single Artix FPGA at HSIO board.



Event Fragment Builder creates ATLAS event fragments : one per arm, flags errors and monitors data flow. Information is passed from Artix via a custom protocol PGP to RCE which communicates with ATLAS RodCrateDAQ (RCD) and uses ATLAS infrastructure to publish relevant info.