

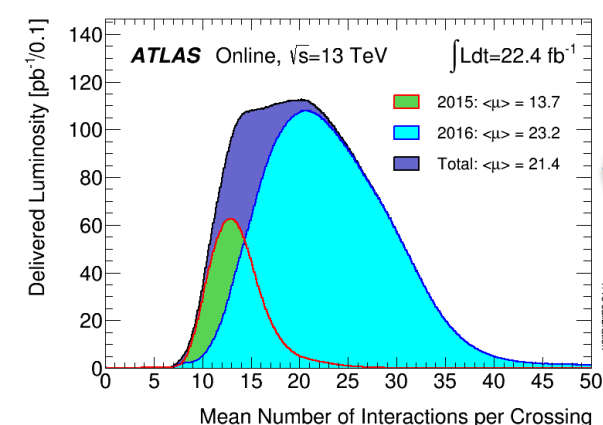
22nd International Conference on Computing in High Energy and Nuclear Physics - October 10-14 2016, San Francisco

During 2013-2015 long shutdown, the Trigger and Data Acquisition system of the ATLAS Detector at CERN underwent a major program of improvements in preparation for the more challenging LHC collision environment at 13 TeV during Run 2.

Run 2 also saw integration of **new detector components**, as well as expansion of **readout bandwidth** from existing systems. **Input and output rate requirements** for the system also **increased**.

New requirements satisfied using new hardware and software technologies system-wide. Updated system more robust, scalable and performant.

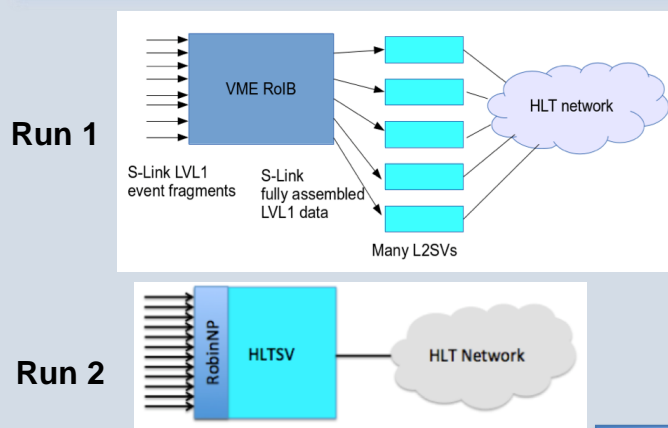
	Run 1	Run 2 (peak)
Pileup	21	40
L1 Trigger Rate (kHz)	70	100
HLT Trigger Rate (kHz)	0.6	1.5
Event Size (MB)	1.5	1.6
Offline Data Recording Rate (GB/s)	1	1.5



High Level Trigger (HLT) processing seeded by detector **regions of interest** built from Level 1 (L1) trigger results.

Original VME based Region of Interest Builder (RoIB) migrated to software and integrated with merged HLT Supervisor (HLTSV) using RobinNP.

Able to support higher L1 rates while moving to more maintainable hardware.



12 x 6 Gb/s optical link

2x DDR3 SODIMM

1156-pin Xilinx Virtex 6 FPGA

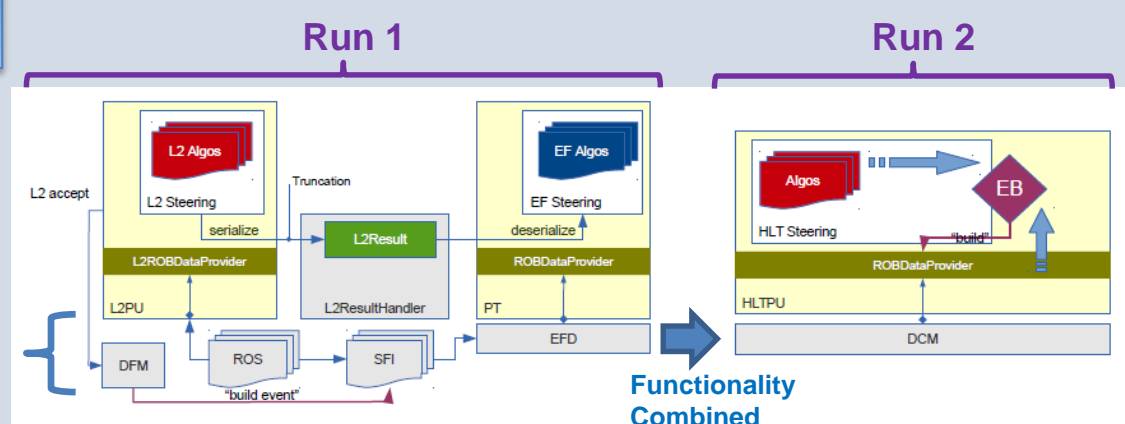
Gen2 x8 PCI Express

**Updated Readout System (ROS)
based on RobinNP PCIe card**

3 x Link Density increase
20 x Output bandwidth increase
10 x Buffer capacity increase
Improved monitoring and diagnostics

Merger of previous Region of Interest based **Level 2 farm** with full event **'filter' farm** into one. Processing merged at HLT algorithm level.

Streamlined processing with reduced data transport needs facilitating better **load balancing** and eliminating need to distribute resources manually between farms.

[illegible]

Overhauled **dataflow infrastructure** supporting new merged HLT and evolved RoI.

New Data Collection Manager (DCM) combining and streamlining functionality of multiple components.

Software infrastructure updated for fully **64 bit processing**, making use of new technologies and standards such as **C++11** and **boost**. Migrating throughout 2016 to modern build and management tools such as **Git** and **CMake**.



Multiple updates across control and monitoring software. Also presented at CHEP 2016:

A web-based solution to visualize operational monitoring data in the Trigger and Data Acquisition system of the ATLAS experiment at the LHC.
I. Soloviev, G. Avolio.

The Resource manager of the ATLAS Trigger and Data Acquisition system. **I. Alexandrov.**

Integrated monitoring of the ATLAS online computing farm. D. Fazio.

Master of Puppets. C. Lee.

The diagram illustrates the network architecture for the ATLAS cavern, showing connections between various components and their link utilization.

Link utilization legend:

- 0 - 20 % (Green)
- 20 - 40 % (Orange)
- 40 - 60 % (Red)
- 60 - 80 % (Purple)
- 80 - 100 % (Blue)

Components and Connections:

- ROS (x98):** Connected to the Router cluster via 4 x 10 Gbps links (Orange).
- RoIB/HLTSV (x1):** Connected to the Router cluster via 2 x 10 Gbps links (Orange).
- Router cluster:** Consists of two core switches, **sw-data-core-01** and **sw-data-core-02**, connected by an 8 x 10 Gbps link (Green).
- TPU (x50):** Connected to the Router cluster via 2 x 10 Gbps links (Red). The TPU is also connected to a **sw-data-tpu-sw** switch (1 Gbps) and a **sw-data-tpu-sw** switch (x40).
- SFO (x6):** Connected to the Router cluster via 2 x 10 Gbps links (Orange). The SFO is also connected to a **sw-data-edge-01** switch (2 x 10 Gbps) and a **sw-data-edge-01** switch (8 x 10 Gbps).
- CERN Permanent Storage:** Connected to the Router cluster via 8 x 10 Gbps links (Blue).

Physical Infrastructure:

- Patch panel ATLAS cavern** and **Patch panel Surface** are shown as horizontal lines.
- The distance between the patch panels is **150 m**.

Redesigned **dataflow network** combining two previous networks into one. Making use of new **multi chassis trunking** technology to providing **40 GbE capability** to each ROS PC with **active-active redundancy**.

Deep buffer **top-of-rack switches** installed significantly **reducing event building time** by reducing rate of packet drops and retransmissions.

Evolved **data logger (SFO)**, making use of **state-of-the-art storage and processing technology** and **reworked multi-threading processing model**.

Capable of meeting new output bandwidth and availability requirements, with **large buffer** able to store up to 24 hours of collision data.