YARR

A PCIe based readout concept for current and future ATLAS Pixel Modules

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Old concept:
• Link between Read-Out-Driver and host computer in crate like architectures slow
• Use FPGAs as hardware accelerator and perform lossy compression in form of histogramming to bypass slow link
• Creates the need to contain complicated logic in not very accessible language, which creates a steep entry level for beginners
• Firmware/Software bound to specific hardware

YARR concept:
• Use high speed PCIe link to transfer all data directly into the host computer
• PCIe FPGA only acts as reconfigurable I/O interface and does not perform any processing
• All data processing is performed in software, making it more accessible for beginners
• Inherently hardware agnostic, as it build around the Front End data
Data flow:
- Each processing step is independent of the other, which enables flexible connection of different block.
- Furthermore, it enables parallel processing and efficient usage of modern CPU architectures.
- Even though this version is fully contained in software, it would be possible to move certain blocks to hardware if acceleration is needed.
- The only interprocess communication needed is the feedback from the analysis to the scan loop to tune the Front End.