Contribution ID: 520

Type: Poster

YARR - A PCIe based readout concept for current and future ATLAS Pixel Modules

Thursday 13 October 2016 16:30 (15 minutes)

The Yet Another Rapid Readout (YARR) system is a DAQ system designed for the readout of current generation ATLAS Pixel FE-I4 and next generation ATLAS ITk chips. It utilises a commercial-of-the-shelf PCIe FPGA card as a reconfigurable I/O interface, which acts as a simple gateway to pipe all data from the pixel chips via the high speed PCIe connection into the host systems memory. Relying on modern CPU architectures which enables the usage of parallelised processing threads and commercial high speed interfaces in everyday computers, it is possible to perform all processing on a software level in the host CPU. Although FPGAs are very powerful at parallel signal processing their firmware is hard to maintain and constrained by their connected hardware, software on the other hand is very portable and upgraded frequently with new features coming at no cost. A DAQ concept which does not rely on the underlying hardware for acceleration also eases the transition from prototyping in the laboratory to the full scale implementation in the experiment. The overall concept and data flow will be outlined, as well as the challenges and possible bottlenecks which can be encountered when moving the processing from hardware to software.

Tertiary Keyword (Optional)

Secondary Keyword (Optional)

Primary Keyword (Mandatory)

DAQ

Primary author: HEIM, Timon (Lawrence Berkeley National Lab. (US))

Co-authors: HINCHLIFFE, Ian (Lawrence Berkeley National Lab. (US)); GARCIA-SCIVERES, Mauricio (Lawrence Berkeley National Lab. (US))

Presenter: HEIM, Timon (Lawrence Berkeley National Lab. (US))

Session Classification: Posters B / Break

Track Classification: Track 1: Online Computing