Contribution ID: **161** Type: **Oral**

Multi-threaded Geant4 on Intel Many Integrated Core architectures

Tuesday, 11 October 2016 14:15 (15 minutes)

In the midst of the multi- and many-core era, the computing models employed by HEP experiments are evolving to embrace the trends of new hardware technologies. As the computing needs of present and future HEP experiments -particularly those at the Large Hadron Collider- grow, adoption of many-core architectures and highly-parallel programming models is essential to prevent degradation in scientific capability.

Simulation of particle interactions is typically a major consumer of CPU resources in HEP experiments. The recent release of a highly performant multi-threaded version of Geant4 opens the door for experiments to fully take advantage of highly-parallel technologies.

The Many Integrated Core (MIC) architecture of Intel, known as the Xeon Phi family of products, provide a platform for highly-parallel applications. Their large number of cores and Linux-based environment make them an attractive compromise between conventional CPUs and general-purpose GPUs. Xeon Phi processors will be appearing in next-generation supercomputers such as Cori Phase 2 at NERSC.

To prepare for tusing hese next-generation supercomputers, a Geant4 application has been developed to test and study HEP particle simulations on the MIC Intel architectures (HepExpMT). This application serves as a demonstrator of the feasibility and computing-opportunity of utilizing this advanced architecture with a complex detector geometry.

We have measured the performances of the application on the first generation of Xeon Phi coprocessors (code name Knights Corner, KNC). In this work we extend the scalability measurements to the second generation of Xeon Phi architectures (code name Knights Landing, KNL) in preparation of further testing on Cori Phase 2 supercomputer at NERSC.

Tertiary Keyword (Optional)

Parallelization

Secondary Keyword (Optional)

Simulation

Primary Keyword (Mandatory)

High performance computing

Primary authors: DOTTI, Andrea (SLAC National Accelerator Laboratory (US)); ASAI, Makoto (SLAC National Accelerator Laboratory (US)); FARRELL, Steven Andrew (Lawrence Berkeley National Lab. (US))

Presenter: DOTTI, Andrea (SLAC National Accelerator Laboratory (US))

Session Classification: Track 5: Software Development

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