GEORG-AUGUST-UNIVERSITÄT
GÖTTINGEN

Highlights-138

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on behalf of the ATLAS Collaboration

BMBF-Forschungsschwerpunkt
ATLAS-EXPERIMENT
Physik bei höchsten Energien mit dem ATLAS-Experiment am LHC
FSP 103
ATLAS
INSPIRE
Bundesministerium
für Bildung
und Forschung

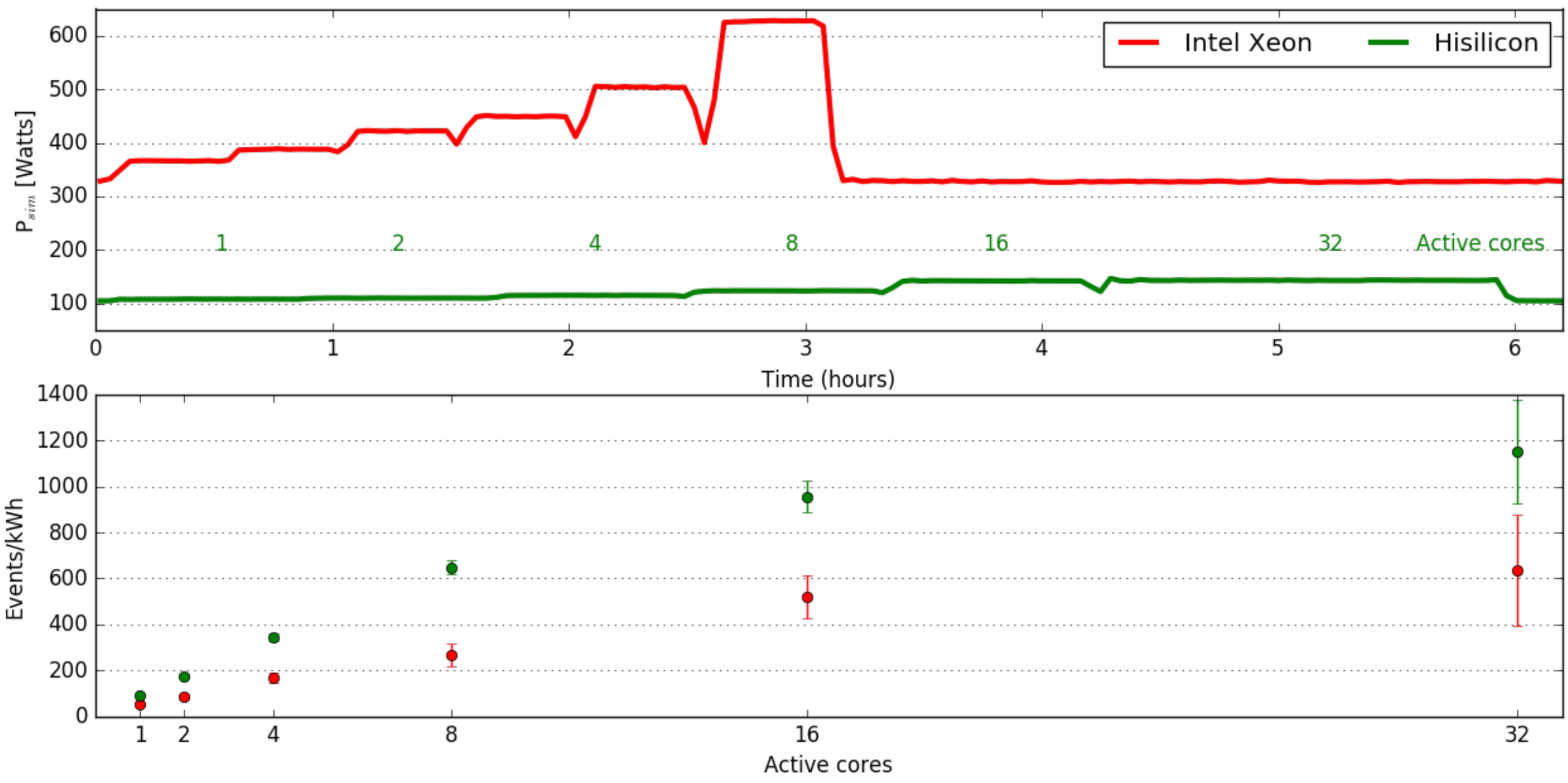
Highlights

- Lots of ATLAS workloads not necessarily CPU intensive (apart from MC Generation)
  - Don’t need high Gflops as top requirement
- How do specifically designed power efficient architectures perform?
- Building for one architecture can be unhealthy
  - Compiler specific code emerges
- More architectures are always being developed

ARM: One such power efficient architecture

- ARM = Advanced RISC Machine
  - RISC = Reduced Instruction Set Computer
- Found in ~95% of smartphones and tablets
- 64-bit (Aarch64) available
- A company that sells its rights to its Intellectual Property.

Highlights



ARM is between ~1.7 and ~2.5 more efficient when performing an ATLAS $t\bar{t}$ simulation!