



# Future of Compute is Big Data

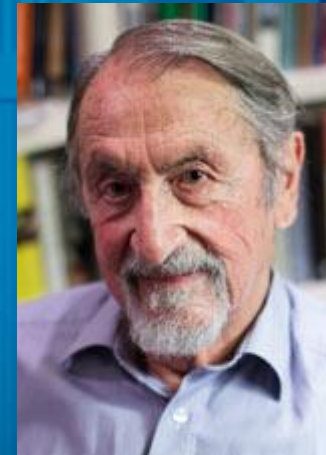
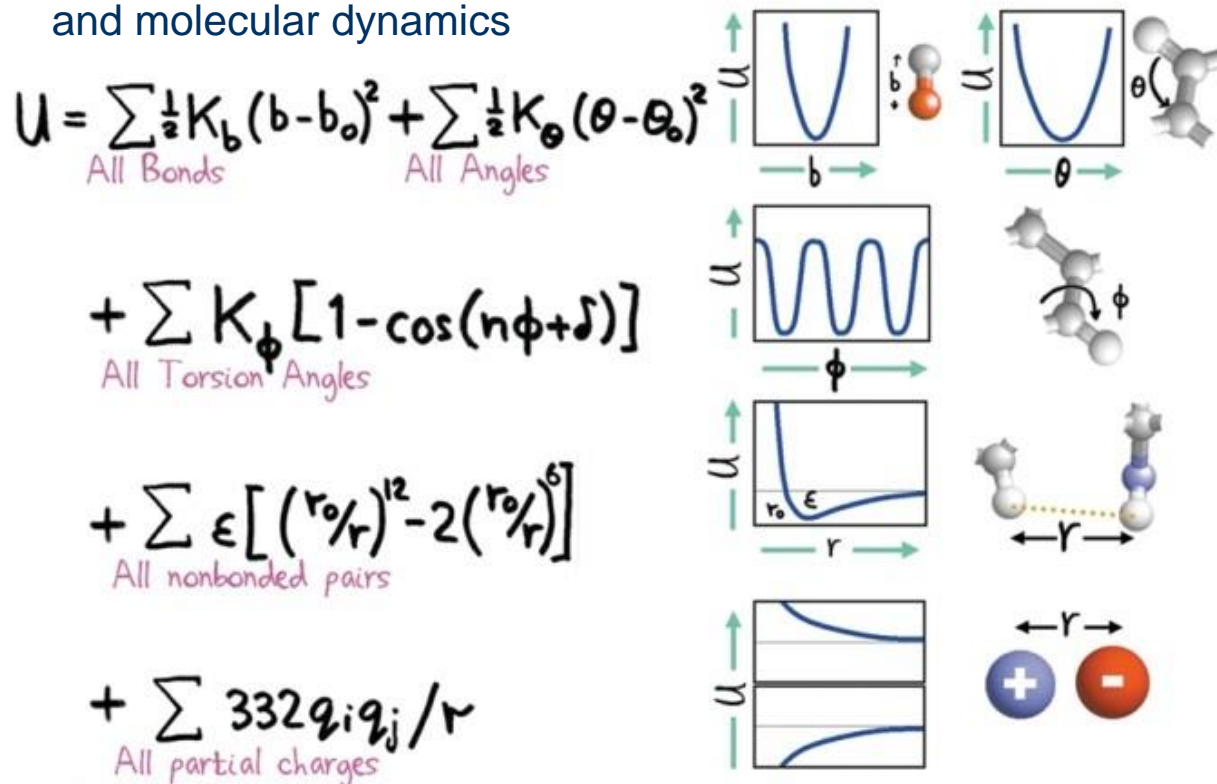
**Mark Seager**  
Intel Fellow,  
CTO for HPC Ecosystem  
Intel Corporation

# Traditional HPC is scientific simulation

## First ever Nobel prize for HPC takes the experiment into cyberspace

Chemical reactions occur at lightning speed; electrons jump between atoms hidden from the prying eyes of scientists. The Nobel Laureates in Chemistry 2013 have made it possible to map the mysterious ways of chemistry by using computers. Detailed knowledge of chemical processes makes it possible to optimize catalysts, drugs and solar cells.

Spanning multiple scales by combining quantum mechanics and molecular dynamics



**Martin Karplus Michael Levitt Arieh Warshel**

The Nobel Prize in Chemistry 2013 was awarded jointly to Martin Karplus, Michael Levitt and Arieh Warshel "for the development of multi-scale models for complex chemical systems".





# Other emerging technical computing usage models are driven by Big Data

## Government & Research



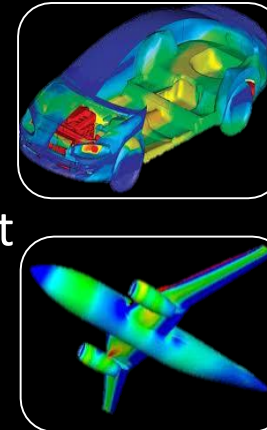
"My goal is simple. It is complete understanding of the universe, why it is as it is, and why it exists at all"

Stephen Hawking

Basic Science

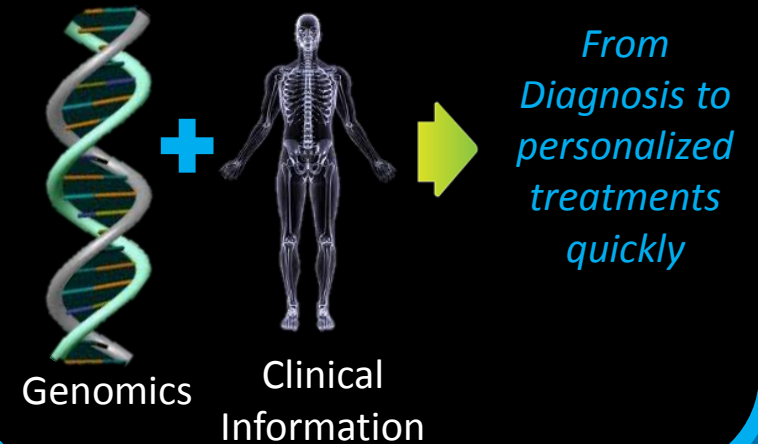
## Commerce & Industry

Better Products  
Digital Twin  
Faster Time to Market  
Reduced R&D  
New Business Models  
Data Services



Business Transformation

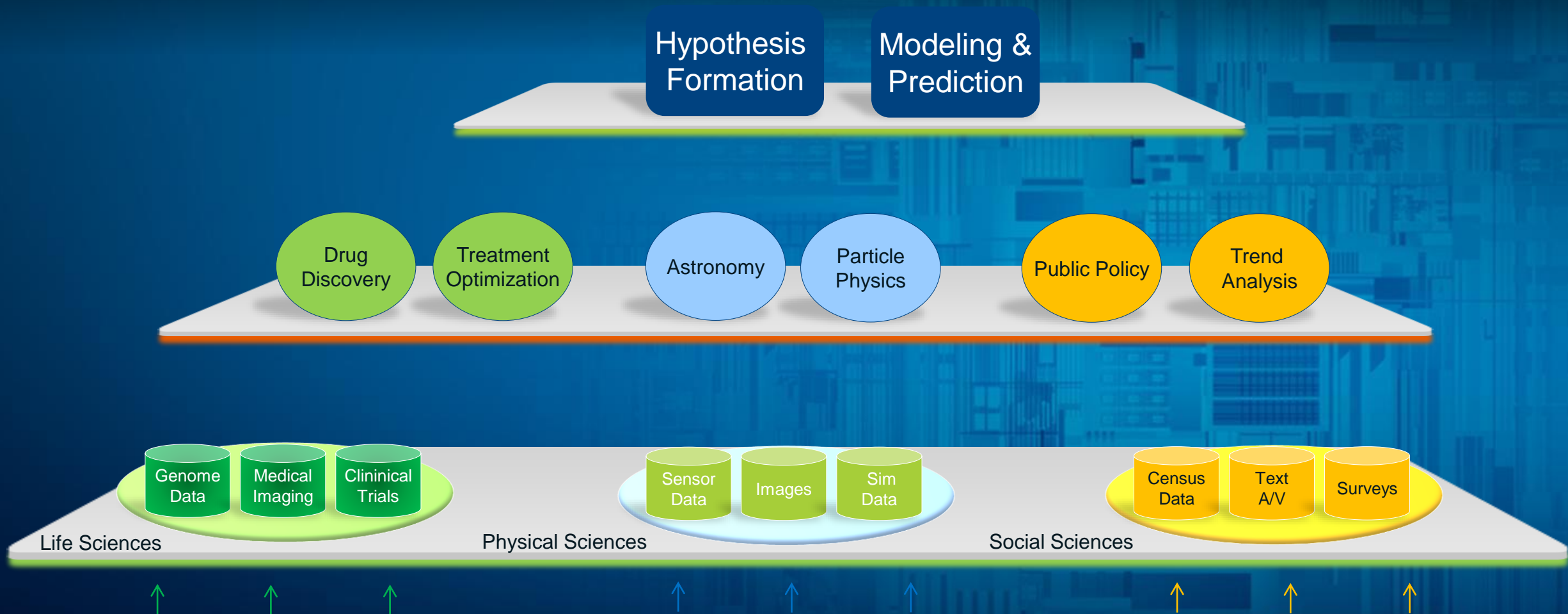
## New Users & New Uses



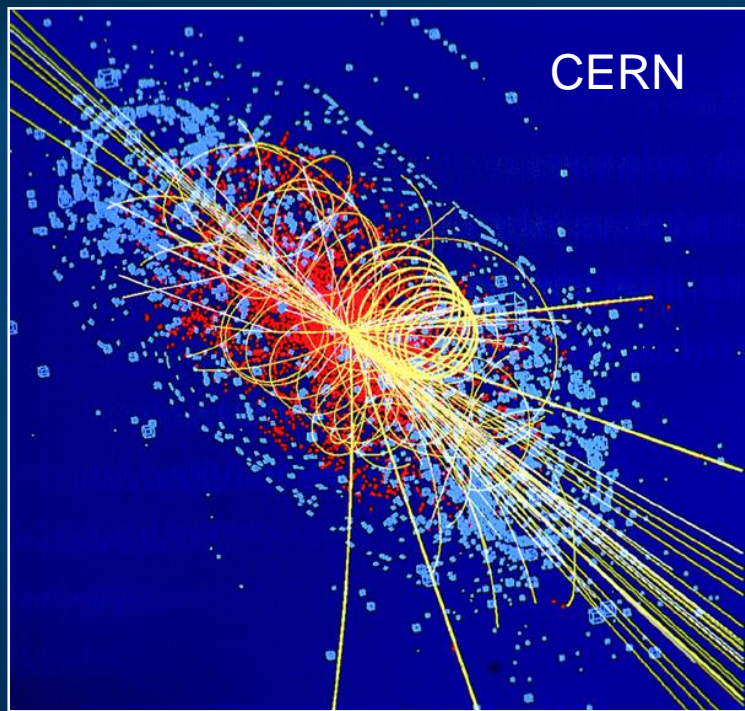
Data-Driven Discovery

# Transform data into useful knowledge

# Data-Driven Discovery



# Data-Driven Discovery in Science



600 million collisions / sec

Detecting 1 in 1 trillion events to help find the Higgs Boson



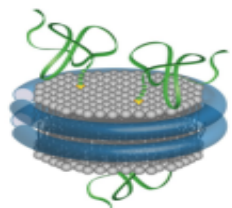
1 human genome = 1 petabyte

Finding patterns in clinical and genome data at scale can cure cancer and other diseases

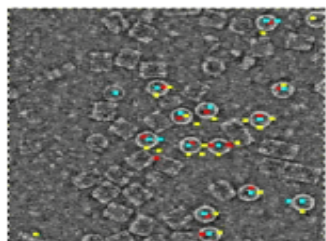


# Project Moonshot for Cancer: Predictive Oncology Pilot 2

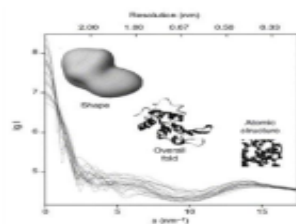
## RAS activation experiments at NCI/FNL



Experiments on nanodisc



CryoEM imaging



X-ray/neutron scattering

Multi-modal experimental data, image reconstruction, analytics

Protein structure databases

## New adaptive sampling molecular dynamics simulation codes

Adaptive time stepping

Coarse-grain MD

Classical MD

Quantum MD

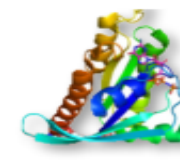
Adaptive spatial resolution

High-fidelity subgrid modeling

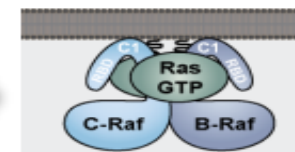
## Predictive simulation and analysis of RAS activation



Granular RAS membrane interaction simulations

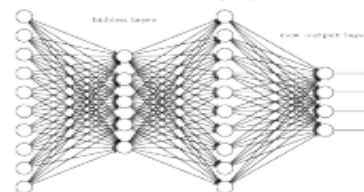


Atomic resolution sim of RAS-RAF interaction



Inhibitor target discovery

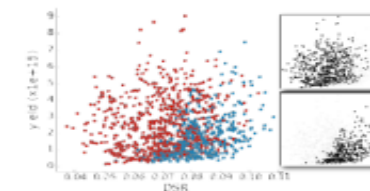
## Machine learning guided dynamic validation



Unsupervised deep feature learning



Mechanistic network models



Uncertainty quantification

# Convergence of Driving Forces

## Intelligent Devices



**19B**

Connected devices  
by 2016<sup>1</sup>

## Cloud



**\$200B**

Cloud services  
In 2016<sup>2</sup>

## HPC



**2X**

Annual growth in  
supercomputing  
FLOPS<sup>3</sup>

## Big Data



**15PB**

Data collected in  
1 year at CERN<sup>4</sup>

<sup>1</sup> Source: Cisco® Visual Networking Index (VNI) Forecast (2011-2016)

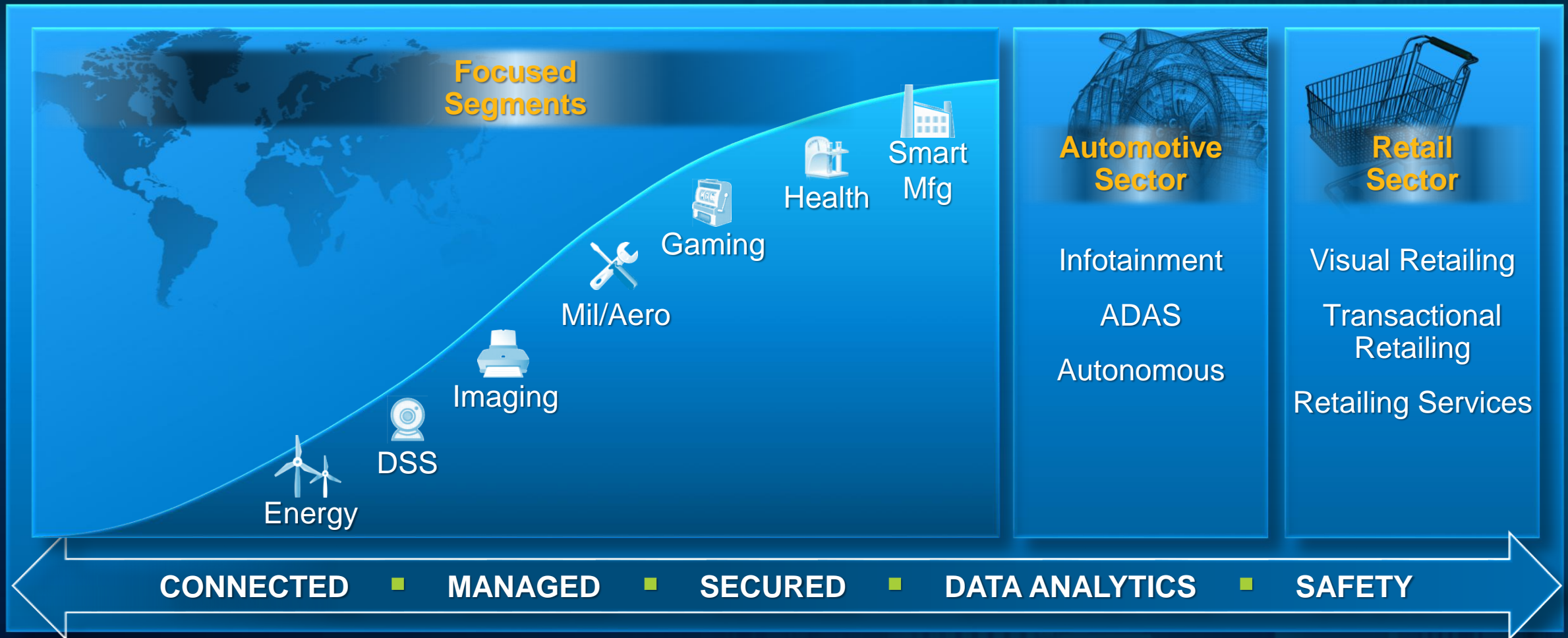
<sup>2</sup> Source: Gartner Worldwide IT Spending Forecast, 2Q12 Update

<sup>3</sup> Source: Top 500 list: Top 10 change from November 2007 to November 2012

<sup>4</sup> Source: CERN



# Intelligent Devices - New Era of Computing Enabling an Industry of Pervasive Computing





# INTEL GIVING SIGHT TO MACHINES IN THE AI AGE

THROUGH INNOVATION & ACQUISITION

## CAPABILITIES

MACHINE &  
DEEP LEARNING

COGNITIVE  
COMPUTING

PROGRAMMABLE  
SOLUTIONS

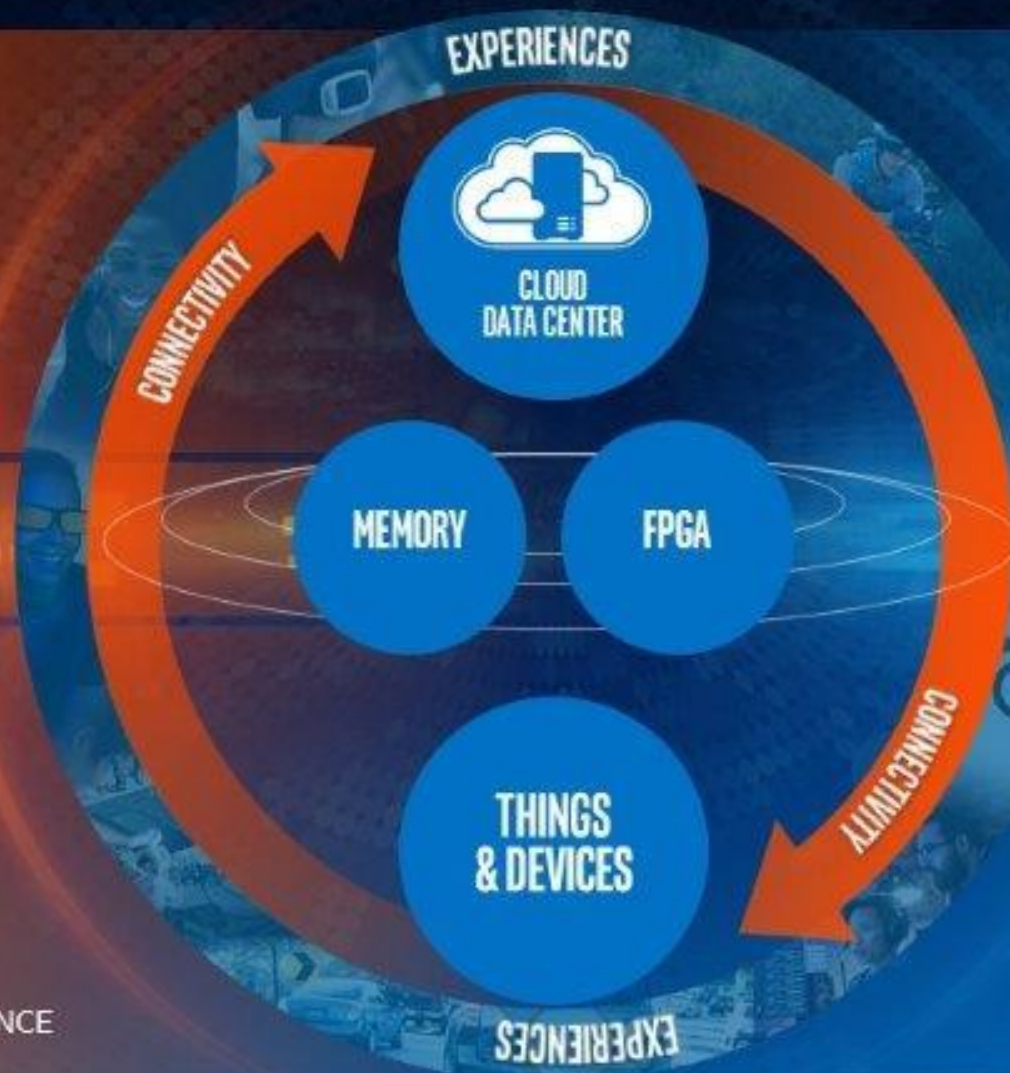
intel **REALSENSE**  
TECHNOLOGY  
DEPTH SENSING

**Movidius**  
COMPUTER VISION  
& DEEP LEARNING

COMPUTER VISION,  
TOOLS & STANDARDS

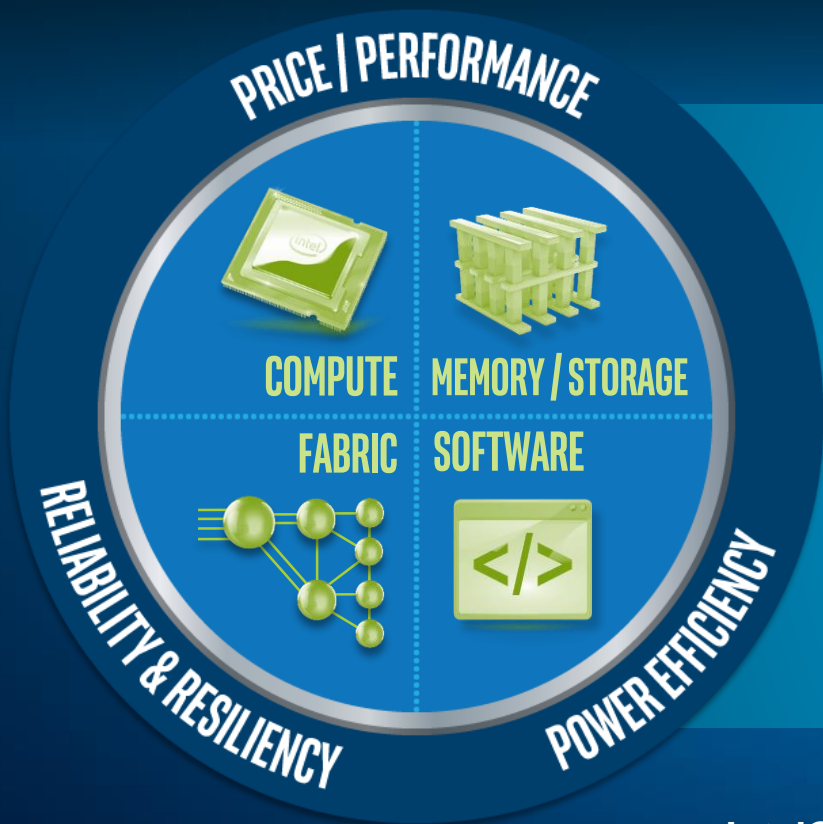
COLLISION AVOIDANCE  
& NAVIGATION

## EXPERIENCES



# Intel® Scalable System Framework

## A Holistic Solution for All HPC Needs



**Small Clusters Through Peta and Exascale**  
**Compute and Data-Centric Computing**  
**Standards-Based Programmability**  
**IA and HPC Ecosystem Enabling**  
**On-Premise and Cloud-Based**

Intel® Xeon® Processors  
Intel® Xeon Phi™ Processors  
Intel® FPGAs and Server Solutions

Intel® Solutions for Lustre\*  
Intel® Optane™ Technology  
3D XPoint™ Technology  
Intel® SSDs

Intel® Omni-Path Architecture  
Intel® Silicon Photonics  
Intel® Ethernet

Intel® HPC Orchestrator  
Intel® Software Tools  
Intel® Cluster Ready Program  
Intel Supported SDVis

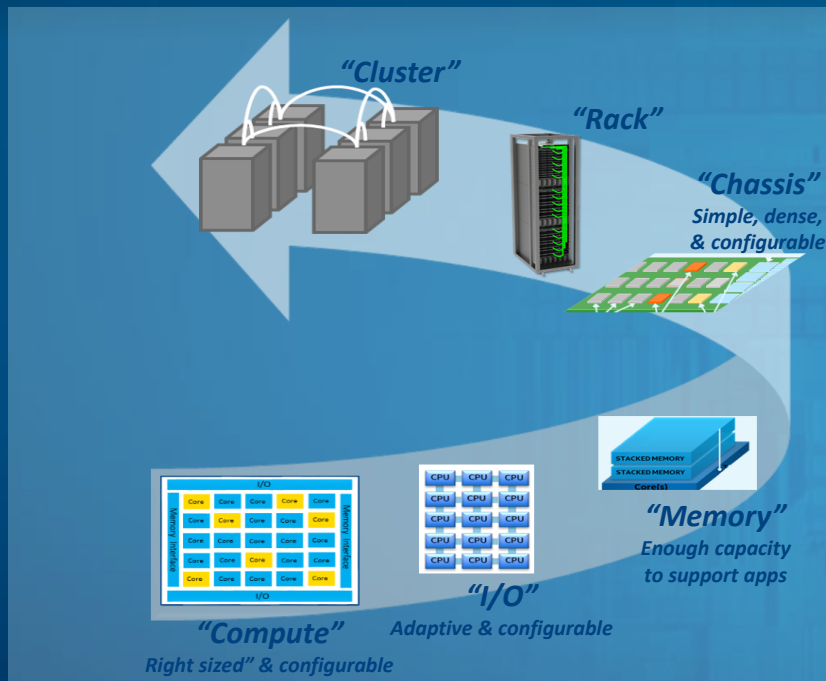




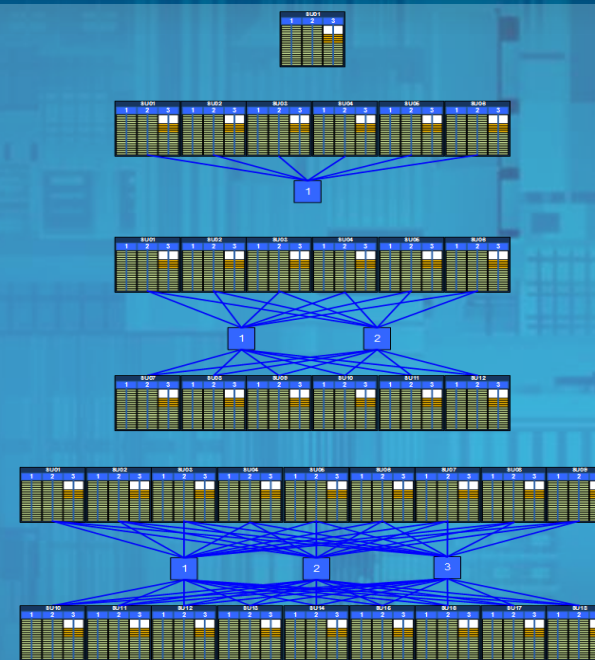
# SSF: Enabling Configurability & Scalability

from components to racks to clusters

## SSF Path To Exascale



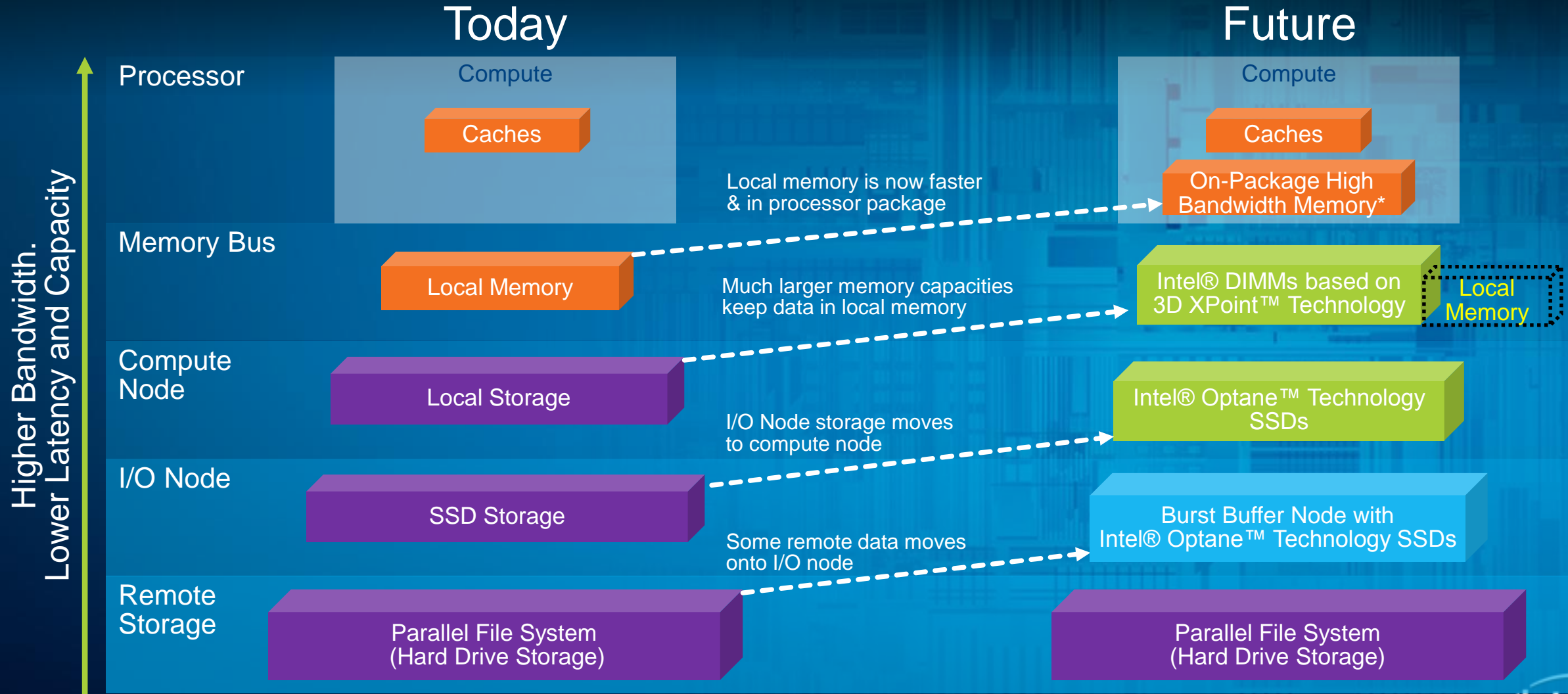
## SSF for Scalable Clusters



- Xeon or Xeon-Phi – based on workload needs
- Compute flexibly aggregated
- Lowest latency compute to compute interconnect
- I/O Topologies for best performance
- Configurable I/O bandwidth director switch
- Burst buffer to decouple storage from I/O

# Tighter **System-Level** Integration

## Innovative Memory-Storage Hierarchy



\*cache, memory or hybrid mode



# Bringing Memory Back Into Balance

## High Bandwidth, On-Package Memory

Up to 16GB with Knights Landing

**5x** the Bandwidth vs DDR4<sup>1</sup>, >400 GB/s<sup>1</sup>

**>5x** More Energy Efficient vs GDDR5<sup>2</sup>

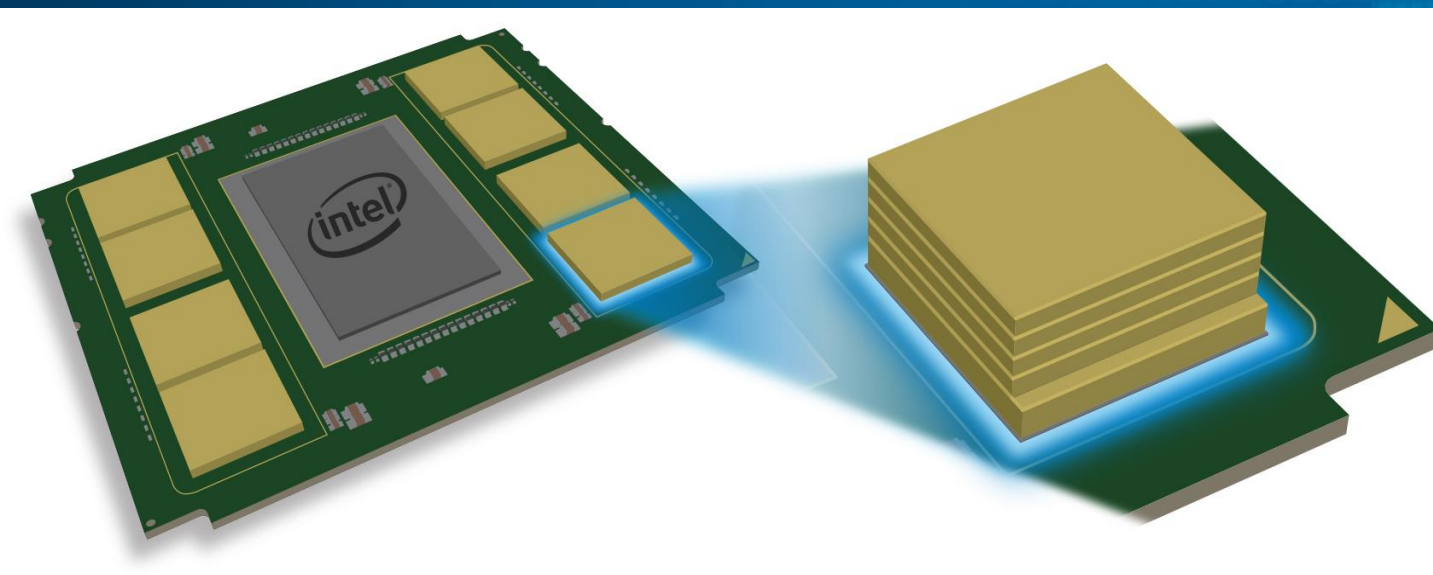
**>3x** More Dense vs GDDR5<sup>2</sup>

**3** Modes of Operation

**Flat Mode:** Acts as Memory

**Cache Mode:** Acts as Cache

**Hybrid Mode:** Mix of Cache and Flat

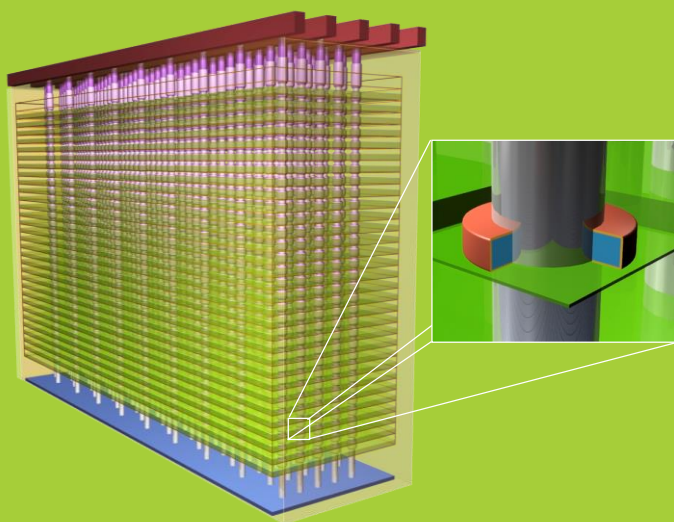


<sup>1</sup> Projected result based on internal Intel analysis of STREAM benchmark using a Knights Landing processor with 16GB of ultra high-bandwidth versus DDR4 memory with all channels populated.

<sup>2</sup> Projected result based on internal Intel analysis comparison of 16GB of ultra high-bandwidth memory to 16GB of GDDR5 memory used in the Intel® Xeon Phi™ coprocessor 7120P.

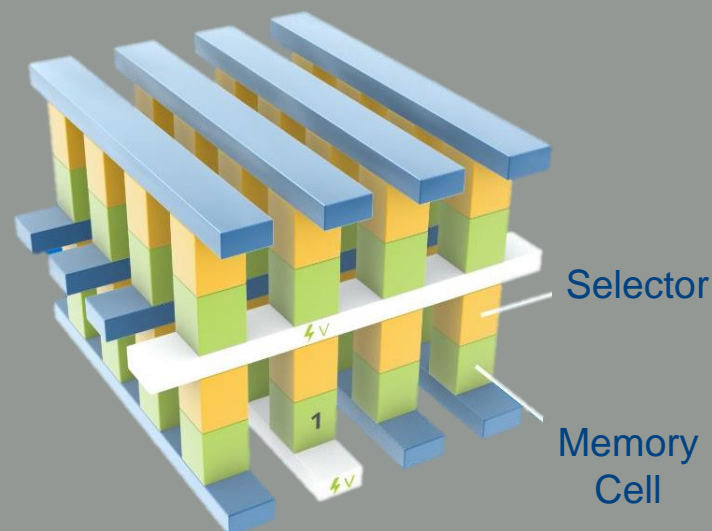
# NAND Flash and 3D XPoint™ Technology

## 3D MLC and TLC NAND



Enabling highest capacity SSDs  
at the lowest price

## 3D XPoint™ Technology



Enabling highest performance  
SSDs and expanding use cases



# 3D Xpoint™ Technology

## Cross Point Structure

Perpendicular wires connect submicroscopic columns. An individual memory cell can be addressed by selecting its top and bottom wire.

## Non-Volatile

3D XPoint™ Technology is non-volatile—which means your data doesn't go away when your power goes away—making it a great choice for storage.

## High Endurance

Unlike other storage memory technologies, 3D XPoint™ Technology is not significantly impacted by the number of write cycles it can endure, making it more durable.

## Transforming the Memory Hierarchy

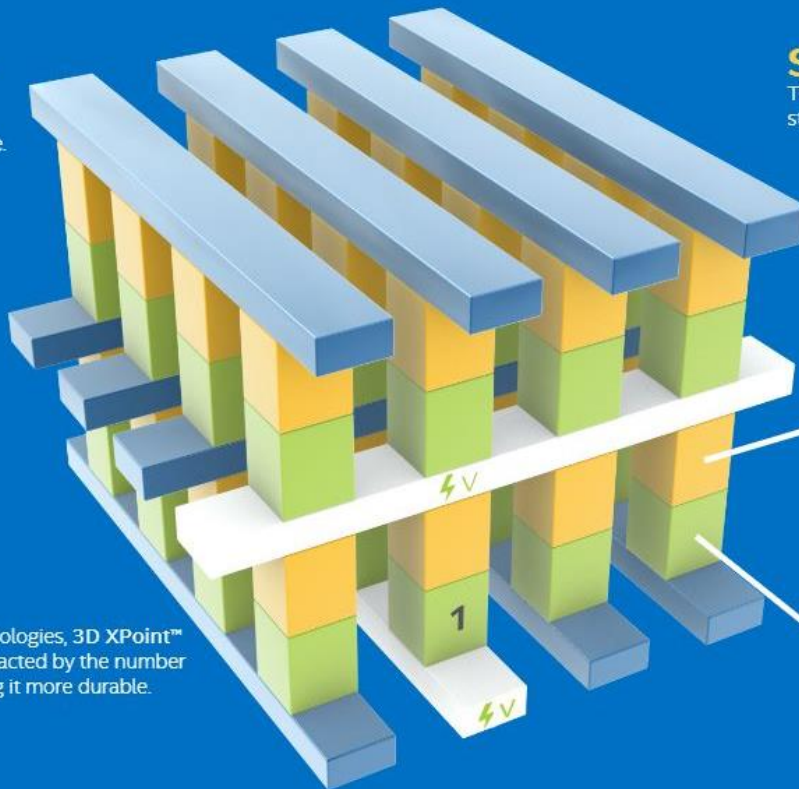
For the first time, there is a fast, inexpensive and non-volatile memory technology that can serve as system memory and storage.



3D XPoint™ Technology



Processor



## Stackable

These thin layers of memory can be stacked to further boost density.

## Selector

Whereas DRAM requires a transistor at each memory cell—making it big and expensive—the amount of voltage sent to each 3D XPoint™ Technology selector enables its memory cell to be written to or read without requiring a transistor.

## Memory Cell

Each memory cell can store a single bit of data.

## ~8x to 10x Greater Density than DRAM¹

3D XPoint™ Technology's simple, stackable, transistor-less design packs more memory into less space, which is critical to reducing cost.

1GB

DRAM



3D XPoint™ Technology

# CPU-Fabric Integration

## with the Intel® Omni-Path Architecture

### KEY VALUE VECTORS

- ✓ Performance
- ✓ Density
- ✓ Cost
- ✓ Power
- ✓ Reliability

PERFORMANCE

TIME

Intel® OPA HFI Card

Twinax Cable  
Twinax Cable

Connector

Intel®  
OPATighter  
IntegrationIntel®  
OPA

### Future Generations

Additional integration,  
improvements, and features

Next generation  
Intel® Xeon® Phi™ processor

Future Intel® Xeon® processor (14nm)

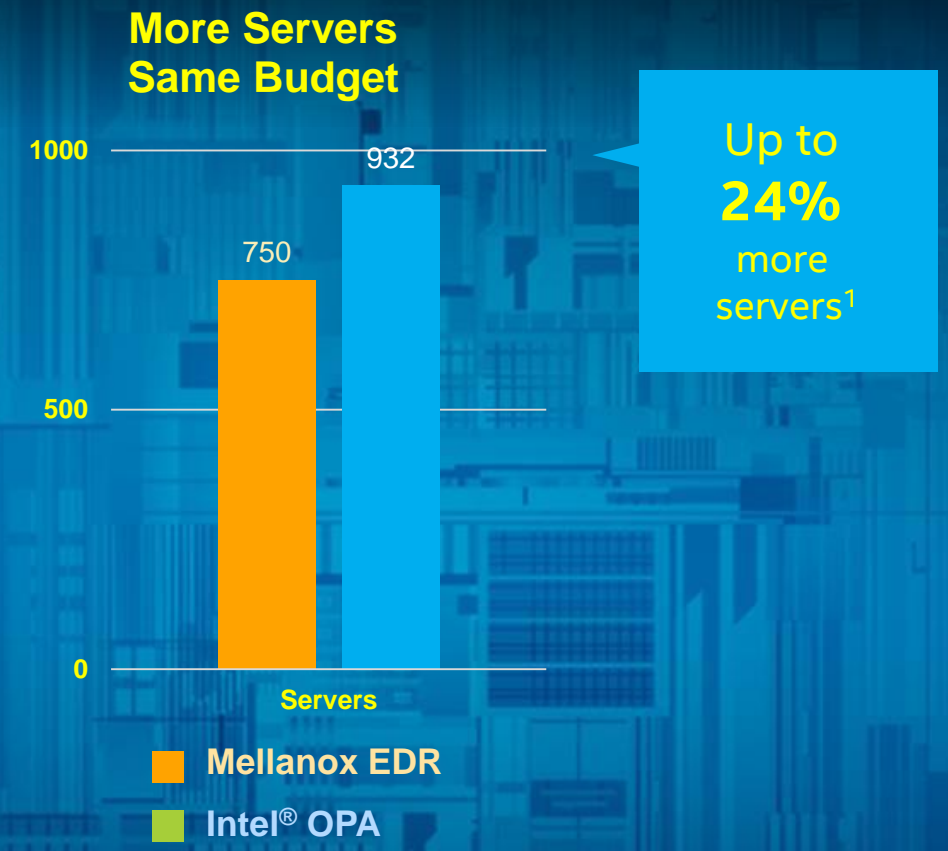
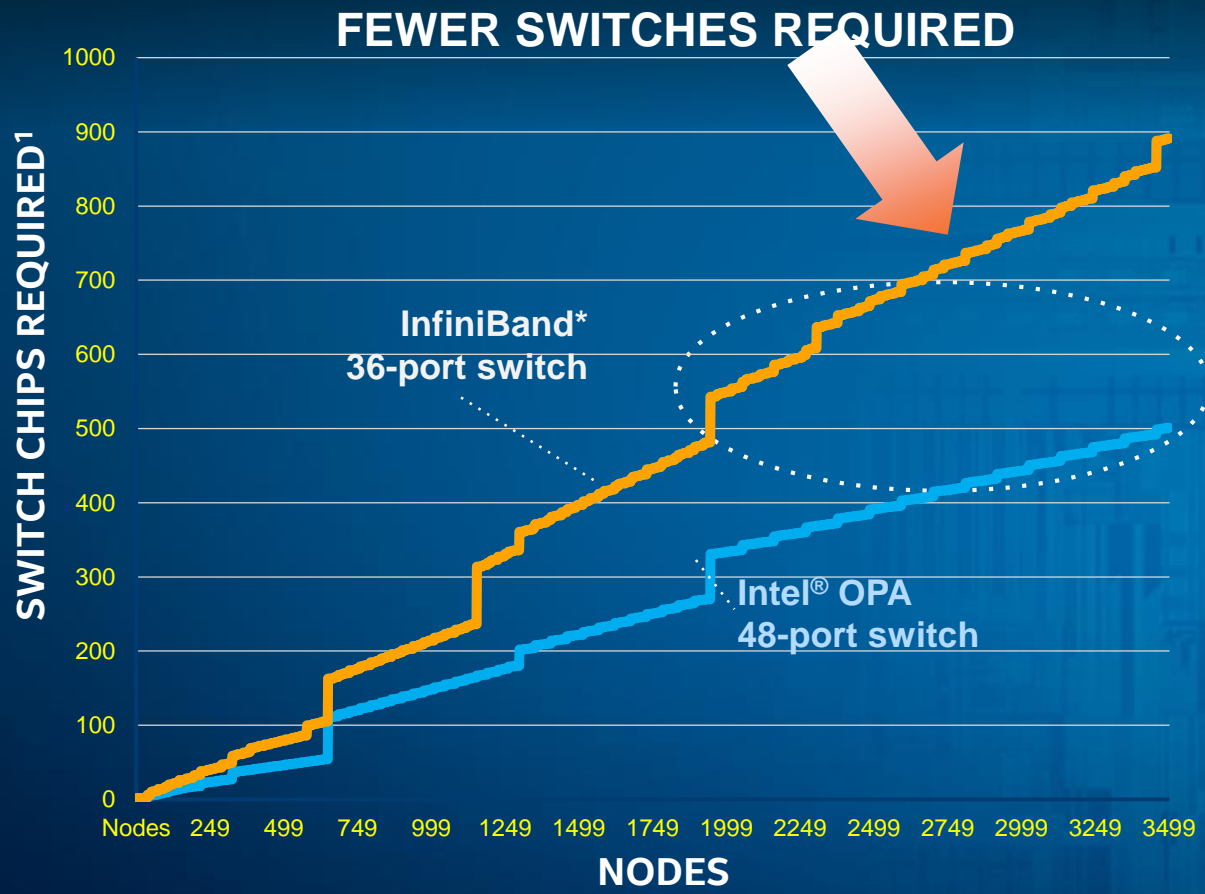
Intel® Xeon Phi™ 7220 (KNL) processor

Next generation Intel® Xeon® processor

Intel® Xeon® processor E5-2600 v3

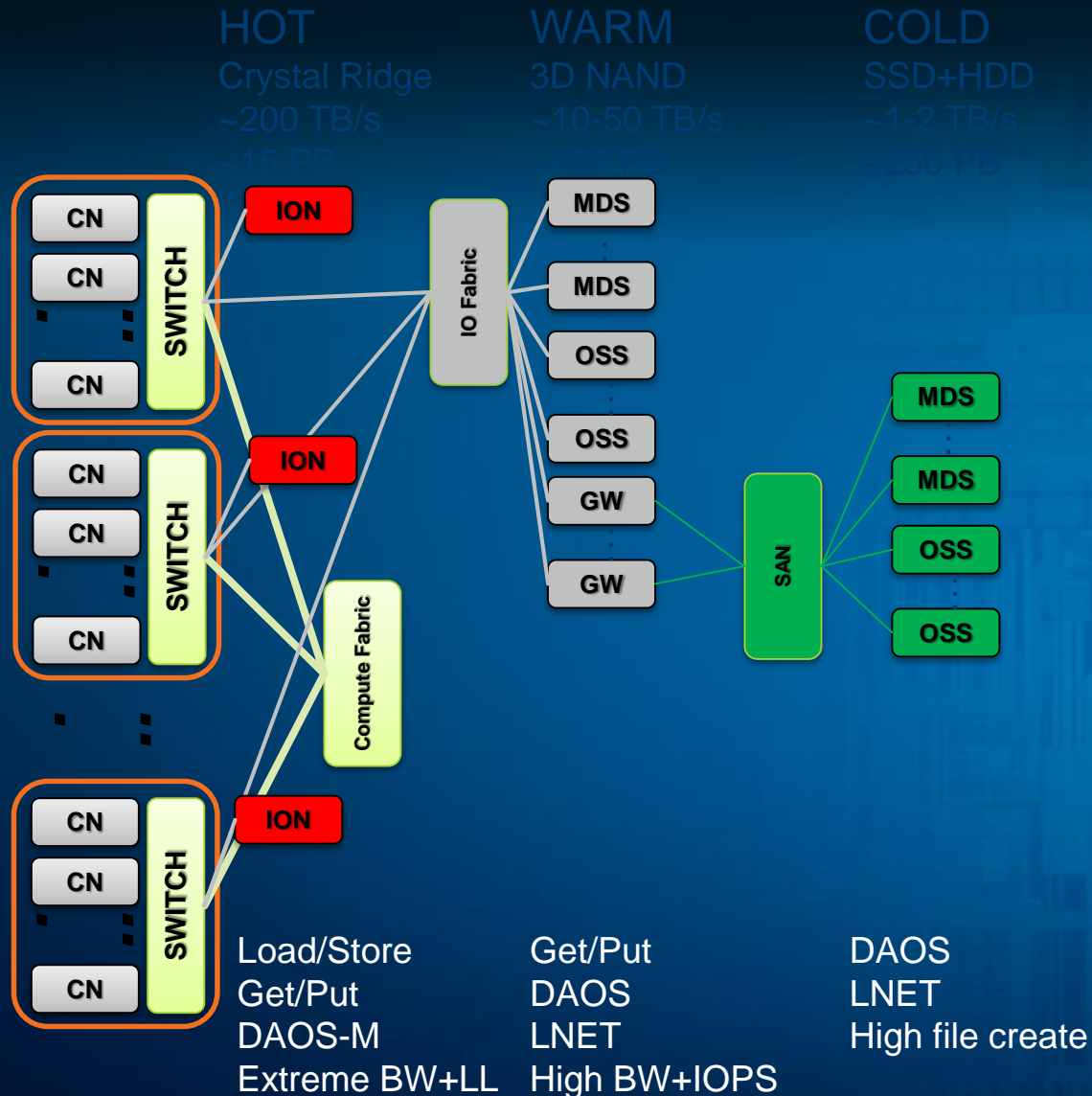


# OmniPath is Optimized for scalability



<sup>1</sup> Configuration assumes a 750-node cluster, and number of switch chips required is based on a full bisectional bandwidth (FBB) Fat-Tree configuration. Intel® OPA uses one fully-populated 768-port director switch, and Mellanox EDR solution uses a combination of 648-port director switches and 36-port edge switches. Intel and Mellanox component pricing from [www.kernelsoftware.com](http://www.kernelsoftware.com), with prices as of May 5, 2016. Compute node pricing based on Dell PowerEdge R730 server from [www.dell.com](http://www.dell.com), with prices as of November 3, 2015. Intel® OPA pricing based on estimated reseller pricing based on projected Intel MSRP pricing at time of launch. \* Other names and brands may be claimed as property of others.

# New storage paradigm for data intensive systems



## • SSF Enables HPC+HPDA workloads

- System components can be configured to match workload requirements
- Enables new access methodologies (DAOS) to create new generation applications
- Incremental improvements to Lustre to provide enhanced performance for existing applications

## Distributed Asynchronous Object Storage





# Benefit from Intel's long-standing investments

A photograph of a green computer motherboard with various components like RAM, CPU, and connectors.

Systems  
Architecture

A close-up photograph of a white, lattice-like microchip or semiconductor component.

Manufacturing  
Leadership

A photograph of a yellow energy meter with multiple dials and a digital display showing '000000'.Energy  
Efficient  
PerformanceA photograph of a heavy, grey metal vault door with a circular handle and a small clock-like dial.

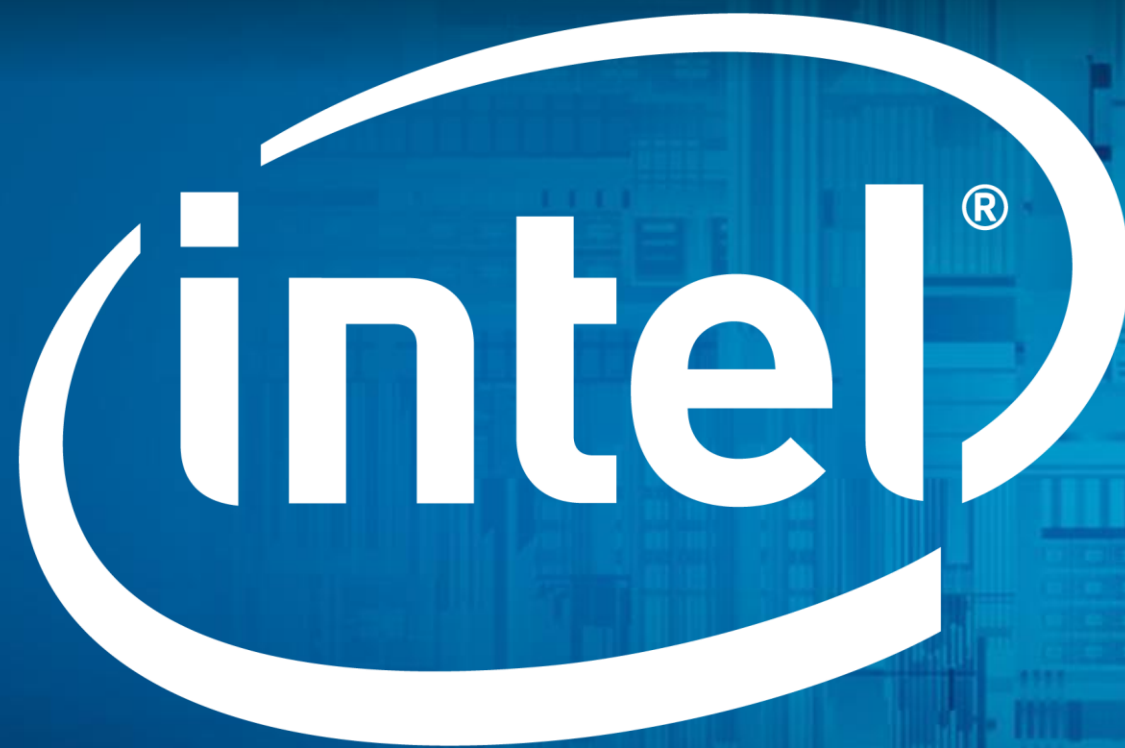
Security

A photograph of a blue, glowing digital display showing binary code (0s and 1s) in a grid pattern.

Software

A photograph showing silhouettes of several people standing in front of a glowing blue globe with a grid overlay.

Global  
Ecosystem





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