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2D and 3D CMOS MAPS with high performance pixel-level signal processing

This work is concerned with the design of analog circuits for processing the signals from deep N-well (DNW) monolithic CMOS sensors.
As compared to conventional MAPS with 3-transistor readout scheme, the design approach proposed here lends itself to pixel-level sparsified processing and is expected to provide the ability to manage the large data flow anticipated for future, high luminosity colliders. This paper will discuss the design features and measurement results of the Apsel5T chip
recently fabricated in a planar 130nm CMOS technology. Also results from physical device simulations, aiming at evaluating the properties of the DNW sensor in terms of charge collection efficiency and cluster size, will be presented, together with the features of a new DNW sensor designed in a CMOS two-layer vertically integrated technology.

Summary (Additional text describing your work. Can be pasted here or give an URL to a PDF document):

Monolithic active pixel sensors (MAPS) properties have been intensely investigated by several research teams involved in the development of detectors for particle physics experiments. Their monolithic structure, featuring a few micron thick superficial active volume, makes them the optimal choice for applications to experiments at the future high luminosity colliders.
Deep N-well (DNW) CMOS MAPS were proposed a few years ago to enable the design of large, highly granular matrices of thin charged particle detectors with fast readout architecture based on sparsification techniques. This devices integrate, in the same substrate, a relatively (as compared to standard 3T MAPS) large collecting electrode featuring a buried n-type layer and a fully CMOS processing chain including a low noise charge preamplifier, a threshold discriminator followed by a digital section for binary information storage and time stamping.
Based on this approach, the first ever DNW MAPS detectors with pixel-level data sparsification have been designed, produced and tested at the Proton Synchrotron facility at CERN.
In the framework of the SLIM5 collaboration, the Apsel series chips were designed and fabricated in a 130nm CMOS technology, aiming at the development of thin tracking systems for high energy physics. The last prototype, Apsel5T, with improved charge detection efficiency, has been fabricated and the characterization activity is in progress.
Recently, new DNW MAPS have been designed in a vertically integrated CMOS technology. Vertical integration (also known as 3D) processes, by stacking two or more standard CMOS layers one on top of the other, could provide increased functional density, physical separation of the analog blocks from the digital blocks and reduction of the area covered by competitive n-wells in the sensor layer. A 3D version of the Apsel5T (Apsel5T3D) chip has been designed in a 130nm CMOS, two-layer, vertically integrated technology.
An infrared laser source was used for the experimental characterization of the device properties in terms of charge diffusion in the substrate, charge collection and charge sharing among the pixels. New laser tests are in progress on the test matrices in order to evaluate the gain uniformity and provide a comparison between the measured charge collection efficiency and device simulation results. The device simulations have been performed with Monte Carlo techniques specifically developed to simulate random walk of minority carriers in an undepleted detector substrate.
The features of the 3D monolithic detector Apsel5T3D, including the analog front-end electronics, will be discussed, together with the results of the laser characterization of the sensor fabricated in the planar 130nm CMOS technology.

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