



The Belle-II Pixel Vertex Tracker at the SuperKEKB Flavour Factory

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On behalf of the DEPFET Collaboration



Universität Karlsruhe (TH)
Research University • founded 1825



The Henryk Niewodniczański
Institute of Nuclear Physics
Polish Academy of Sciences



MAX-PLANCK-GESELLSCHAFT



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TECHNISCHE
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universität**bonn**



- DEPFET Collaboration



❖ DEPFET is not only a technology but also a Collaboration

- **University of Barcelona**

- **Ramon Llull University**

- **Bonn University**

- **Heidelberg University**

- **Goettingen University**

- **Karlsruhe University**

- **IFJ PAN, Krakow**

- **MPI Munich**

- **Charles University, Prague**

- **TU Munich**

- **IFIC, CSIC-UVEG, Valencia**

- **University of Giessen**

- **LMU Munich**

www.depfet.org

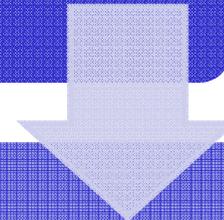


- Outline



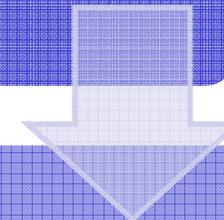
DEPFET

- Basics
- System elements



Belle-II PXD

- Detector overview
- Ladder design



Mechanical and Thermal issues

- Simulation results
- Mechanical/thermal support
- Cooling baseline

Biased...



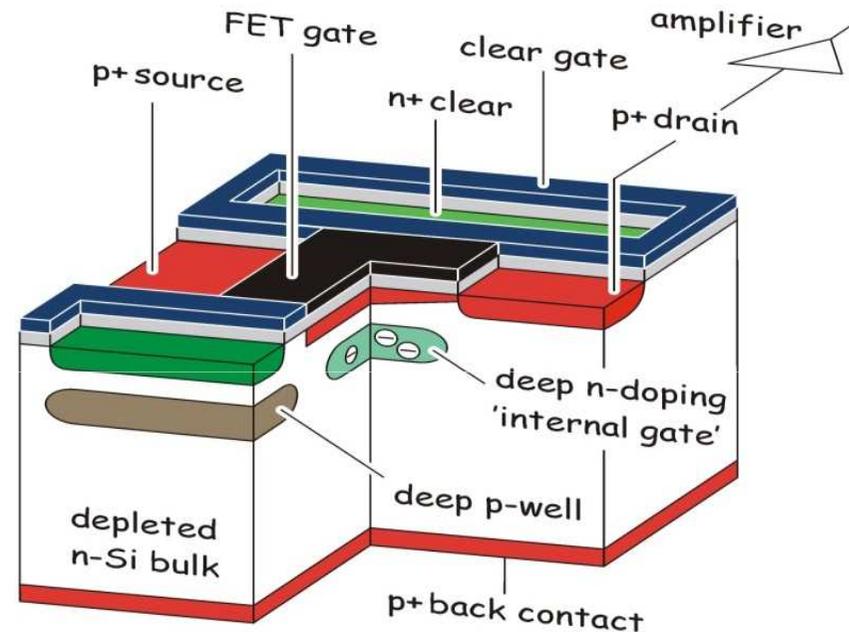
- DEPFET – DEpleted P-channel Field Effect Transistor



- Each pixel is a p-channel FET on a completely depleted bulk (sideward depletion). Charge is collected by drift
- A deep n-implant creates a potential minimum for electrons under the gate (internal gate)

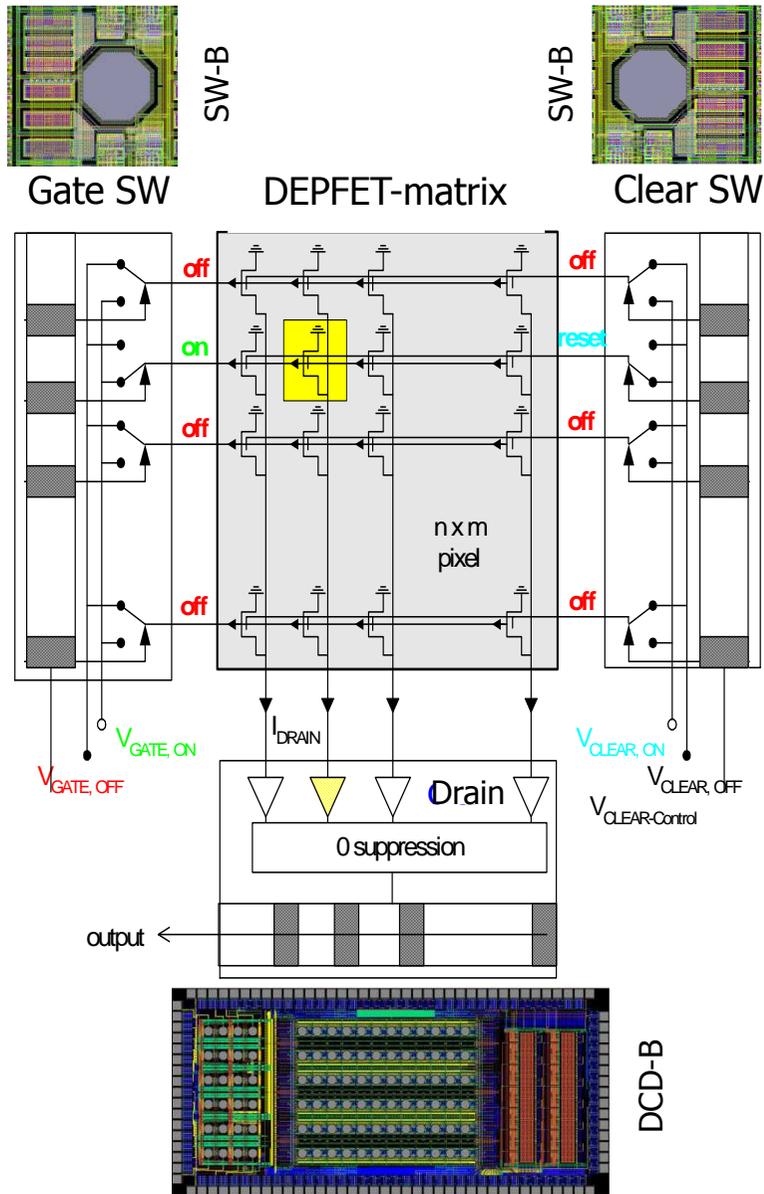
- Signal electrons accumulate in the internal gate and modulate the transistor current ($g_q \approx 600 \text{ pA/e}^-$)
- Accumulated charge can be removed by a clear contact

- Internal amplification
- Low power consumption: Readout on demand (Sensitive all the time, even in OFF state)



- Small pixel size
- Intrinsic Noise $\approx 40e^-$ at high bandwidth \rightarrow Small capacitance and first in-pixel amplification
- Thin Detectors $\approx 50 \mu\text{m}$

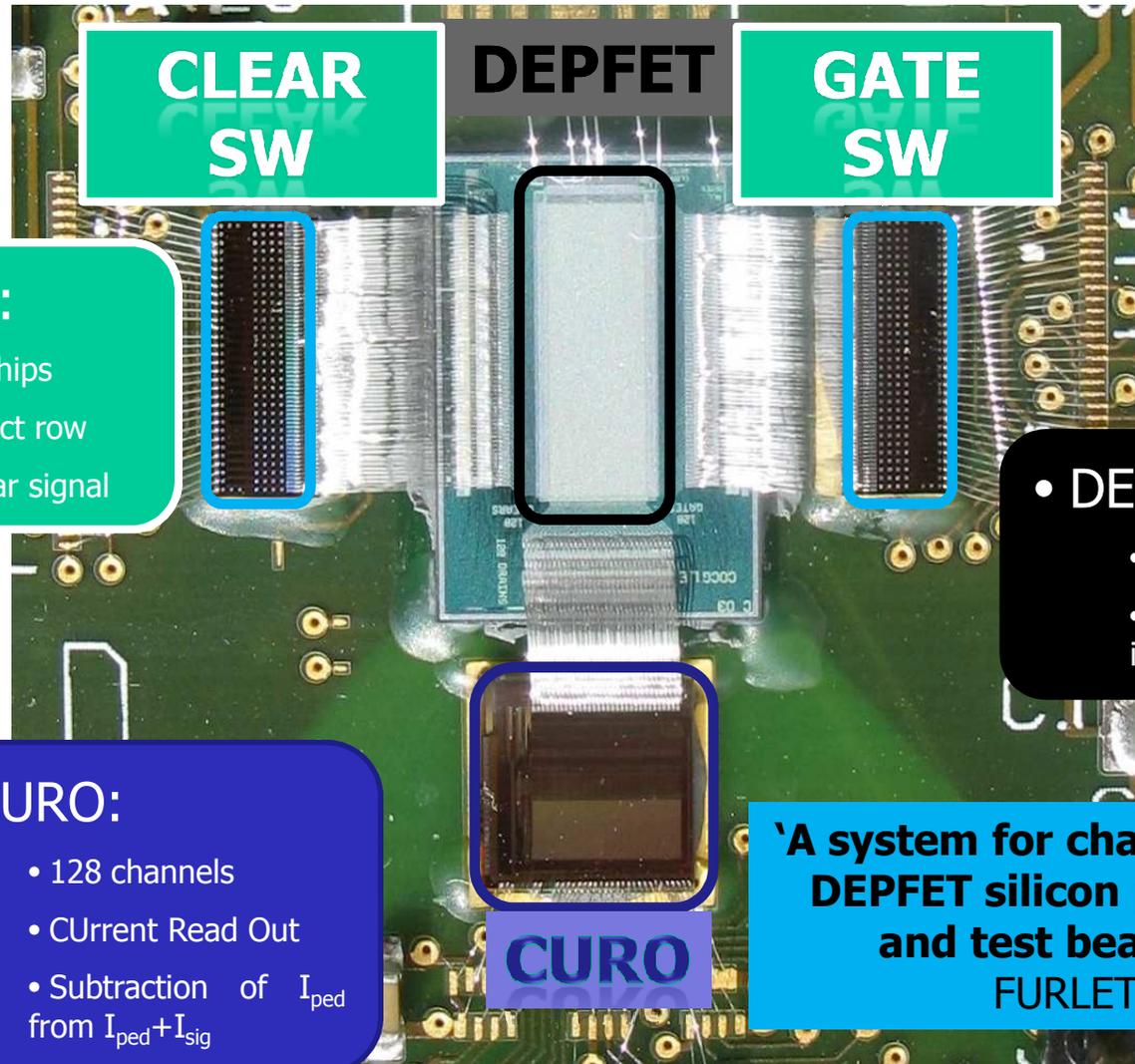
● Operation mode: Row wise readout



Row wise r/o (Rolling Shutter)

- Select row with external gate, read current, clear DEPFET, read current again → The difference is the signal
- Low power consumption: Only one row active at a time; Readout on demand (Sensitive all the time, even in OFF state)
- Two different auxiliary chips needed (Switchers)
- Limited frame rate

- Prototype system: Hybrid board



- Switchers:
 - Steering chips
 - Gate: Select row
 - Clear: Clear signal

- DEPFET Matrix
 - 64x256 pixels
 - Several pixel sizes, implants, geometries

- CURO:
 - 128 channels
 - CUrrent Read Out
 - Subtraction of I_{ped} from $I_{ped} + I_{sig}$

**'A system for characterisation of DEPFET silicon pixel matrices and test beam results'.
FURLETOV, S.**

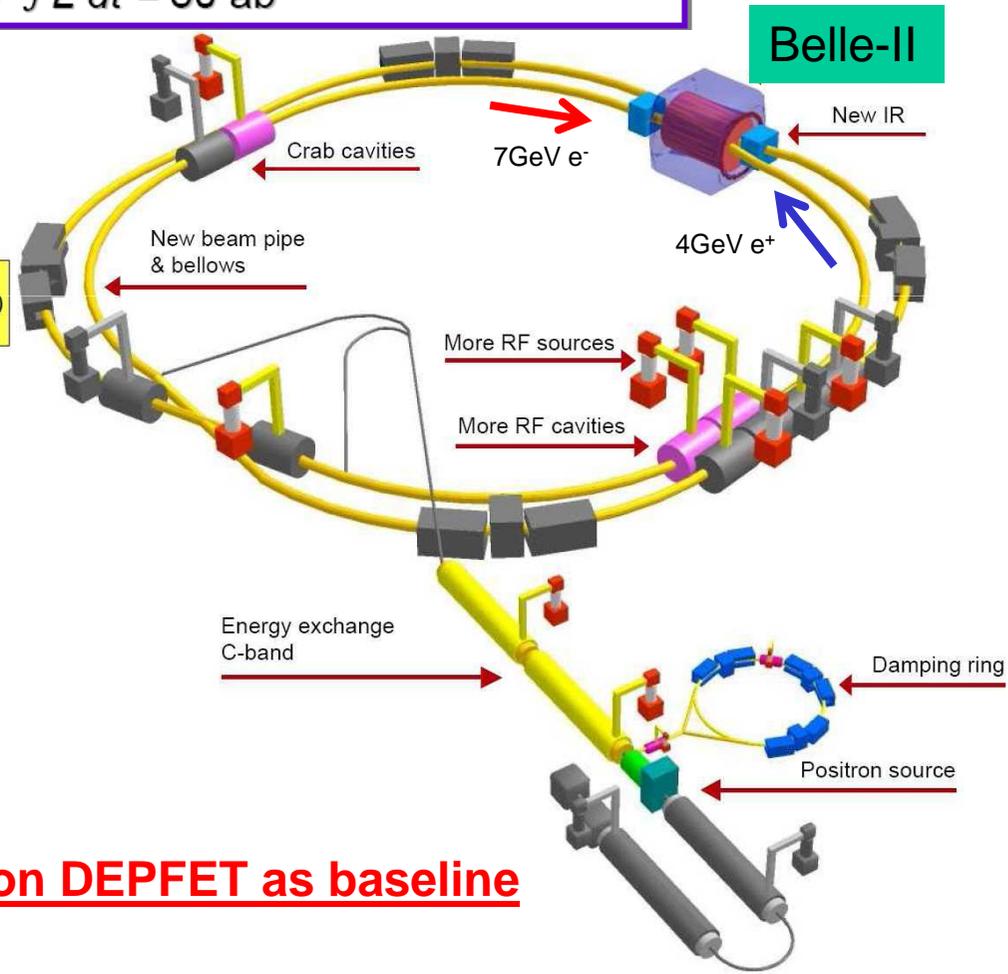
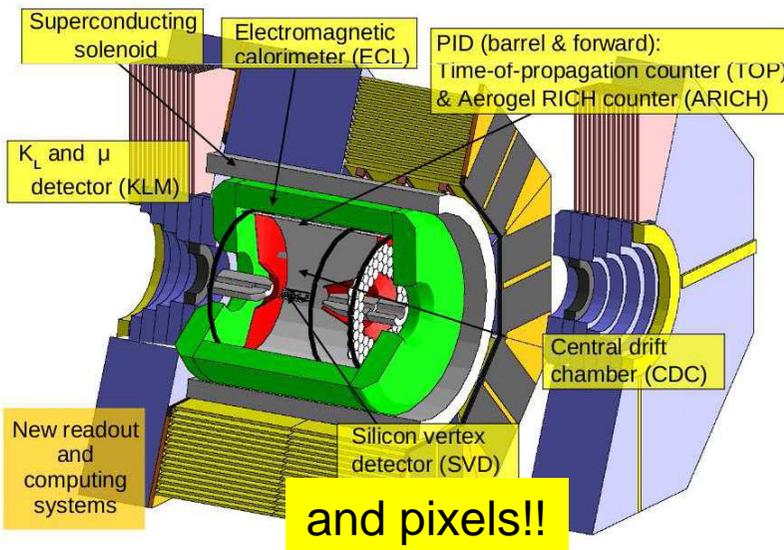
The latest DEPFET Generation 'PXD5' → Test Beam 2009 at CERN

KEKB Upgrade Plan : Super-B Factory at KEK



- Asymmetric energy e^+e^- collider at $E_{CM}=m(\Upsilon(4S))$ to be realized by upgrading the existing KEBK collider.
- Initial target:** $10 \times$ higher luminosity $\cong 2 \times 10^{35}/\text{cm}^2/\text{sec}$
 $\rightarrow 2 \times 10^9$ BB and $\tau^+\tau^-$ per yr.
- Final goal:** $L=8 \times 10^{35}/\text{cm}^2/\text{sec}$ and $\int L dt = 50 \text{ ab}^{-1}$

Luminosity 50 times larger than Belle
 Current 2 times larger

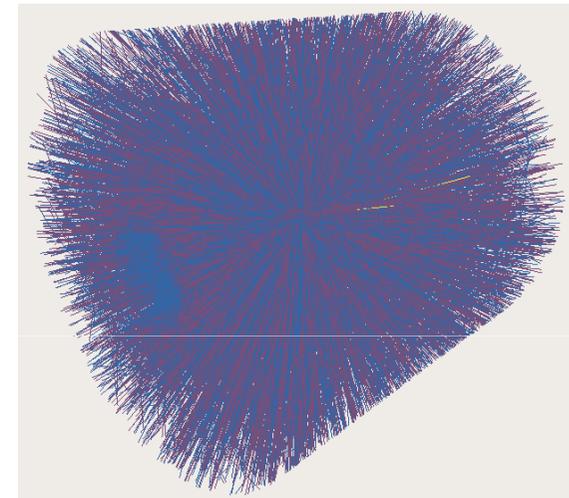


Belle-II PXD group has decided on DEPFET as baseline

- Belle-II



	Belle-II
Occupancy	0.4 hits/ $\mu\text{m}^2/\text{s}$ **
Radiation	> 1Mrad/year
Frame time	20 μs (continuous r.o. mode)
Momentum range	Low momentum (< 1 GeV)
Acceptance	17 $^\circ$ -155 $^\circ$



- Belle II

- Required spatial resolution ($\sim 10\mu\text{m}$) \rightarrow Moderate pixel size ($50 \times 50 \mu\text{m}^2$)
- Few 100 MeV momenta \rightarrow Lowest possible material budget (0.15% X_0/layer)

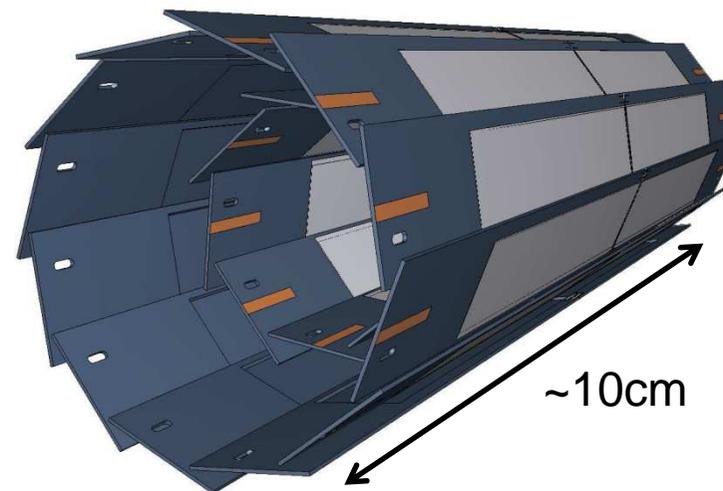
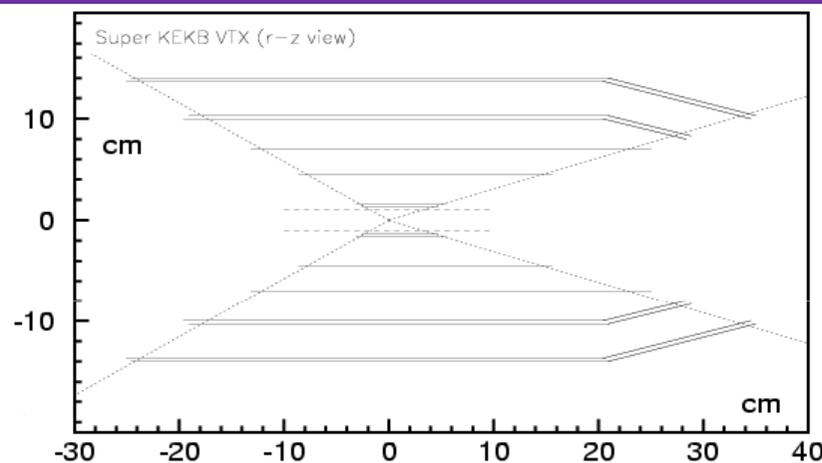
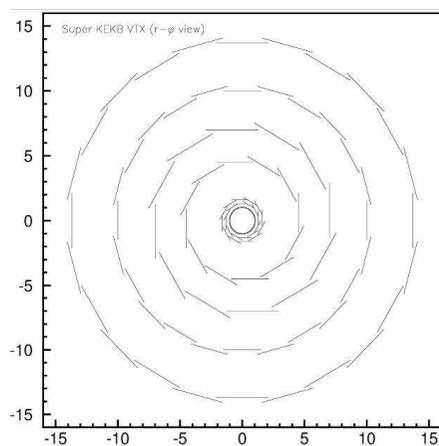
\rightarrow The DEPFET technology can cope with this challenging requirements

** Occupancy for the obsolete High-current option. Chosen Nano-beam is under study!

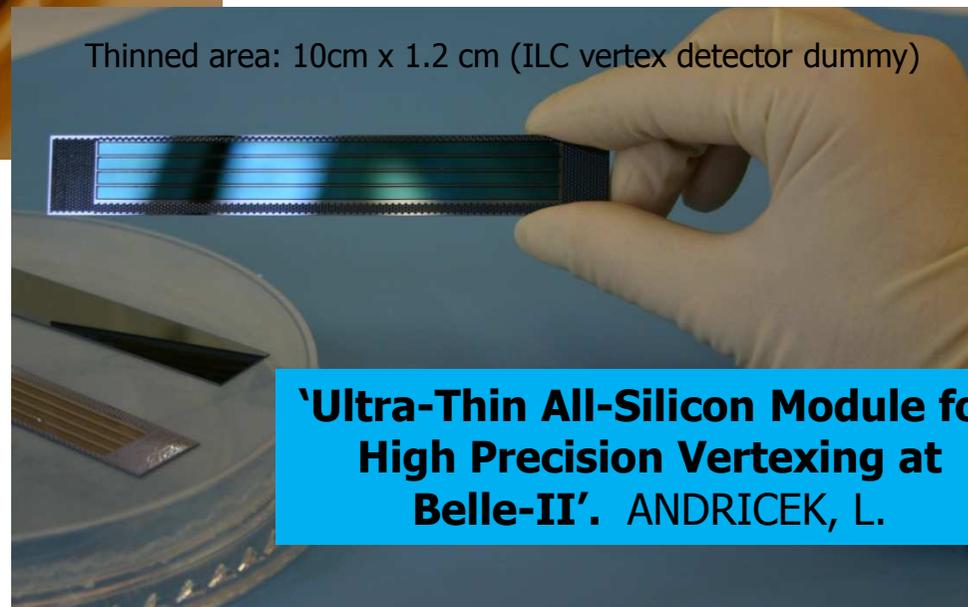
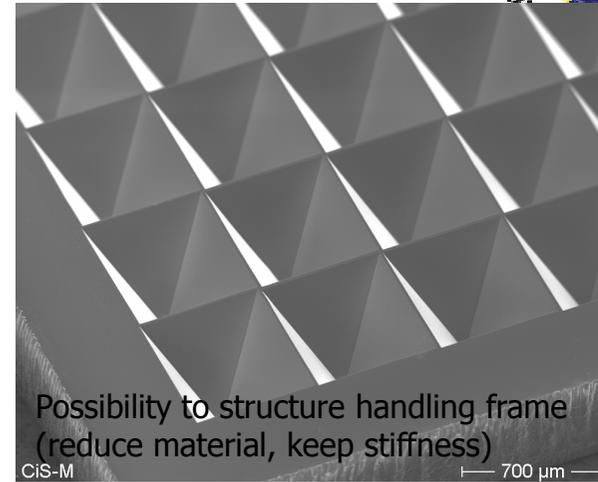
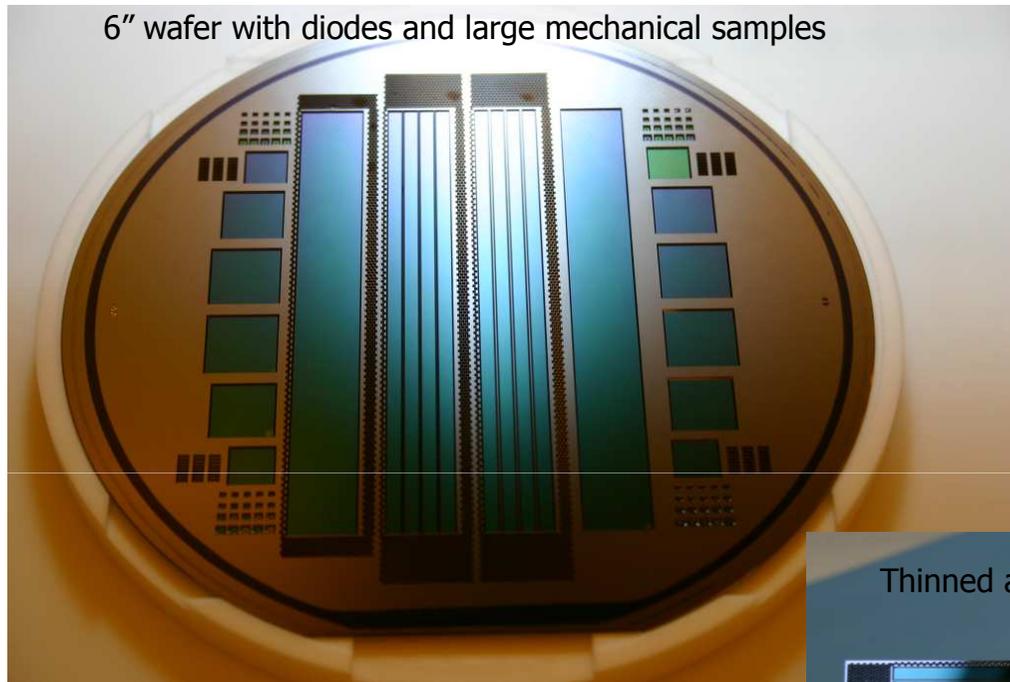
Belle-II PXD and DEPFET



- 2 thin pixel layers at 1.4 cm and 2.2 cm (subject to optimization)
- 4 layers with double sided Si-strip detectors
- Angular coverage $17^\circ < \theta < 155^\circ$, slanted at the end



- Elegant thinning technology: mechanical samples



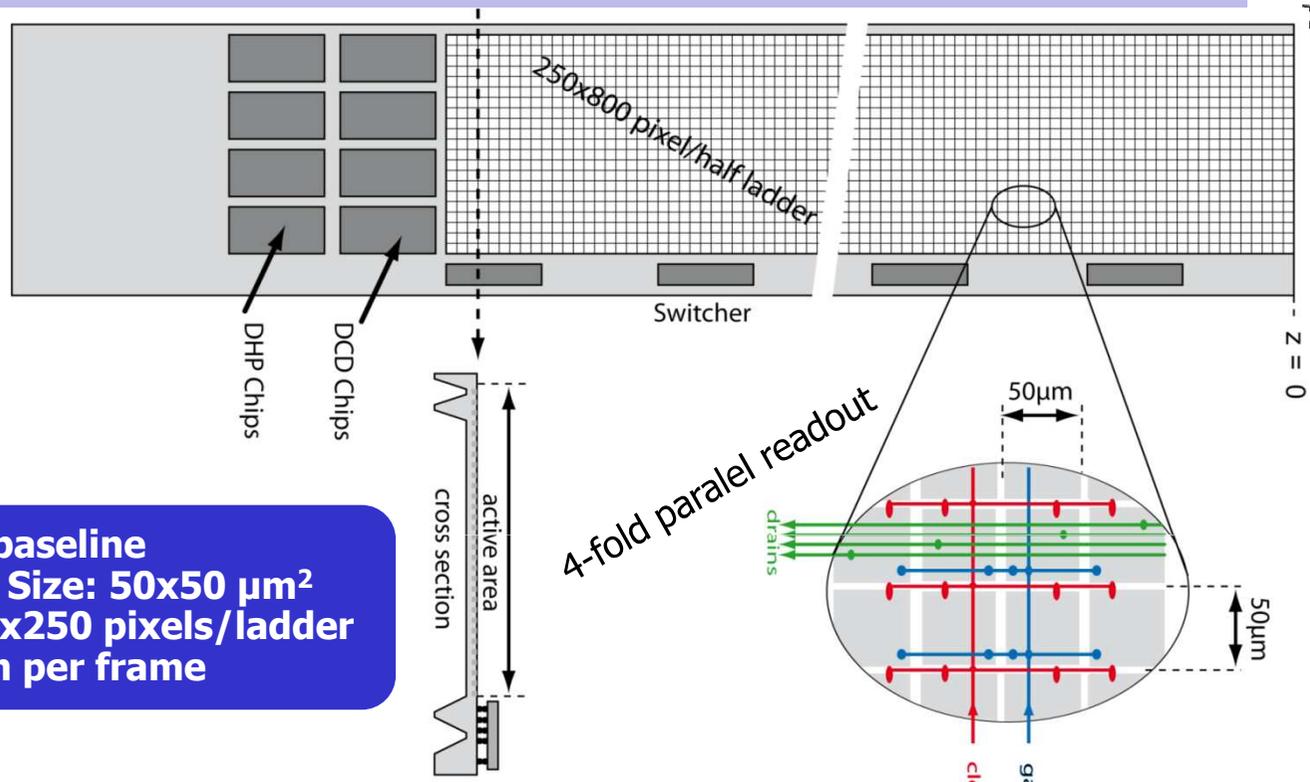
The material budget... a crucial issue!

→ Try to reduce the m.s. contribution

- **Sensor: Thinned down to 50μm**
- **Balconies: Etched grooves**

'Ultra-Thin All-Silicon Module for High Precision Vertexing at Belle-II'. ANDRICEK, L.

- The Belle-II half ladder

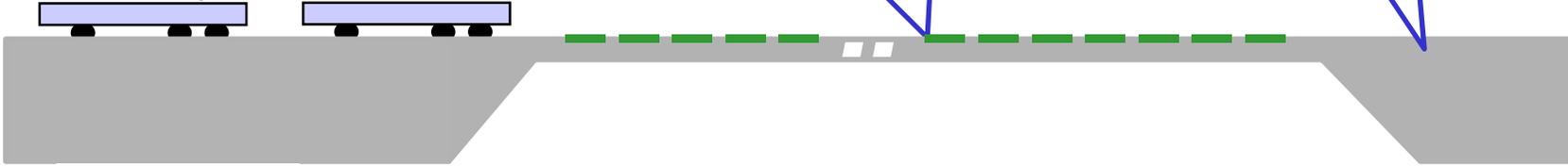


- Belle-II baseline**
Pixel Size: 50x50 µm²
1600x250 pixels/ladder
20µm per frame

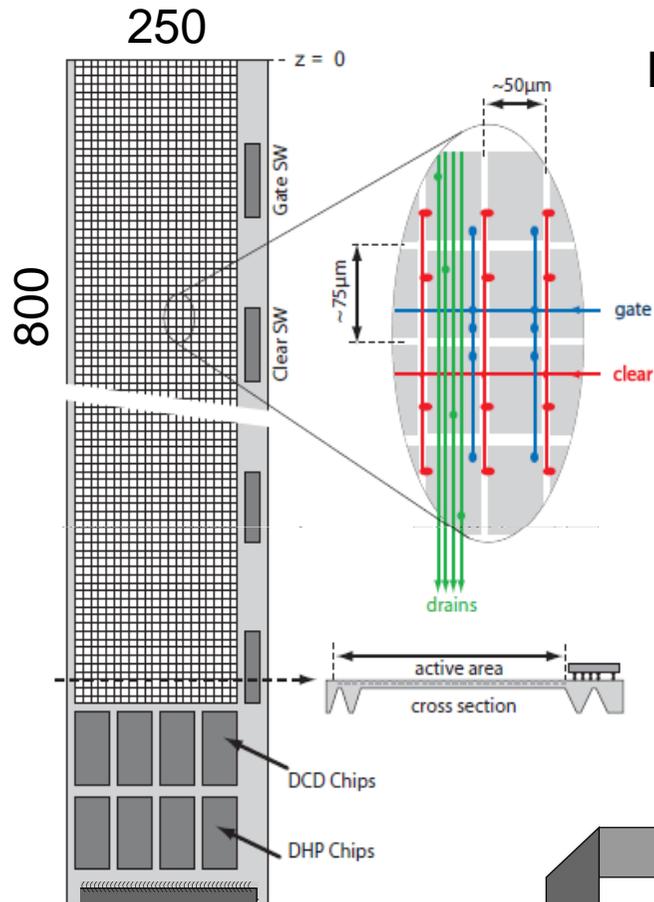
Chips connection via bump bonding

Thinned sensor (50 µm) in active area

Support frame



● Data flow

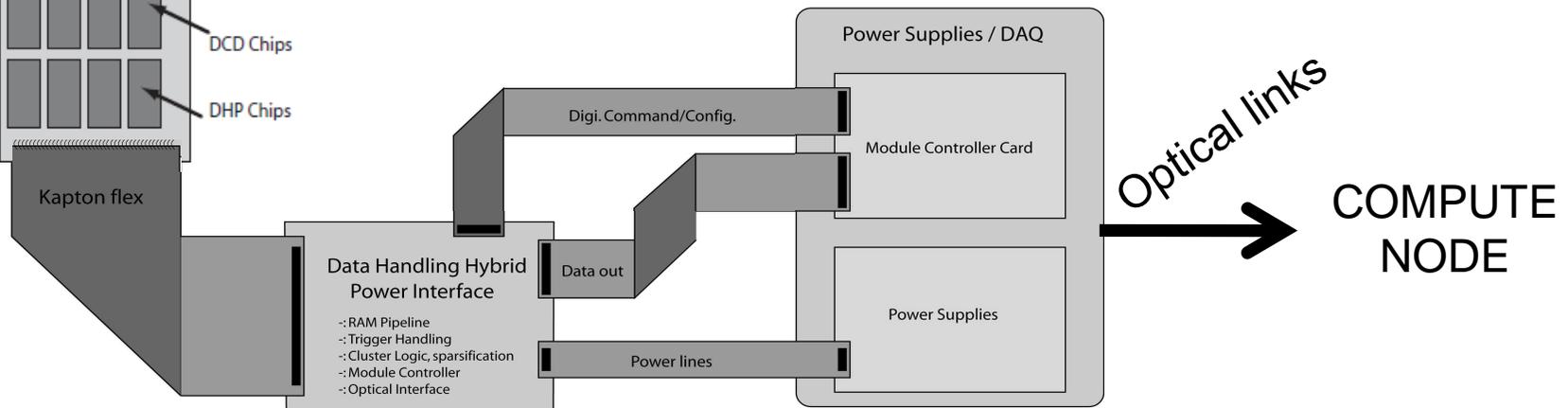


Half ladder (readout channel)

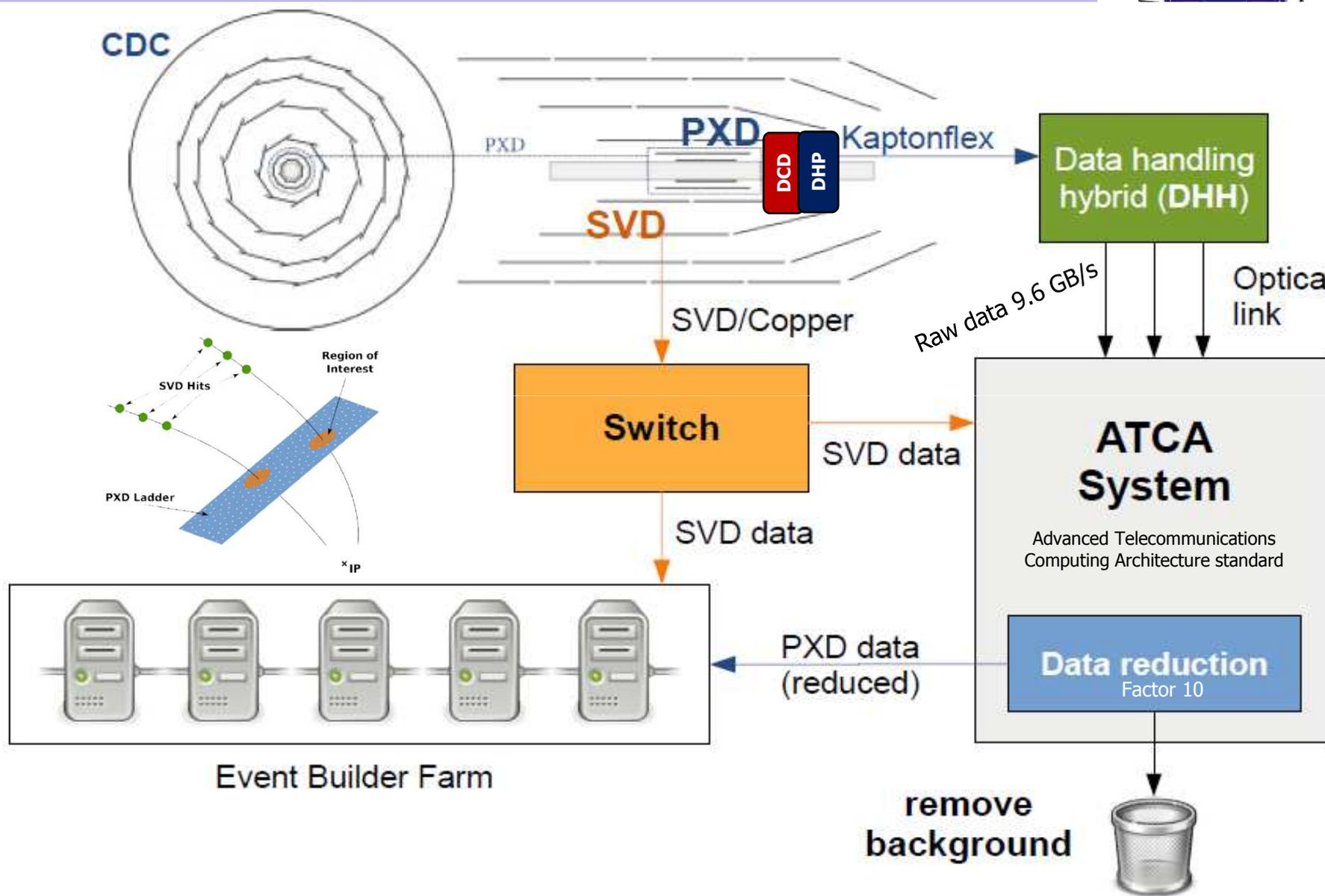
Number of pixels per ladder:

$$250 \times 800 \times 2 = 4 \cdot 10^5 \text{ px/ladder}$$

- 20 ladders
- 0.4 Mill. Pixel per ladder
- 8 Million pixels (px) total
- assumed occupancy 1%
 $8 \cdot 10^4$ pixels fired/each frame
- if trigger rate 30 kHz
- 2.4×10^9 px/s
- 4 bytes per px (pos + ADC)
- **9.6 GB/s total**
- 40 optical links
- 240 MB/s per 1 optical link
- 1.92 Gb/s per 1 optical link



● Data path



● Optimization: Full simulation chain

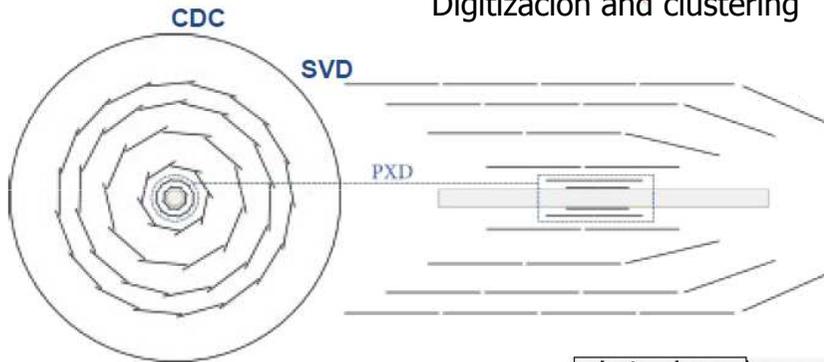


Particle gun (single event)
EvtGen (physics event)
Mokka geometry

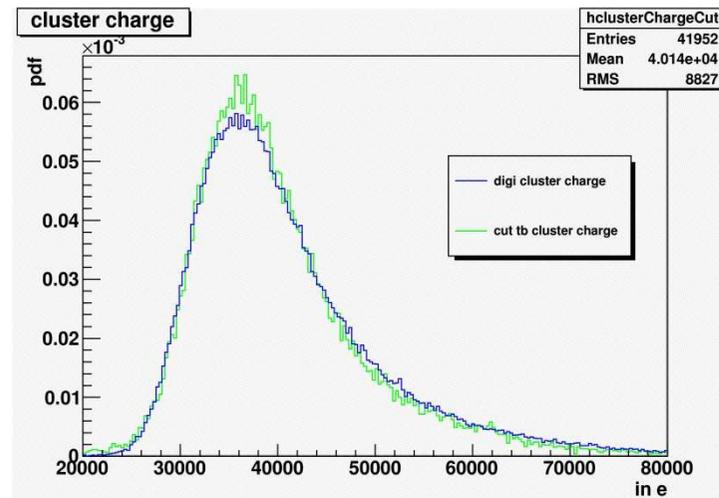
Ionization points
Signal points
Electronic noise
Digitization and clustering

Marlin tracking
PXD+SVD+CDC

Physics channels



- Digitizer (Geant4) tuned with TestBeam data:
 - Electric noise
 - Electric field in Si (charge collection time)
 - Lorentz angle in magnetic fields



● Detector optimization

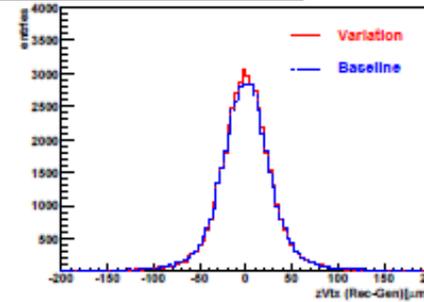


J/Psi z-Vertex resolution

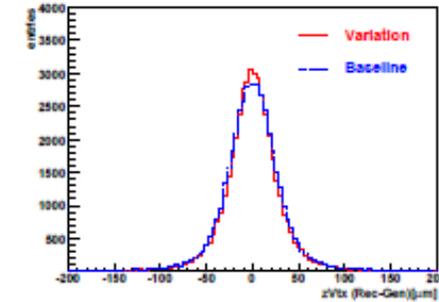
Optimization studies:

- Sensor thickness
- Pixel size
- Inner layer radius

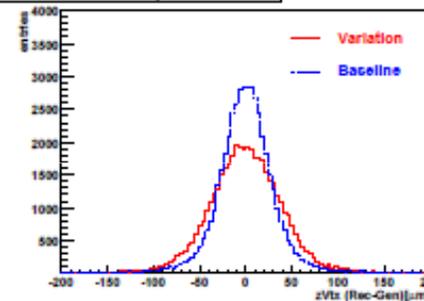
Radius of inner layer: $r_i = 13\text{mm}$ (vs. 14mm)



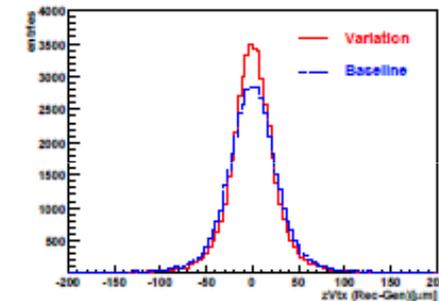
Sensor thickness: $d = 75\mu\text{m}$ (vs. $60\mu\text{m}$)



Number of pixel rows: $N_r = 800$ (vs. 1600)



Optimistic Design vs. Baseline Design



$d, \#px_{in}, \#px_{out}, r_{in}$	0.5 GeV [μm]	1 GeV [μm]
50 μm , 800x800, 14	53.43	36.04
50 μm , 800x1600, 14	50.28	31.90
50 μm , 1600x1600, 14, Split	42.41	23.93
50 μm , 1600x1600, 14	41.26	23.59
75 μm , 1600x1600, 14	40.71	22.97
50 μm , 1600x1600, 13	40.92	23.59
50 μm , 2000x2000, 13	38.96	21.57

← Base line

Impact parameter resolution z_0

Angle: 55 degree

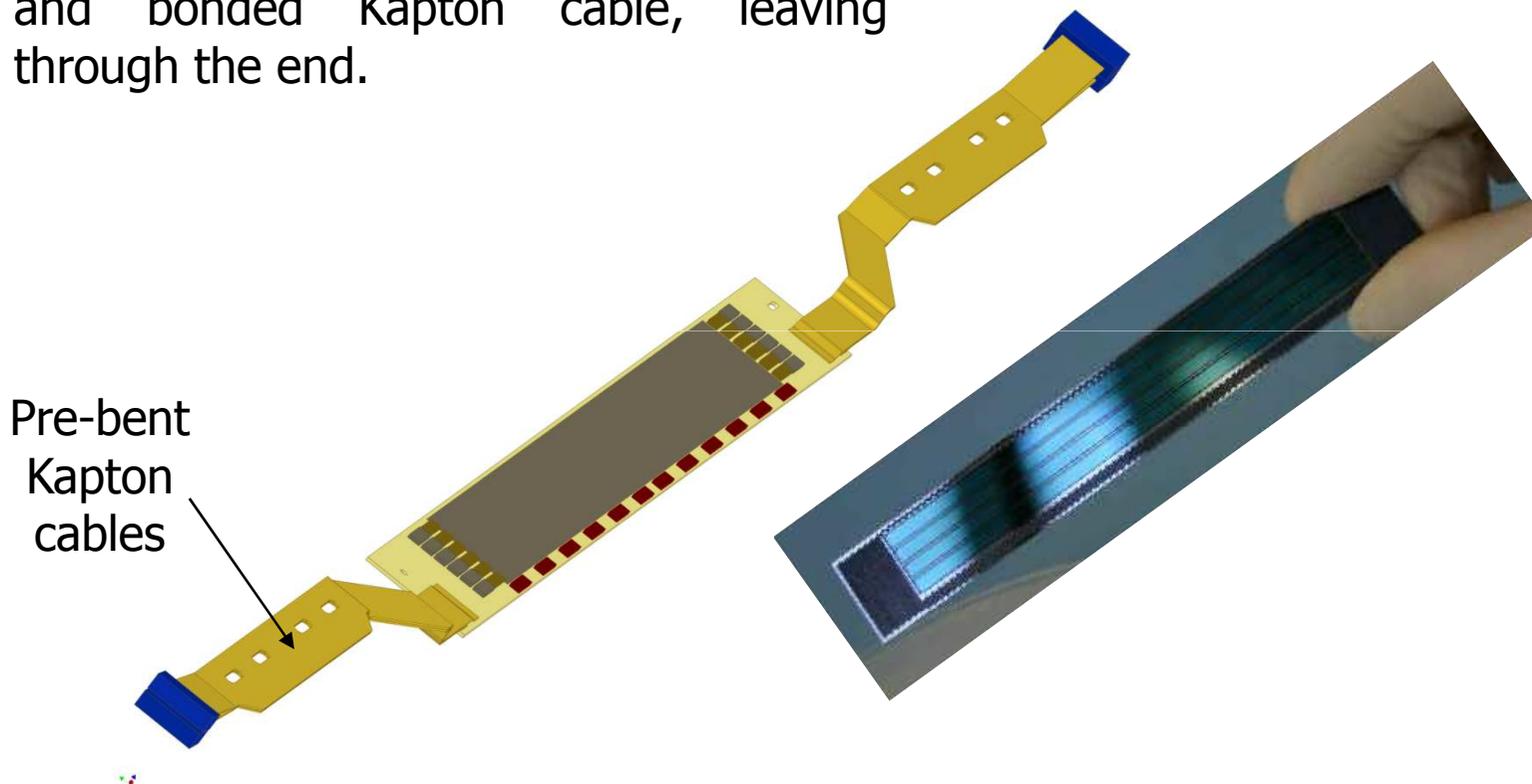
Single muon tracks



- The Belle-II PXD ladder: The all silicon module

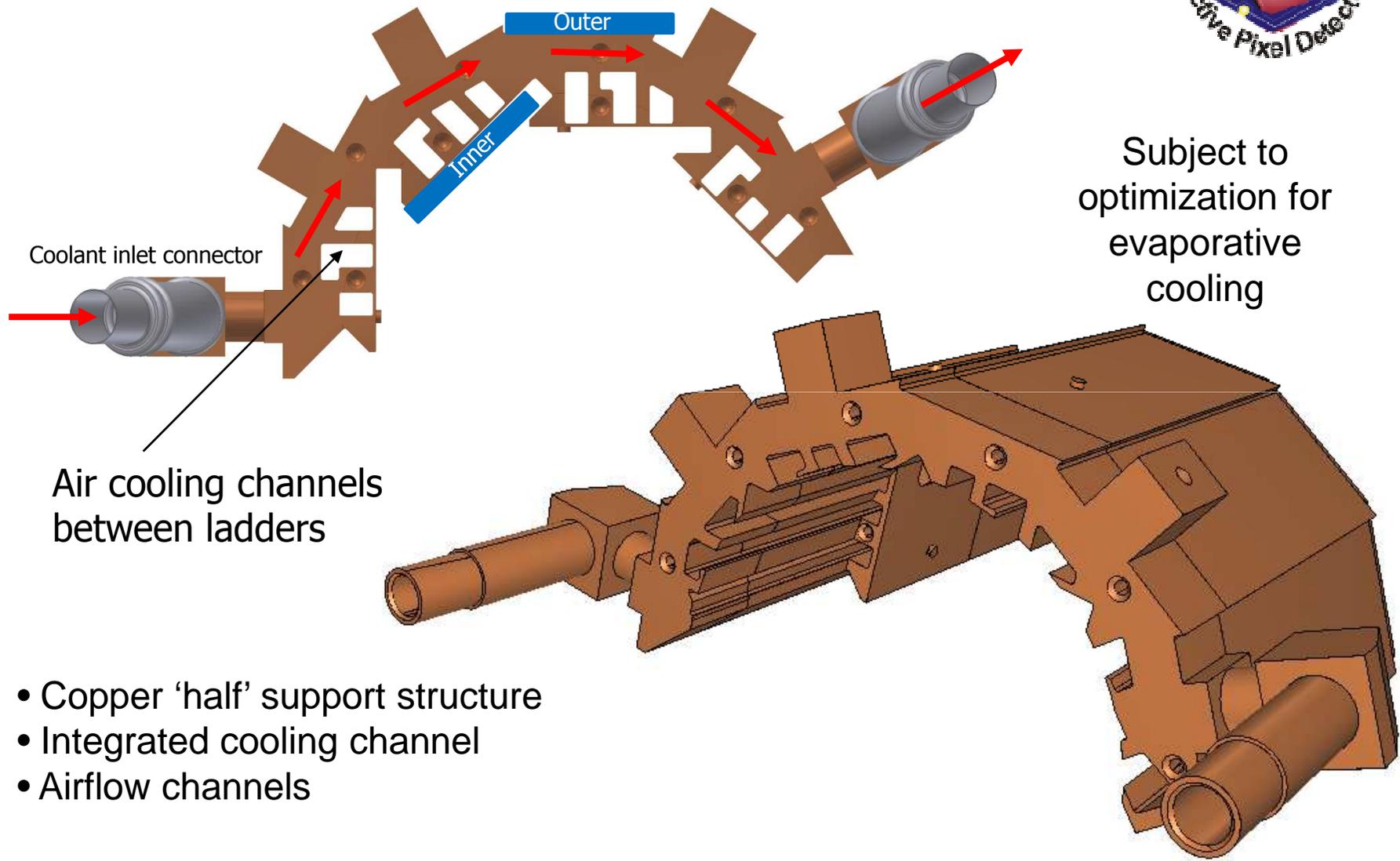


A fully equipped ladder, with electronics and bonded Kapton cable, leaving through the end.



With this geometry in mind... let's design the support...

● Integrated Support and Cooling Structure (ISCS)



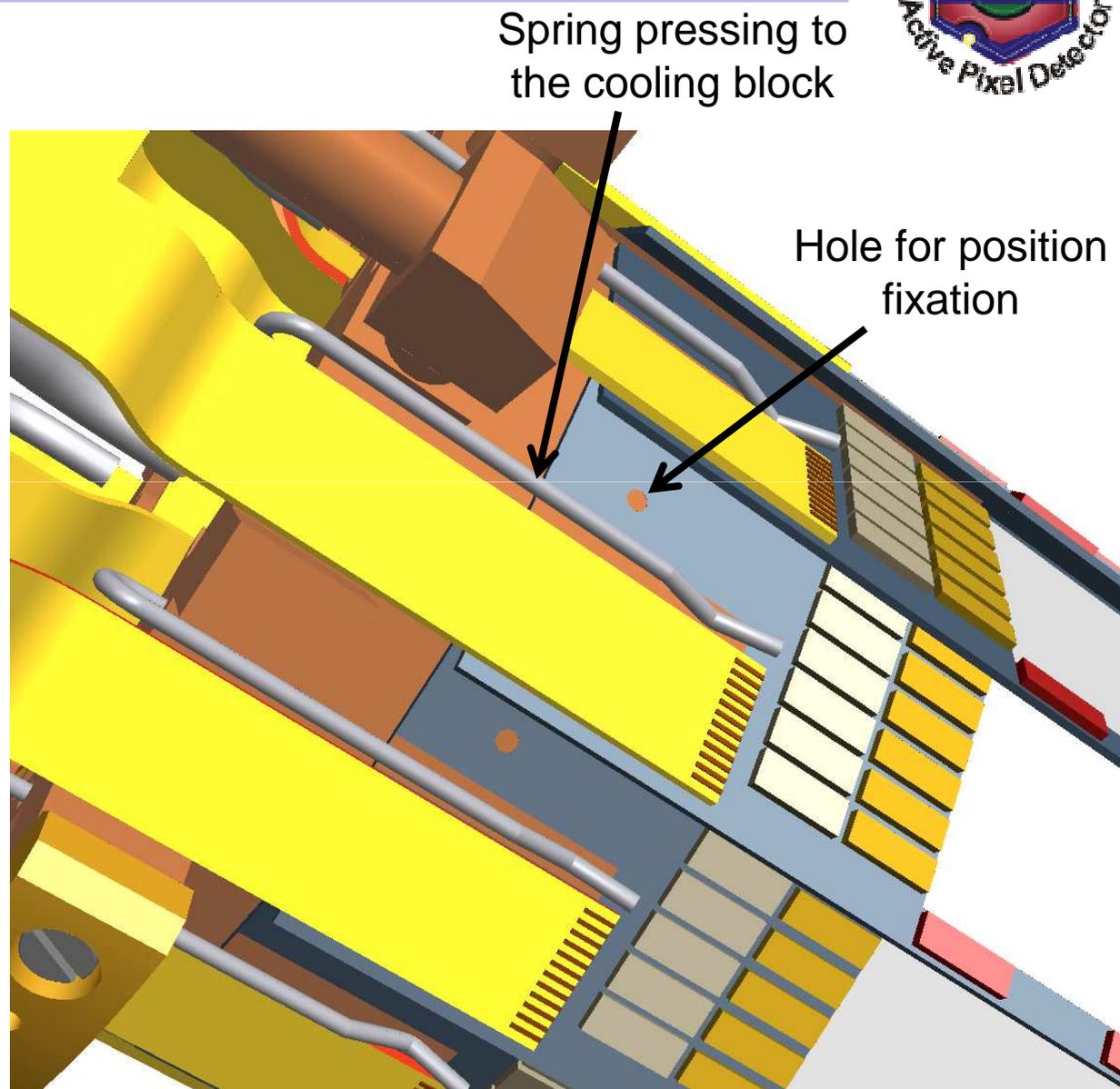
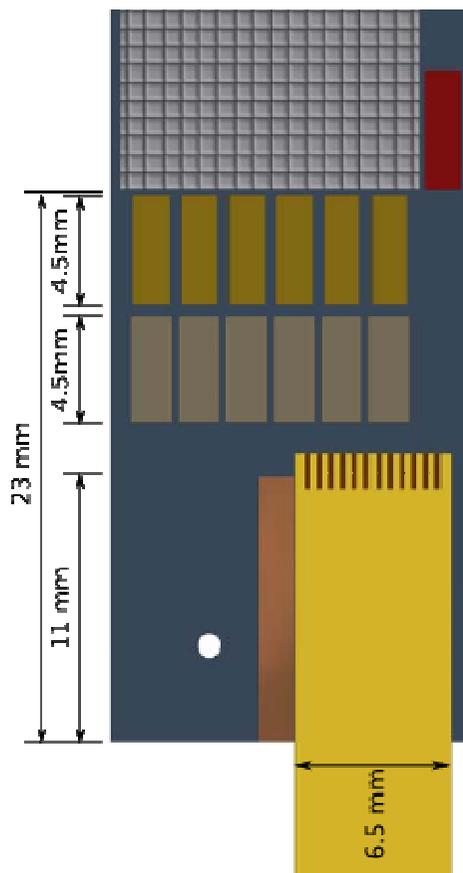
Air cooling channels between ladders

Subject to optimization for evaporative cooling

- Copper 'half' support structure
- Integrated cooling channel
- Airflow channels

❑ Idea: Put the cooling block directly under the sensor and the electronics

- End of stave layout



- Design components



Beampipe

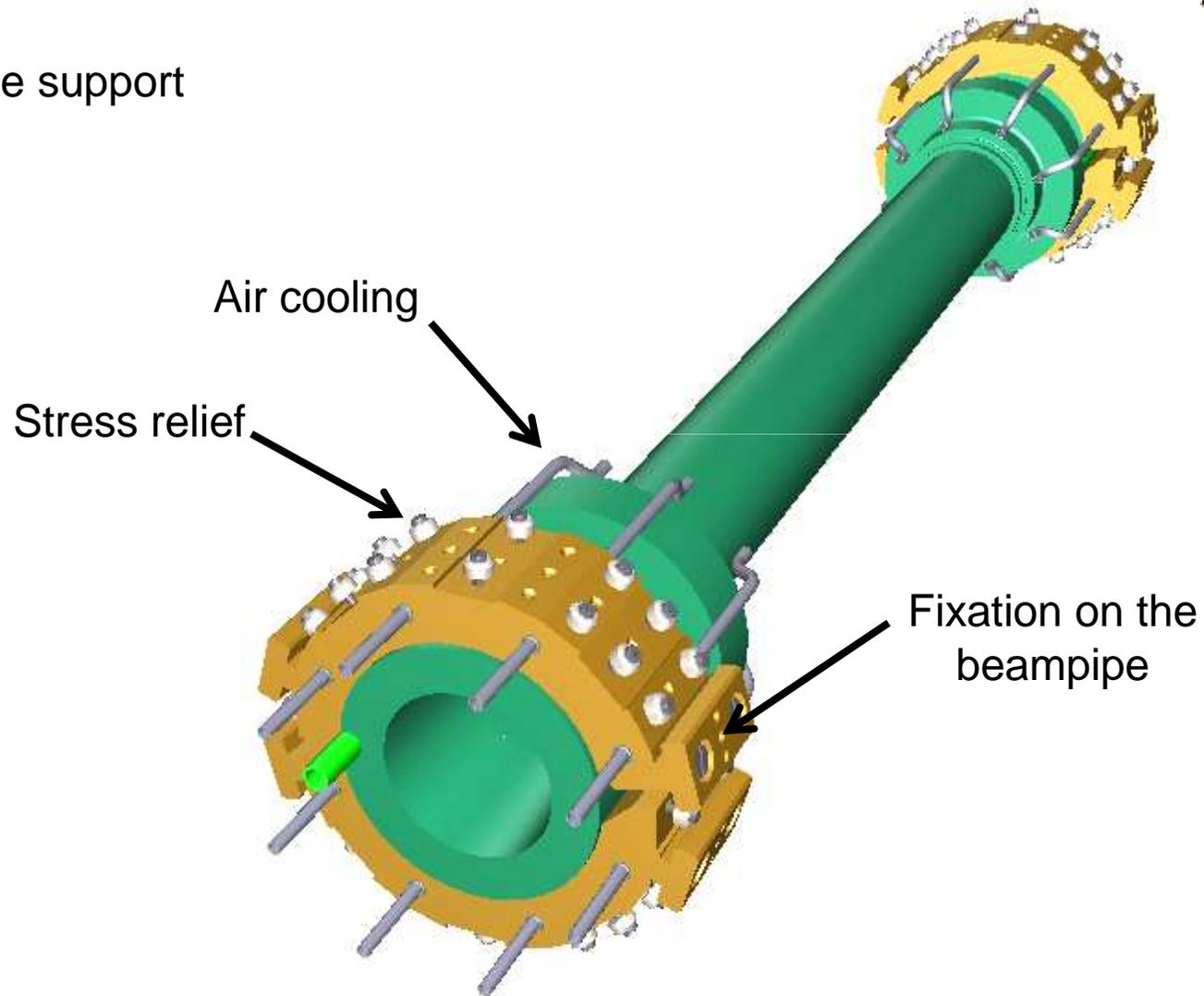
Beampipe cooling



- Design components



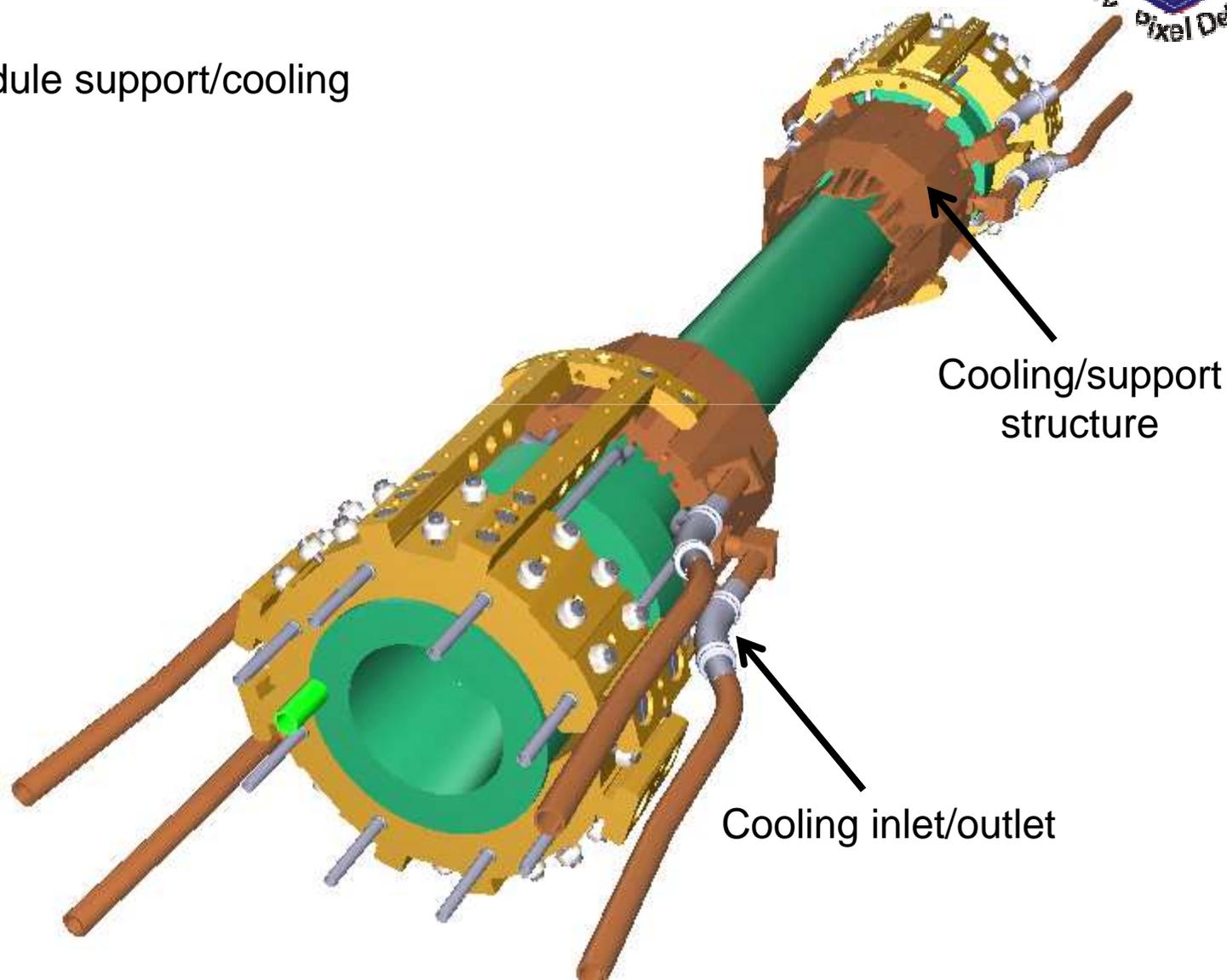
Beampipe support



- Design components



PXD Module support/cooling



Cooling/support structure

Cooling inlet/outlet

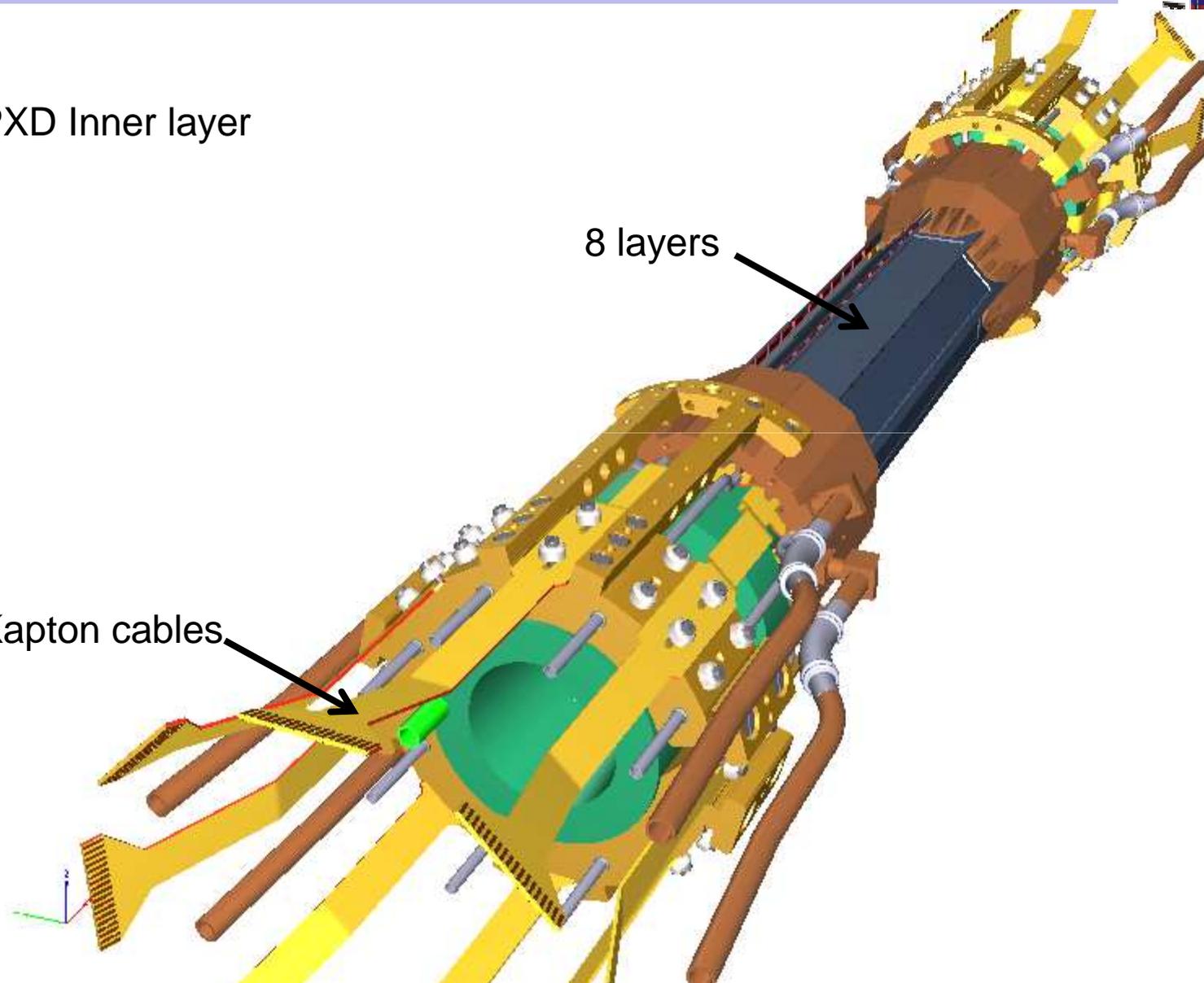
- Design components



PXD Inner layer

8 layers

Kapton cables

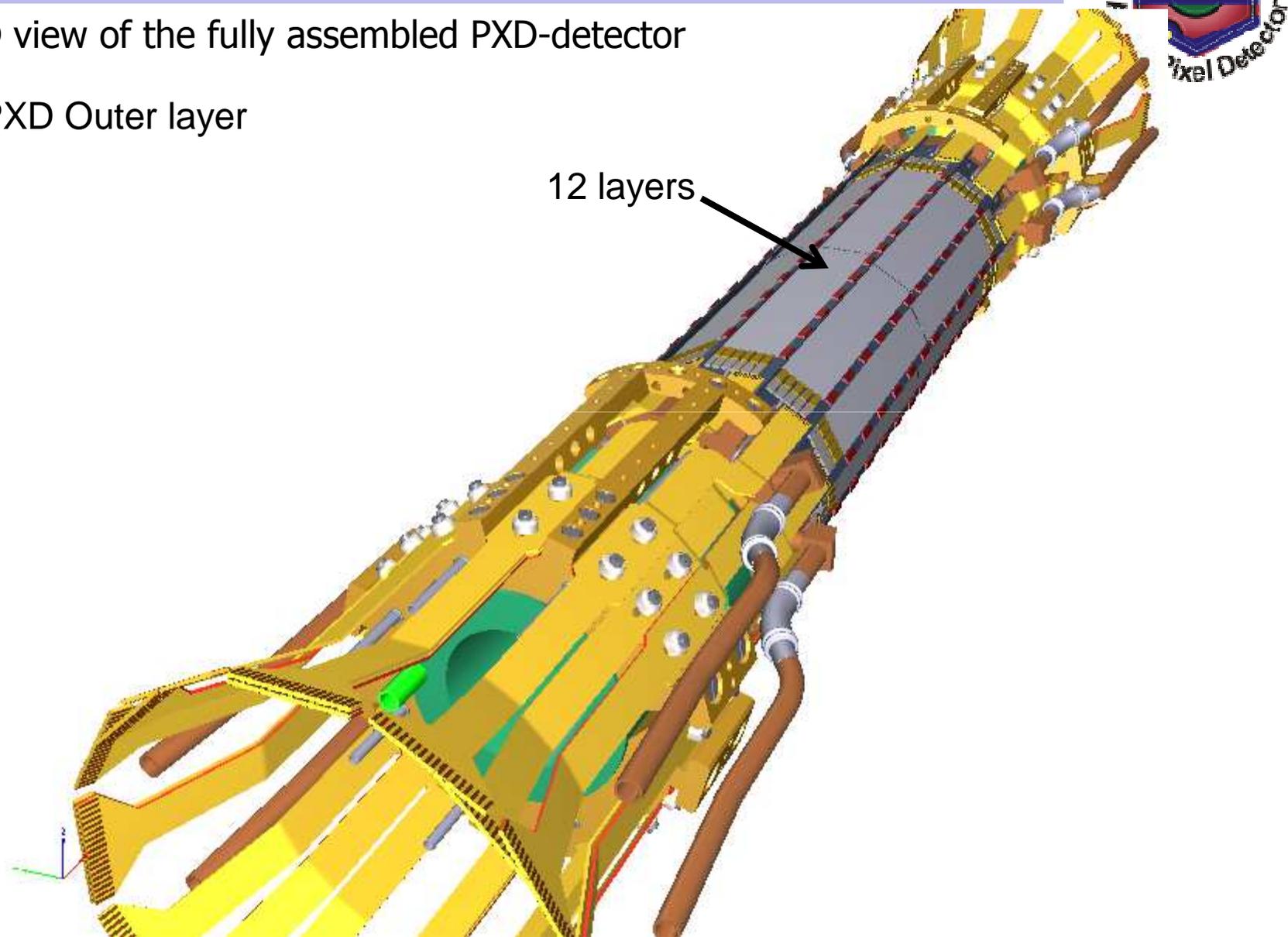


- Design components

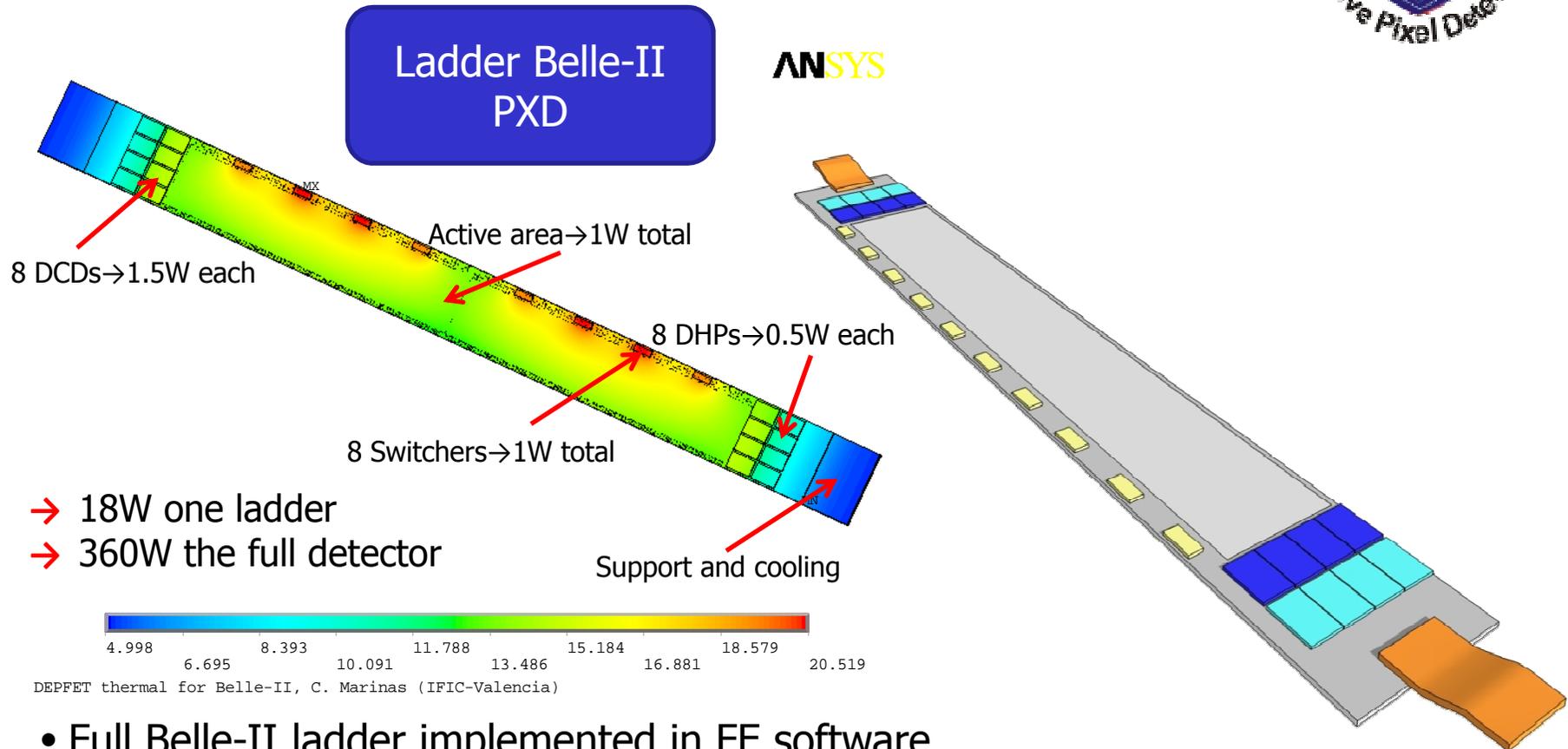
3-D view of the fully assembled PXD-detector

PXD Outer layer

12 layers



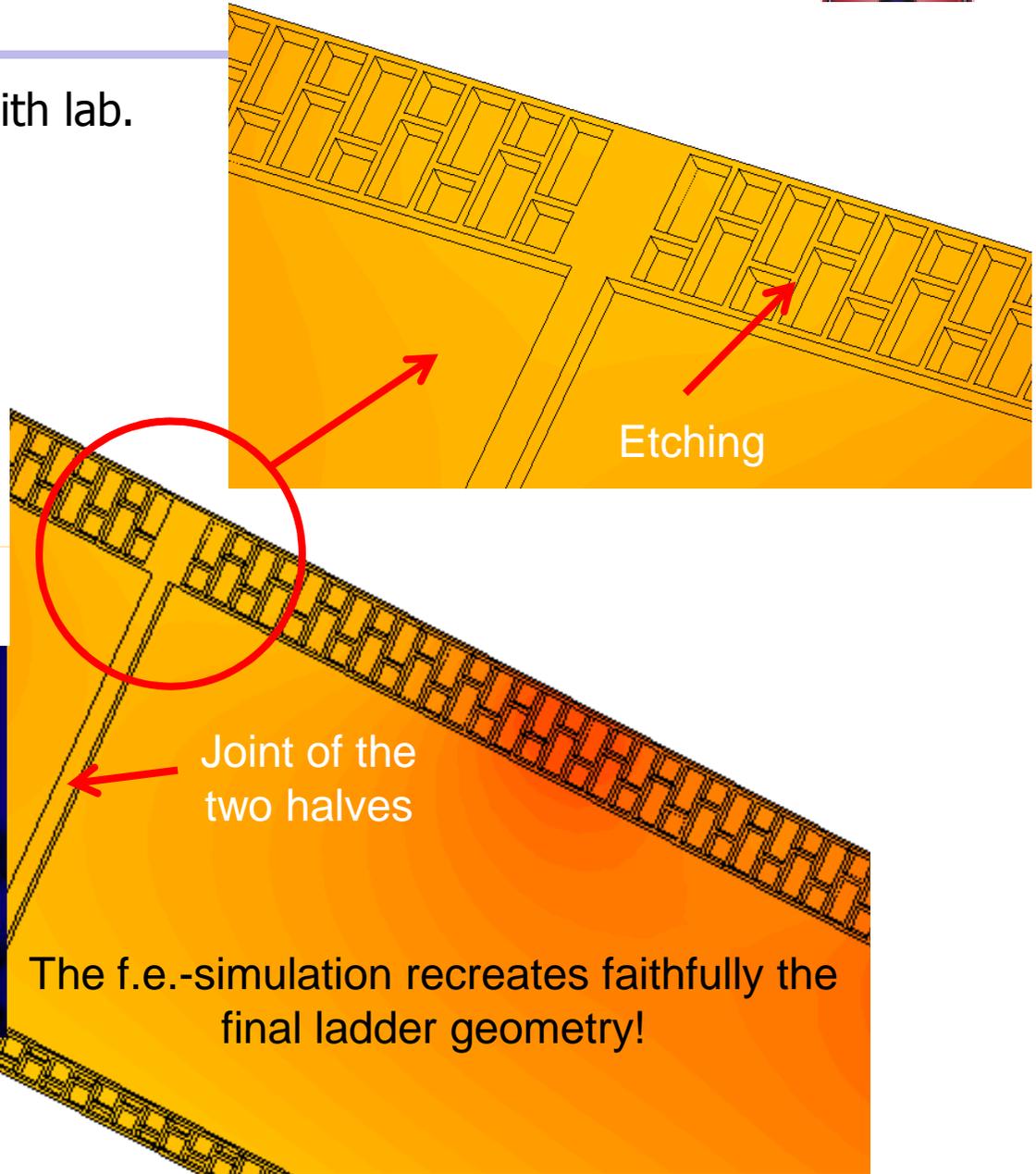
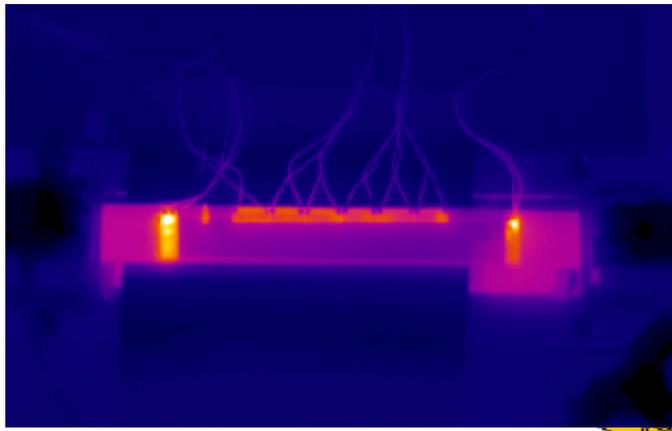
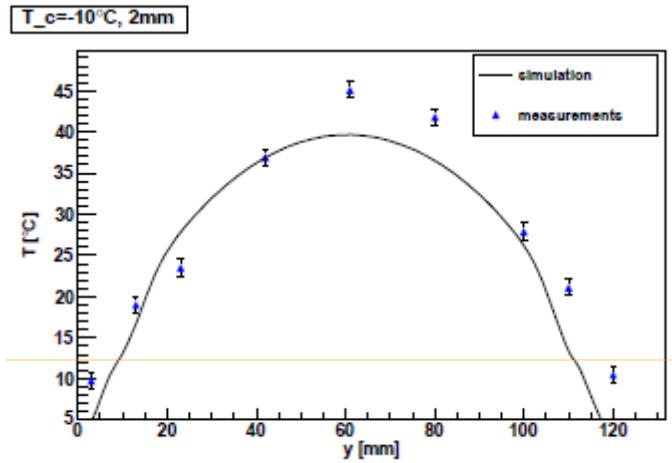
- Thermal studies



- Full Belle-II ladder implemented in FE software
- Development of cooling options imposing upper limits on the temperatures:
 - T_{\max} (Sensor) < 30°C
 - T_{\max} (Chips) < 60°C

- Frame perforation

Simulations cross-checked with lab. measurements

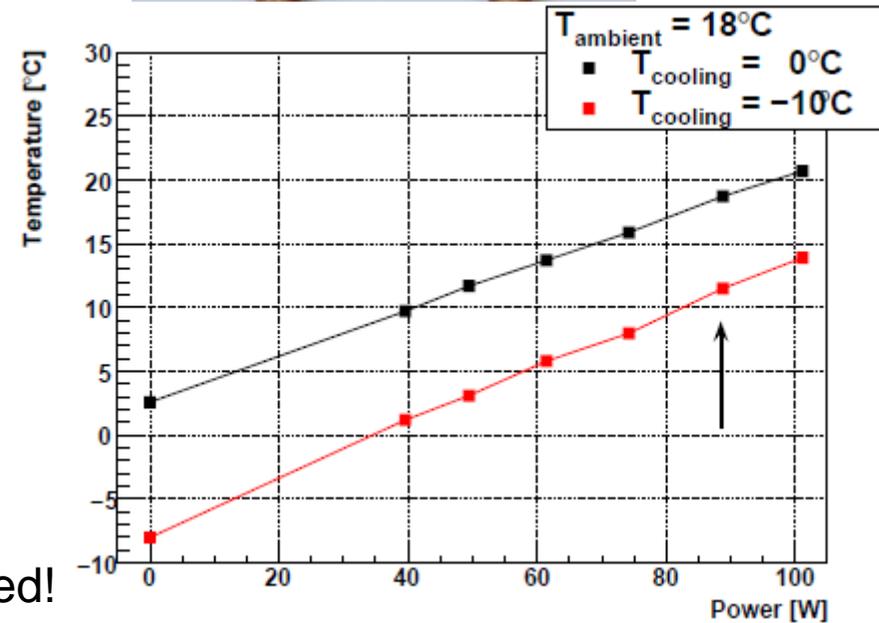
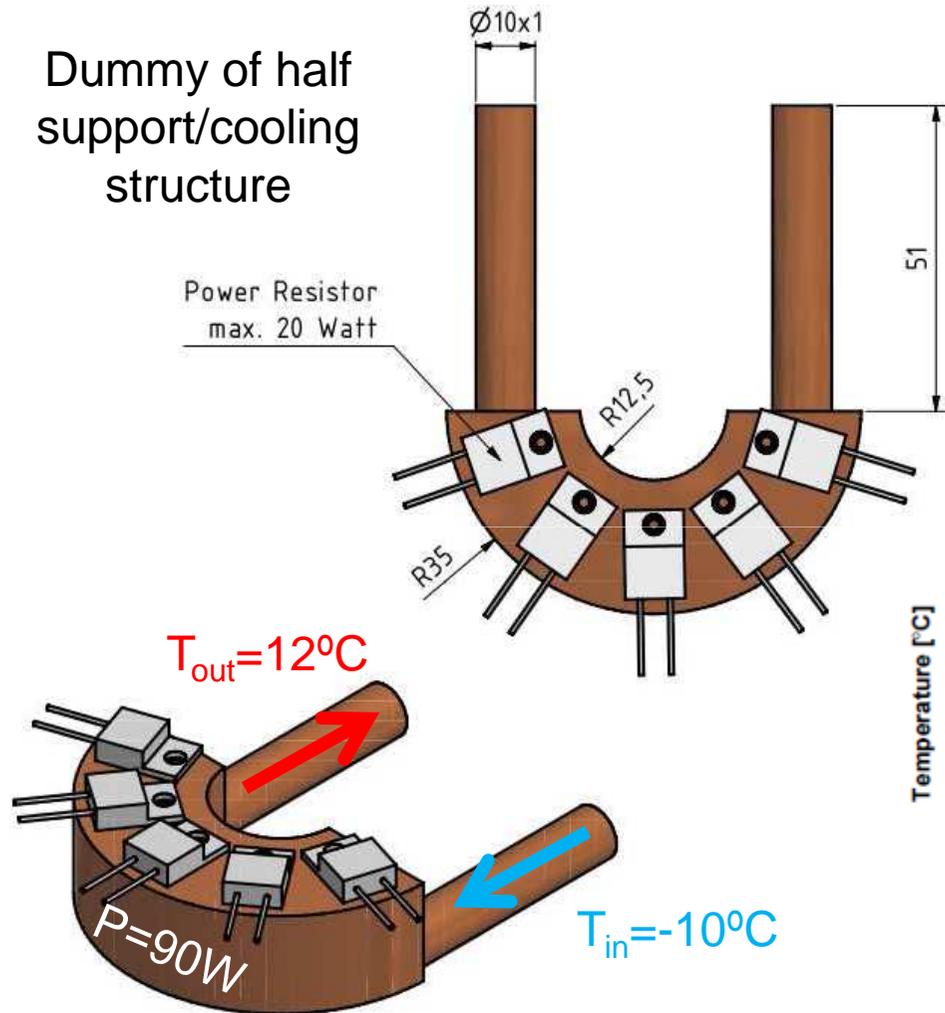


The f.e.-simulation recreates faithfully the final ladder geometry!

- Dummy support ring



Dummy of half support/cooling structure



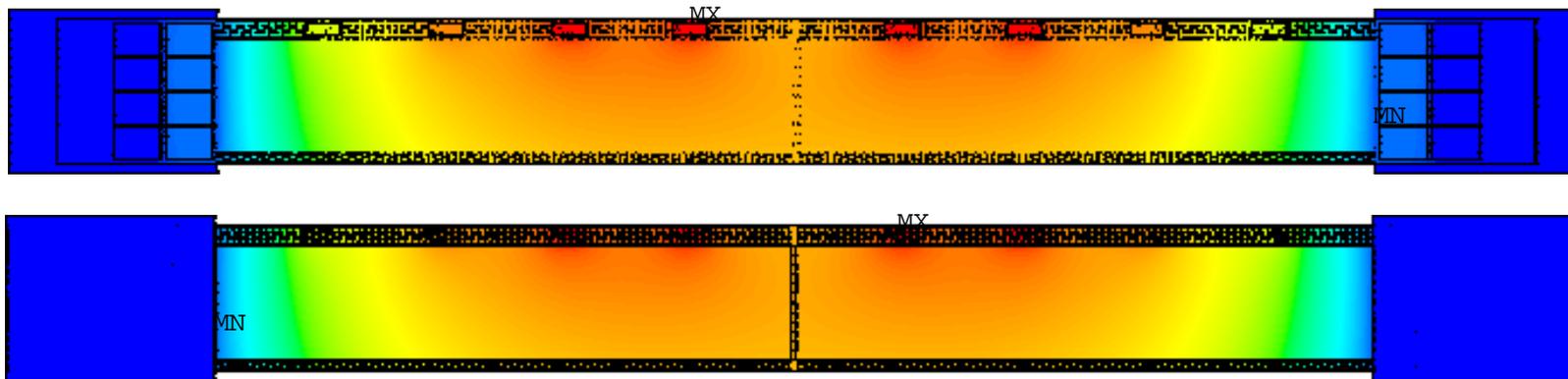
A temperature drop of ~20°C is expected!

- Evaporative cooling **without** cold-dry volume

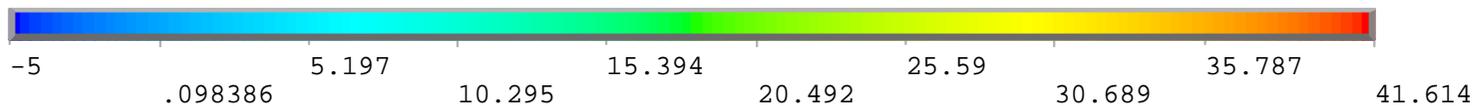


$T_{env} = 15^{\circ}\text{C}$ (**Without** cold-dry volume)
 $T_{coolingblock} = -5^{\circ}\text{C}$ ($-25^{\circ}\text{C} \rightarrow \text{CO}_2$ cooling inlet)

htc=27.52 W/m²-K | Air speed=1 m/s
 Sensor thk.=50 um
 $T_{env} = 15^{\circ}\text{C}$ | $T_{cb} = -5^{\circ}\text{C}$
 k bumps=6 W/m-K | k contacts=3 W/m-K
 Without TPG



$T_{max} = 41^{\circ}\text{C} !!!$



DEPFET thermal for Belle-II, C. Marinas (IFIC-Valencia)

→ From lab measurements with mockups, the center of the sensor is a forced air issue...

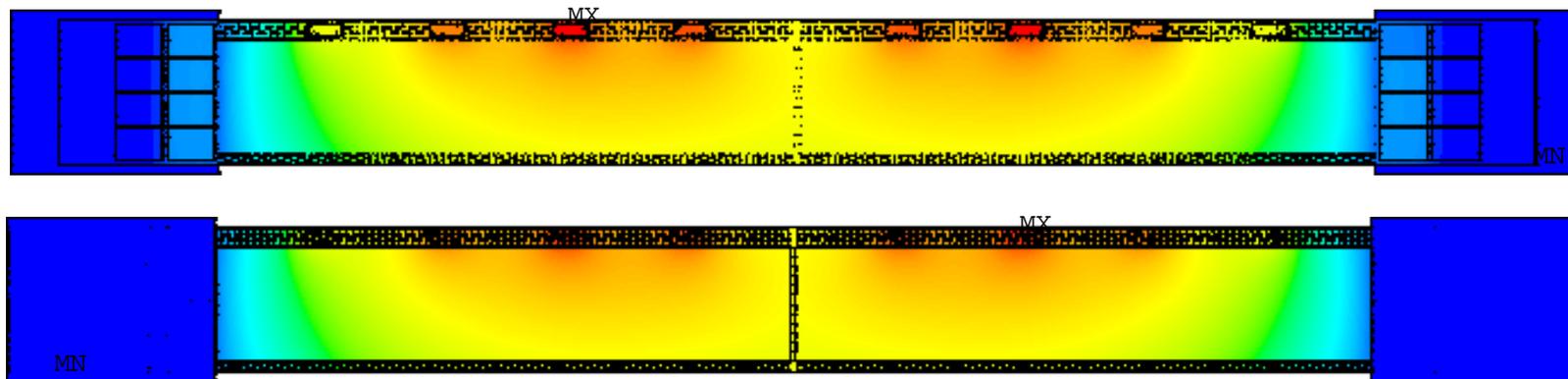
- Evaporative cooling with cold-dry volume



$T_{env} = -8^{\circ}\text{C}$ (**With** cold-dry volume)

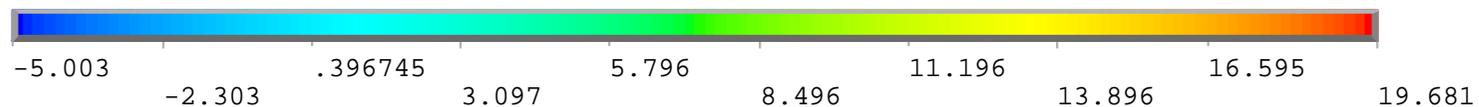
$T_{coolingblock} = -5^{\circ}\text{C}$ ($-25^{\circ}\text{C} \rightarrow \text{CO}_2$ cooling inlet)

htc=27.52 W/m²-K | Air speed=1 m/s
 Sensor thk.=50 um
 $T_{env} = -8^{\circ}\text{C}$ | $T_{cb} = -5^{\circ}\text{C}$
 k bumps=6 W/m-K | k contacts=3 W/m-K
 Without TPG



$\Delta T_{\text{Sensor}} = 24^{\circ}\text{C}$

$T_{\text{max}} = 20^{\circ}\text{C} !!!$



DEPFET thermal for Belle-II, C. Marinas (IFIC-Valencia)

→ Even with CO₂... **the cold-dry volume with forced air is mandatory!!!**

● Conclusions



- DEPFET is the baseline technology chosen by the Belle-II PXD committee
 - High gain, low material budget, good spatial resolution technology
 - Ready to cope with the Belle-II challenging requirements!
 - Simulation chain is almost ready
 - Best detector configuration is under study
- A 'two in one' cooling/mechanical support structure was presented
 - First design to work with water cooling
 - Could be modified to work with evaporative cooling if needed (CO₂ and C₃F₈ are under evaluation)
- Thermal studies
 - FE simulations were presented
 - Reasonably low temperature on the cooling blocks is needed to cool down the readout chips
 - The center of the ladder must be cooled by forced convection with very cold air!



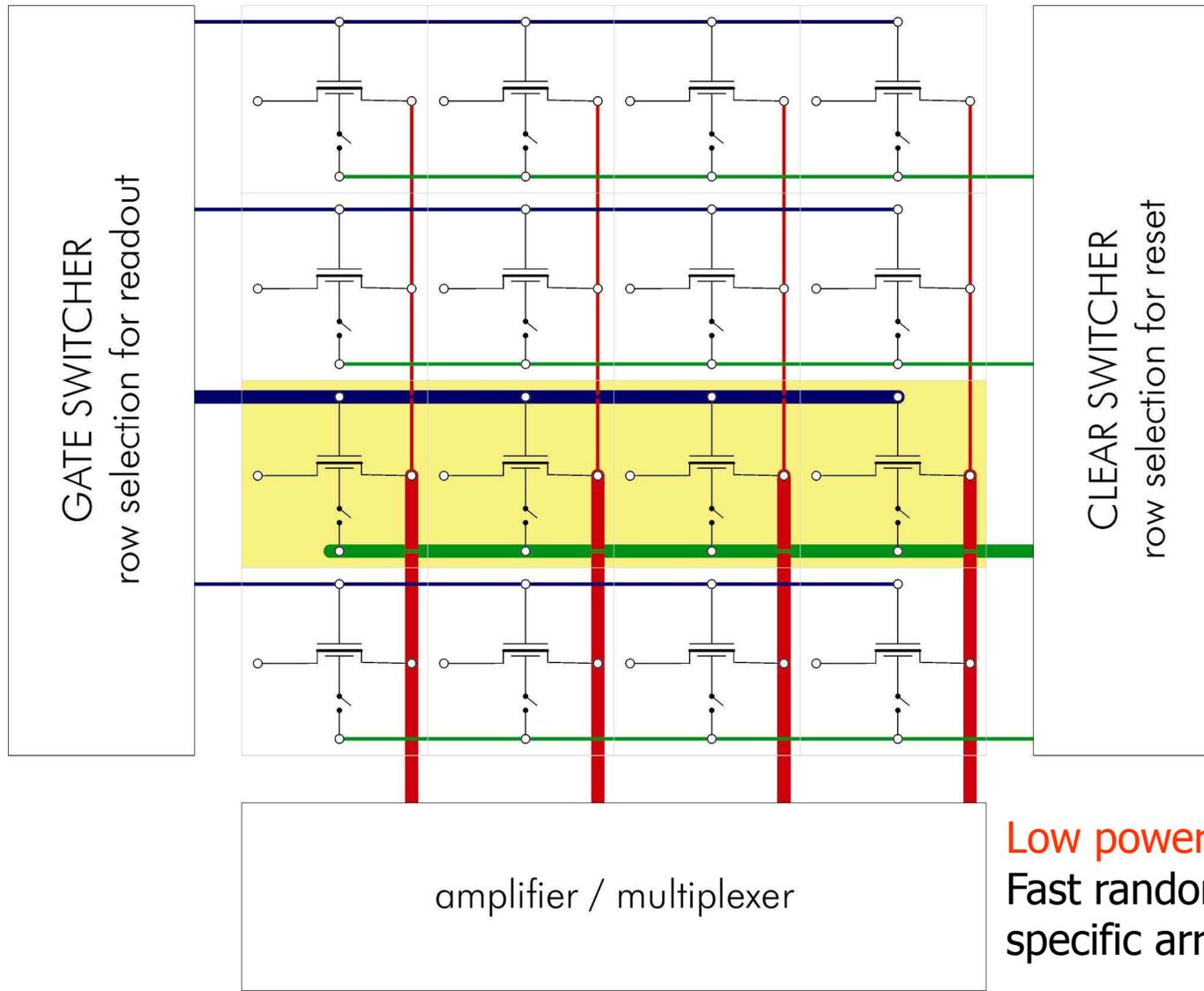
Thank you very much!



Backup slides



● DEPFET: From a pixel to a matrix



Low power consumption
Fast random access to specific array regions

- ILC S3b prototype system



- Hybrid Board

- DEPFET 64x256 matrix
- Readout chip (CURO)
- Steering chips (Switchers)

- S3b Readout Board

- ADCs→Digitization
- FPGA→Chip config. and synchronization during DAQ
- RAM→Data storage
- USB 2.0 board→PC comm.



- The latest DEPFET Generation 'PXD5'

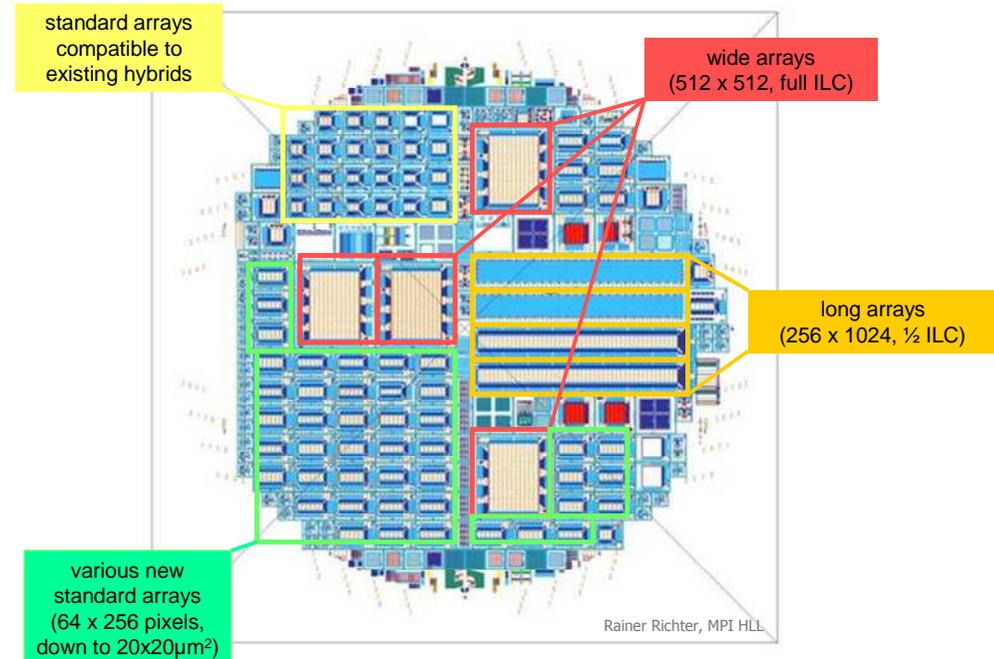
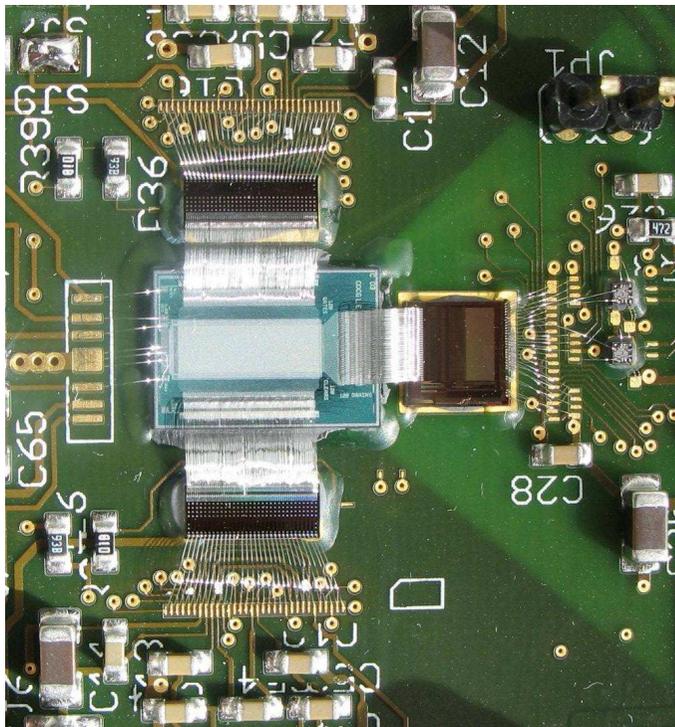


- Longer matrices (256x64 pixels)

- New DEPFET variants:

- ✓ Very small pixels (20 μ m x 20 μ m)
- ✓ Capacitively Coupled Clear Gate (C3G) → New step forward in gain
- ✓ Shorter Gate lengths → Increased internal amplification g_q , (6 μ m in PXD4; 5 μ m in PXD5 → Factor 2 better expected)

→ Test Beam 2009 at CERN

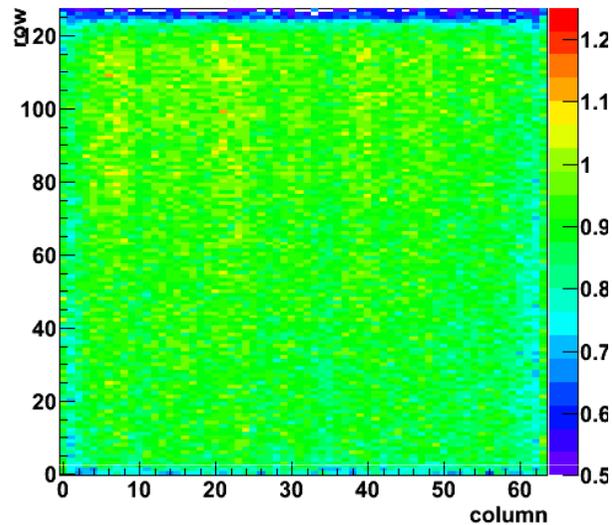


'A system for characterisation of DEPFET silicon pixel matrices and test beam results'. Dr. FURLETOV, Sergey

- TB 2008 and 2009 results



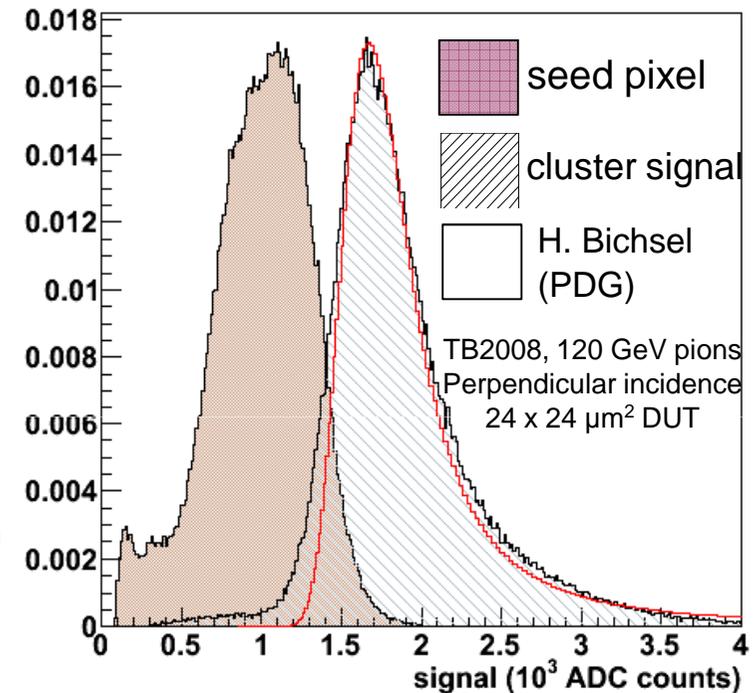
Gain map: Deviation from average seed signal



- 64x128, 24x24 μm^2 Common Cleargate (TB2008)
MPV=1715 ADC counts
 $g_q=363\text{pA/e}^-$

- 64x256, 32x24 μm^2 Capacitive Coupled Cleargate (TB2009)
MPV~2400 ADC counts
 $g_q\sim 500\text{pA/e}^-$

- 64x256, 20x20 μm^2 Common Cleargate, $\text{Length}_{\text{Gate}}=5\mu\text{m}$ (TB2009)
MPV~3100 ADC counts
 $g_q\sim 650\text{pA/e}^-$ (2x previous g_q , as expected)



- TB 2008: Resolution



We cannot ignore multiple scattering (even at 120 GeV) or telescope resolution. DUT resolution measurement obtained by plugging in a theoretical expectation for the Multiple Scattering (either by simulating the setup in GEANT4) and error from tracking fit (P. Kvasnicka).

Module #	0	1	2	3	4	5
X Residual (μm)	2.9	2.2	2.3	2.0	3.1	3.4
Y Residual (μm)	2.3	1.7	1.7	1.7	2.2	2.6
X Resolution (μm)	2.1	1.6	1.9	1.3	2.6	2.4
Y Resolution (μm)	1.5	1.3	1.2	1.2	1.8	1.7

120 GeV pions, perpendicular incidence, $32 \times 24 \mu\text{m}^2$ telescope + $24 \times 24 \mu\text{m}^2$ DUT (3)

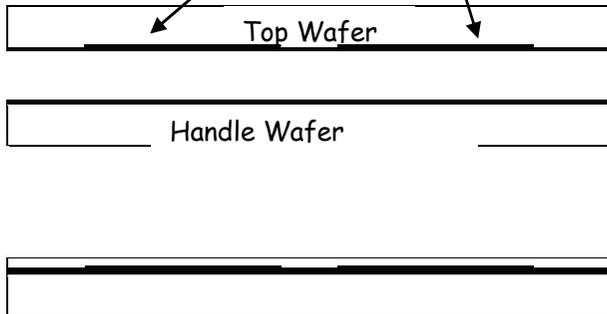
Energy scan is a useful cross-check to disentangle intrinsic resolution-MS correctly.



● Thinning technology



a) Oxidation and back side implant on sensor wafer



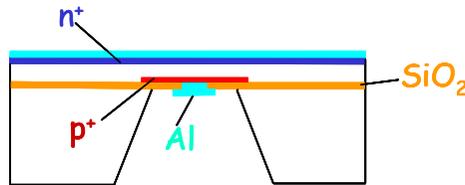
b) Wafer bonding and grinding/polishing of top wafer. Thin sensor side to desired thickness

c) Process DEPFET on top side → passivation



d) Anisotropic deep etching opens "windows" in handle wafer. Structure resist, etch backside up to oxide/implant

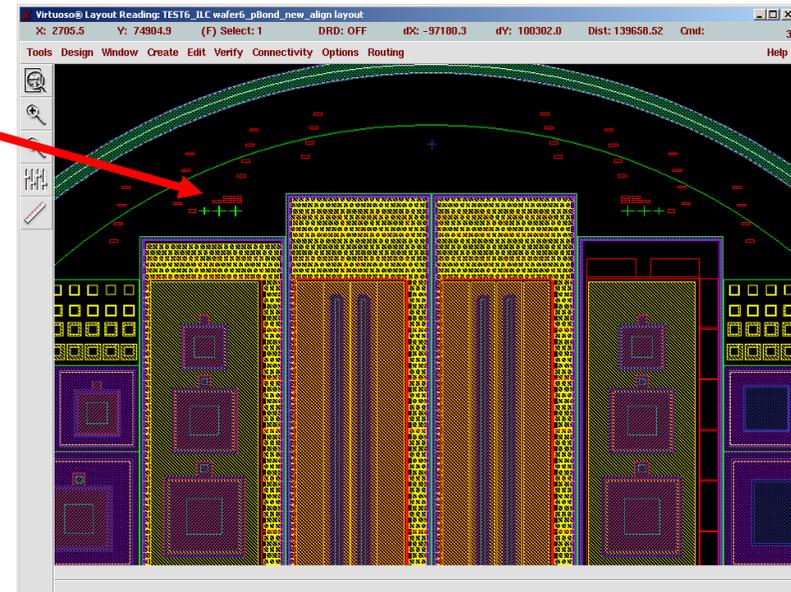
Implants like DEPFET config.



Alignment marks to find the partial p-implant after bonding

unstructured n+ on top
structured p+ in bond region

- Sensor wafer: high resistivity d=150mm wafer.
- Bonded on low resistivity "handle" wafer".
- 50 μm thickness produced
- Rigid frame for handling and mechanical stiffness



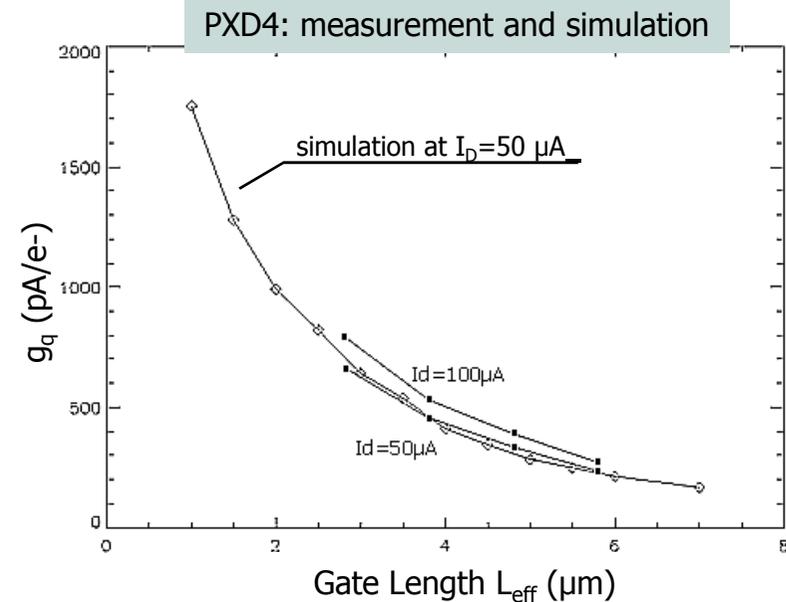
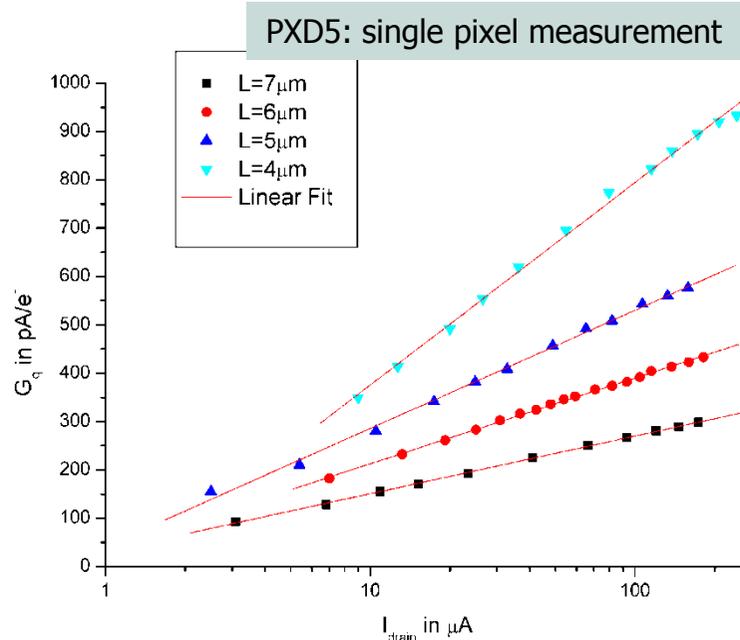
● Internal Amplification



- ✓ The internal amplification measures the change in drain current in the presence of charge in the internal gate:

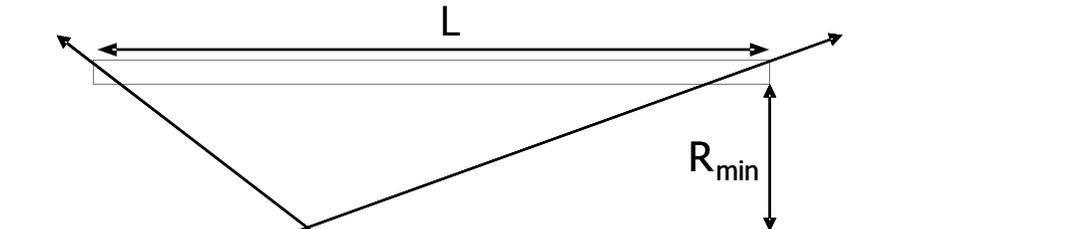
$$g_q = \frac{dI_{ds}}{dQ_{int}} \sim \frac{\sqrt{I_{ds}}}{\sqrt{WL}L^{\frac{3}{2}}}$$

- ✓ Increasing g_q increases SNR
- ✓ Playing with channel length we can achieve up to $g_q \sim 1 \text{ nA/e}^-$
- ✓ PXD4 has $L=6\mu\text{m}$, some matrices in PXD5 have now $L=4\mu\text{m}$ → Expect factor 2 better S/N



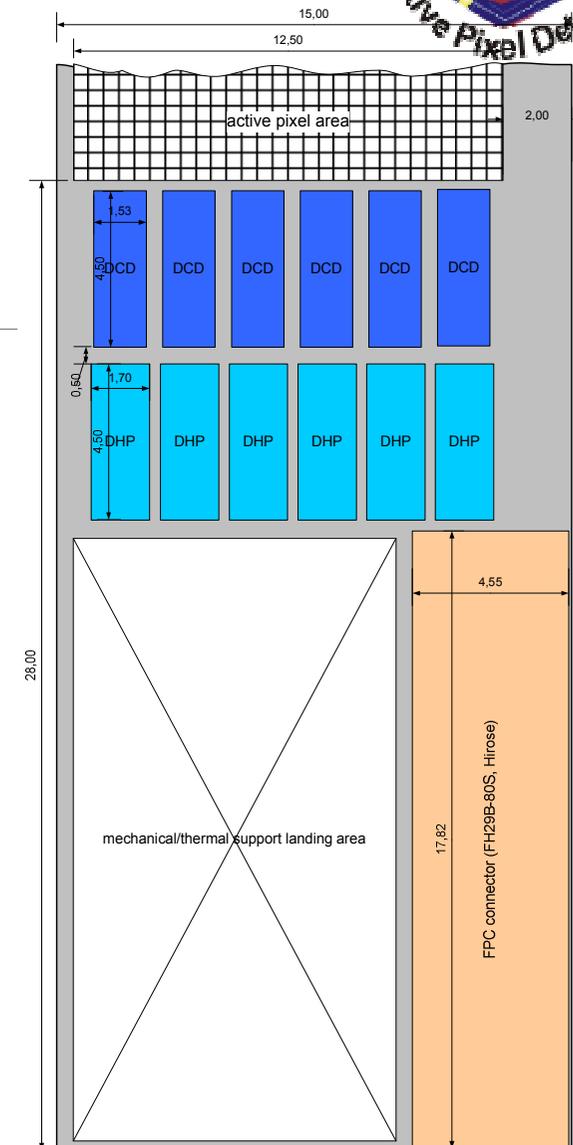
Ladder dimensions

- Monolithic inner layer
- Broken outer layer

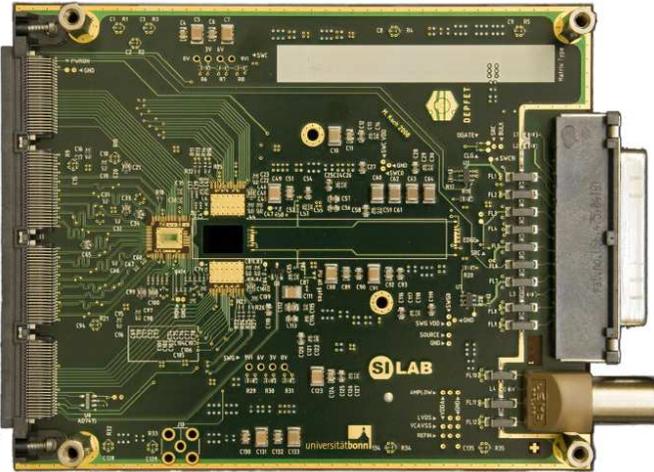


	Layer 1	Layer 2
R_{min} (cm)	1.3	2.2
Sensitive Width (cm)	1.25	1.25
Balcony (cm)	0.2	0.2
Geometrical Width (cm)	1.5	1.5
Sensitive Length (cm)	7.5	11.7
Geometrical Length (cm)	8.06	12.26

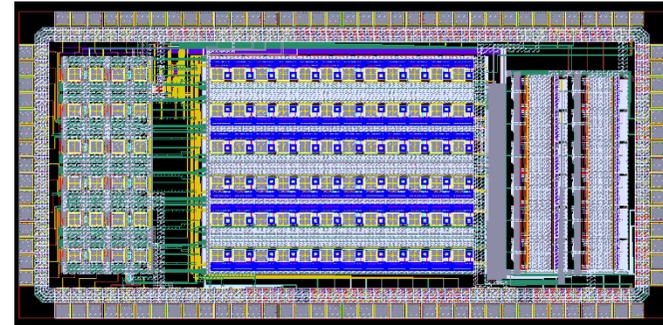
- Sensitive Length_{Inner} = 1000 lines · 75 microns = 7.5cm
- Sensitive Length_{Outer} = 1000 lines · 117microns = 11.7cm
- Sensitive Width = 250 columns · 50 microns = 1.25cm



- A new r/o chip – DCD (Drain Current Digitizer)



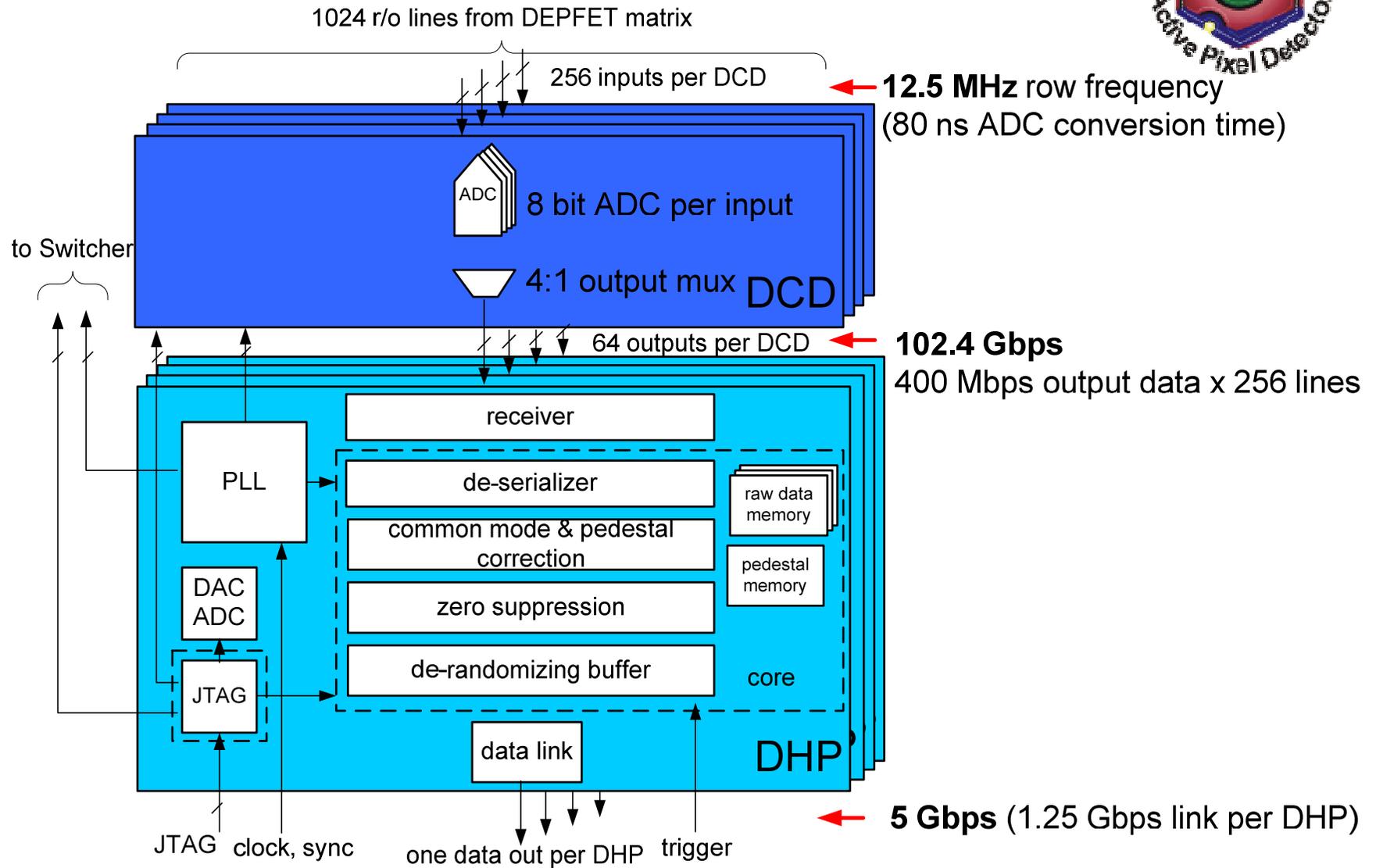
Test chip DCD2: 6X12 channels



- Improved input cascode (regulated) and current memory cells
- Integrated 8bit current based ADC per channel
- Designed for 40 pF load at the input (5cm Drain line)
- Layout for bump bonding, radiation hard design
- Power consumption per channel 2.0 mW (Analog) + 0.8 mW (Digital)
- Digital hit processing done with second digital chip (DHP)



● Signal rates and data flow



● DHP functionality



- timing signal generation
 - PLL controlled DCD clock
 - Switcher sequencer
- signal processing
 - raw data correction: common mode offset and pedestal fluctuations
 - latency buffer
 - data reduction: 0-suppression, triggered r/o
- module interface
 - module slow control interface (JTAG chain including DCD and Switcher chips)
 - Gigabit data link

- Components irradiations



Component	Process	max	Dose	Result	comment
DCD	UMC 180nm	10MRad	7.5MRad	ok	DSM CMOS
Switcher3	AMS 0.35	10MRad	5.7MRad	ok	DSM CMOS
Switcher4	AMS 0.35 HV	10MRad	36MRad	ok	
DHP	IBM 90nm	10MRad			DSM CMOS
Optolink		?MRad			
DHH ASIC		?MRad			
Regulator		?MRad			

The ASICS will work well for the Belle-II doses

irradiation	TID / NIEL fluence	ΔV_{th}	g_m	I_{Leak} in int. gate at RT(*)
gamma ^{60}Co	913 krad / ~ 0	$\sim -4V$	unchanged	156 fA
neutron	~ 0 / 2.4×10^{11} n/cm ²	~ 0	unchanged	1.4 pA
proton	283krad / 3×10^{12} n/cm ²	$\sim -5V$	$\sim -15\%$	26 pA

(*) 5..22 fA non irradi.



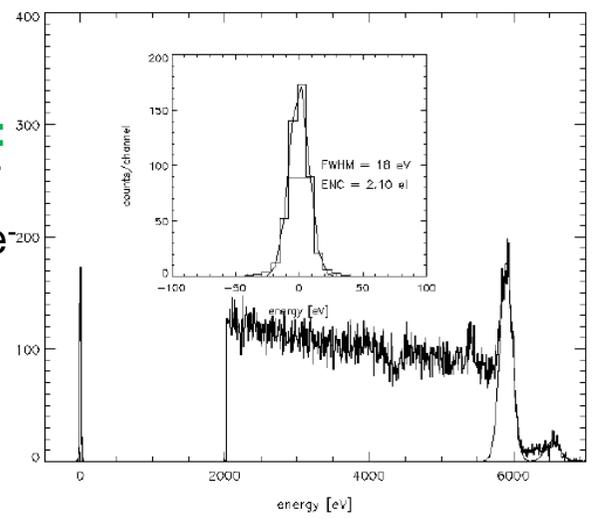


Irradiations

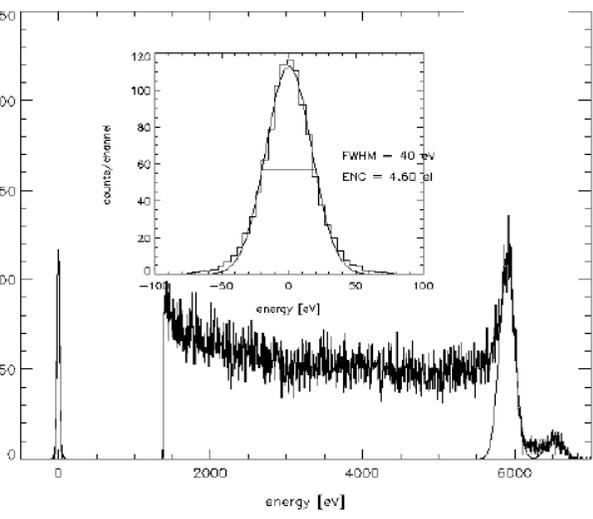
- ✓ Non ionizing Energy Loss (NIEL)
 - Leakage current increase -> shot noise
 - Trapping not critical
- ✓ Ionizing radiation – Total Ionizing dose (TID)
 - 2 MOS gates (Gate, Clear Gate) susceptible to be damaged
 - Fixed oxide positive charge -> ΔV_T
 - Interface trap density
 - Reduced mobility (g_m)
 - Higher 1/f noise

$$ENC = \sqrt{\underbrace{\alpha \frac{8kTg_m}{3g_q^2} \frac{1}{\tau}}_{\text{Therm. noise}} + \underbrace{2\pi a_f C_{tot}^2}_{1/f} + \underbrace{qI_{Leak}\tau}_{I_L}}$$

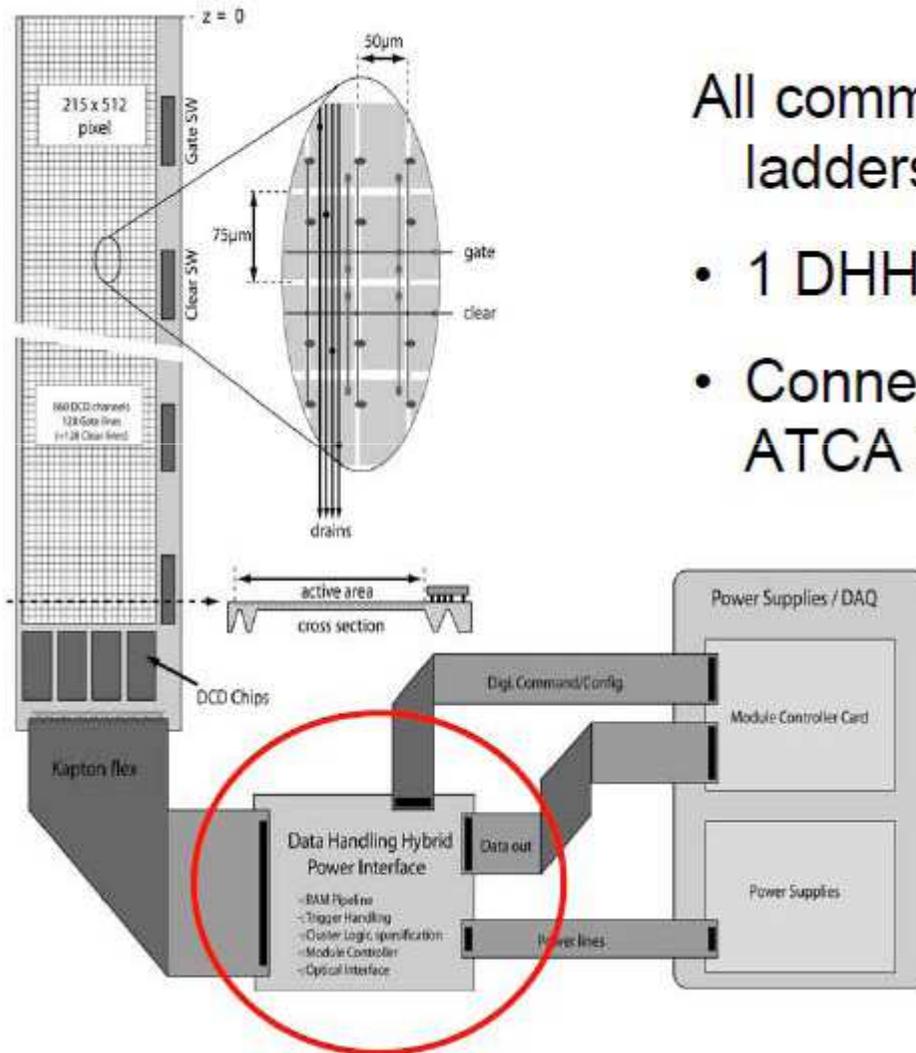
Unirradiated:
 $\tau=10\mu s$ $T=RT$
 $ENC_{noi} = 2.1e^{-}$



4 MRad X-Ray
 $\tau=10\mu s$ $T=RT$
 $ENC_{noi} = 4.6e^{-}$



- Data Handling Hybrid (DHH)

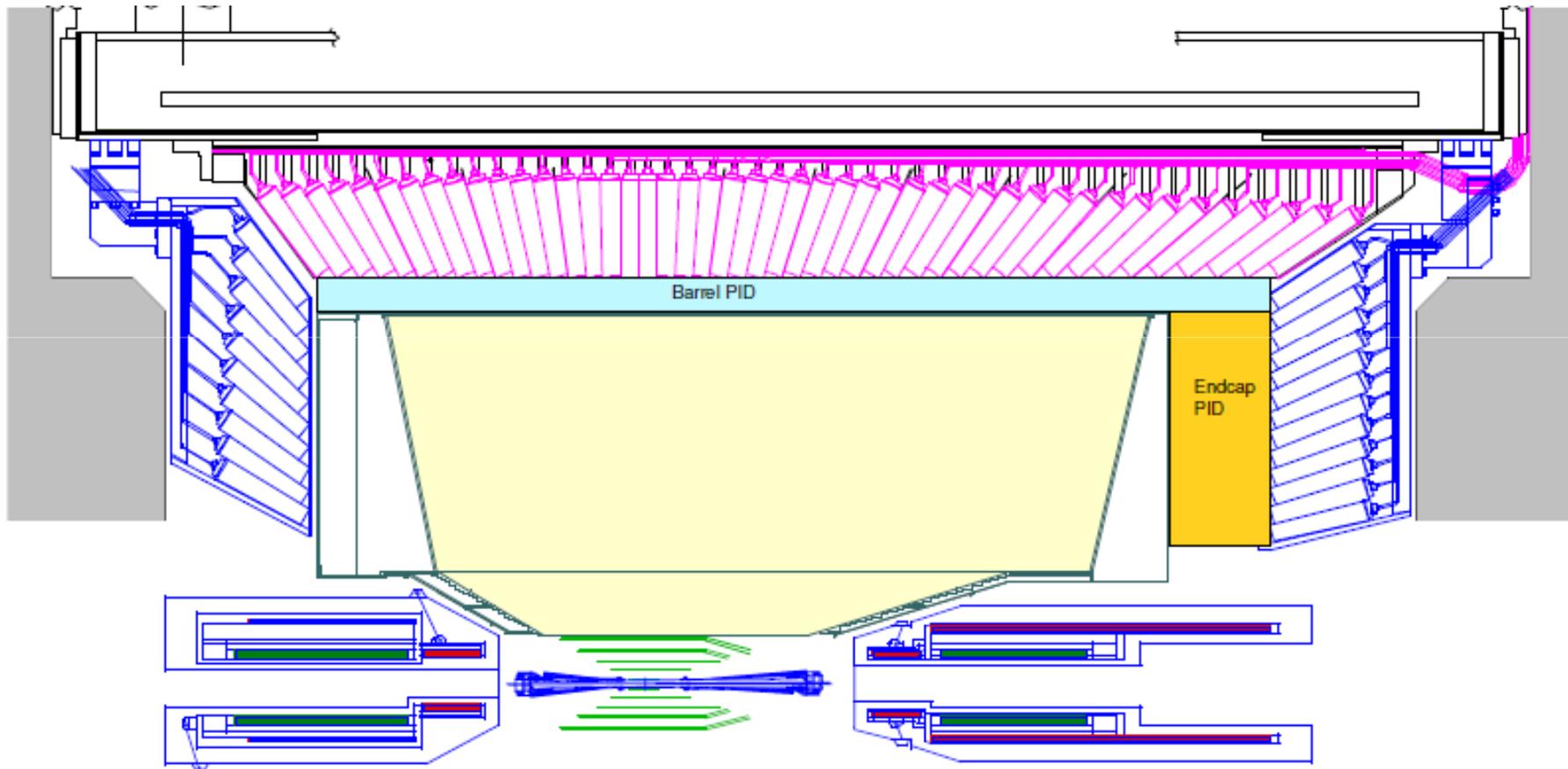


All communication from and to the ladders goes through the DHH !

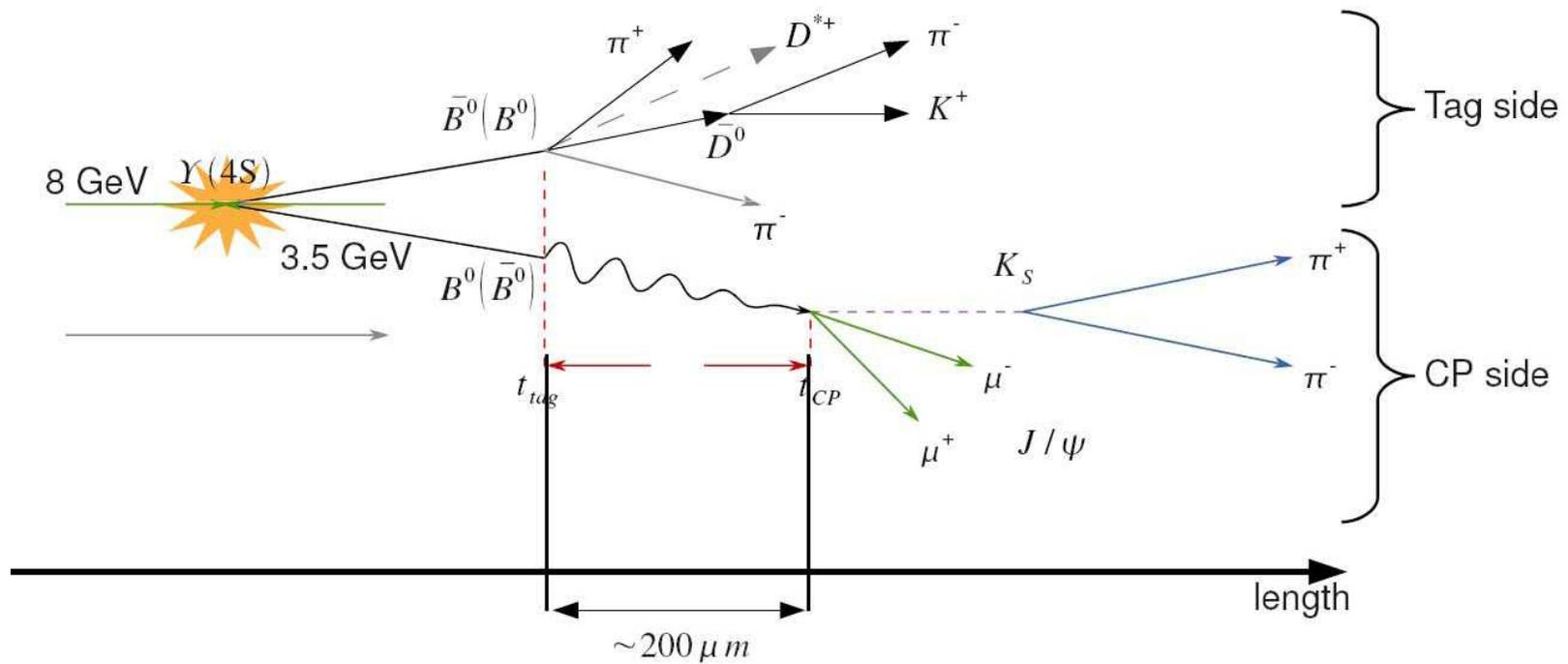
- 1 DHH per half-ladder (total 40)
- Connection between DHP and ATCA DAQ system

- Impedance matching
- Electrical ↔ optical
- Power filtering
- Local power regulation (?)
- Slow control (JTAG)

- Common cold dry volume



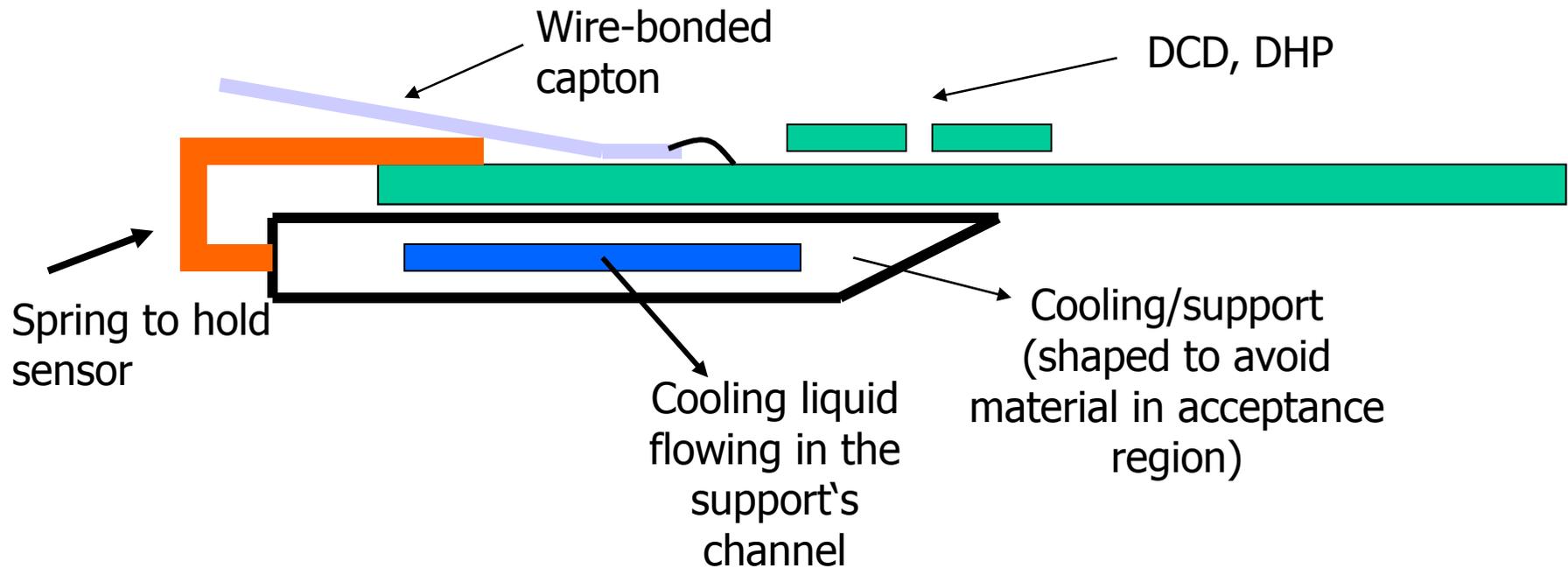
- Golden Channel



- Belle-II PXD schematic support



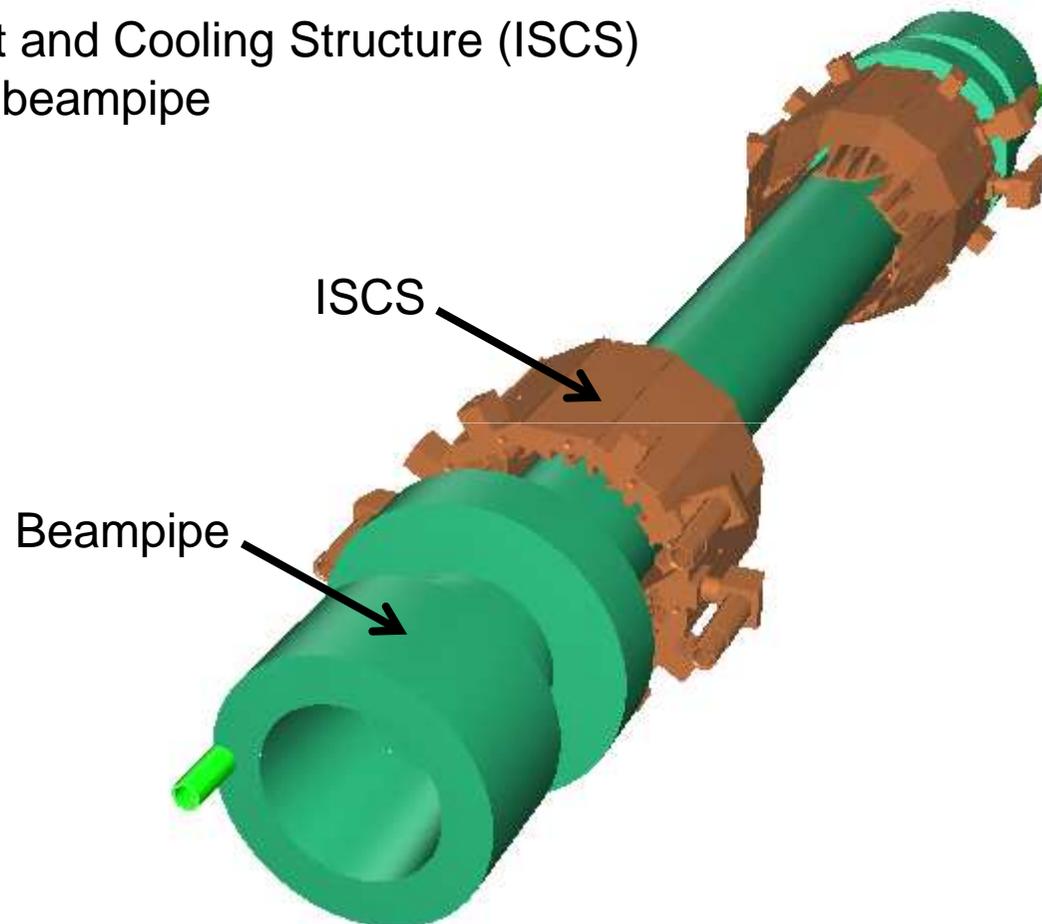
- Idea: Put the cooling block directly under the sensor and the electronics
- This way, the cooling structure and support are the same unit



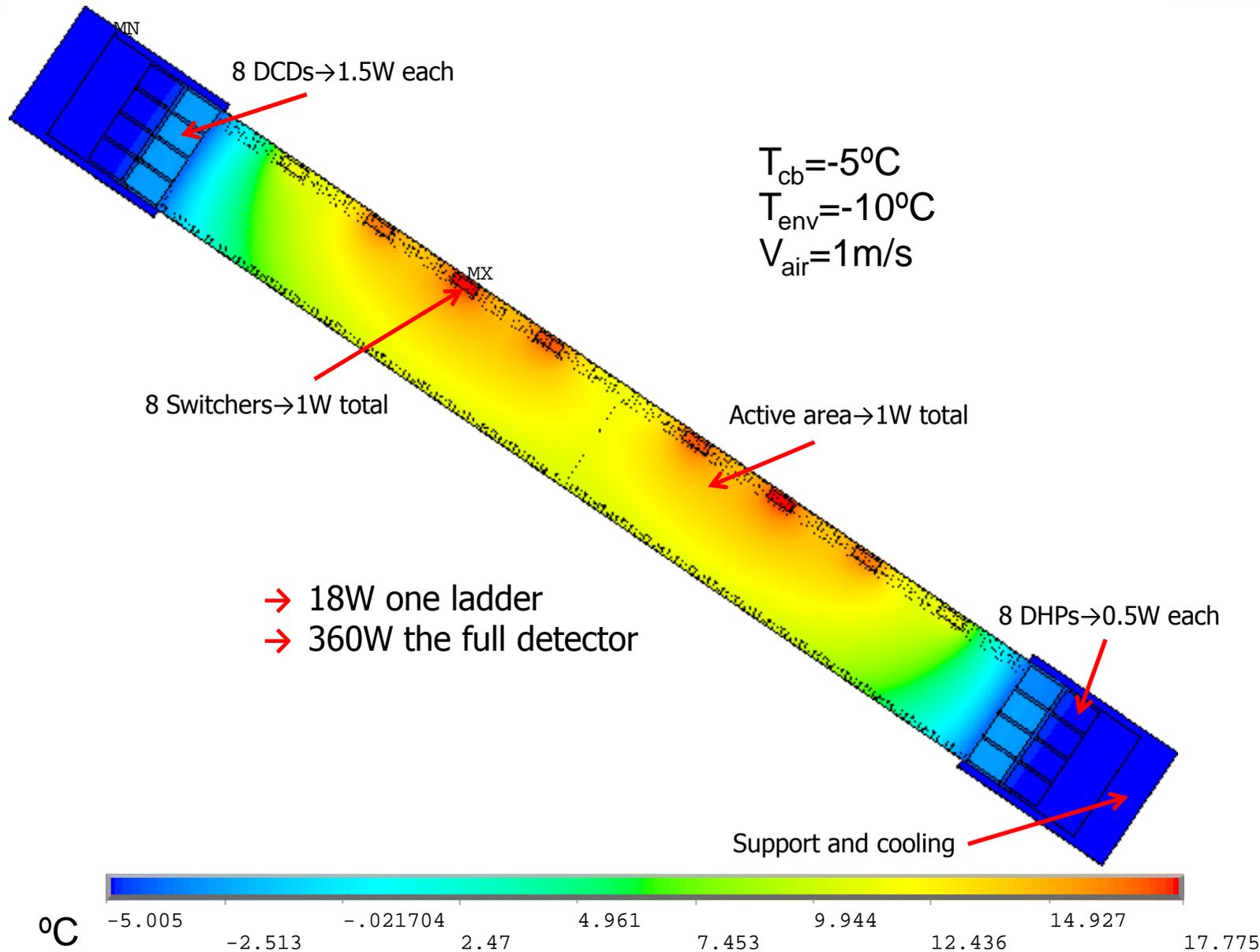
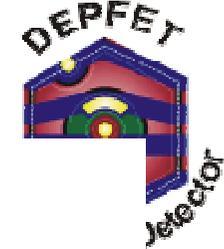
- Design components



Integrated Support and Cooling Structure (ISCS)
assembled on the beampipe



● Thermal studies

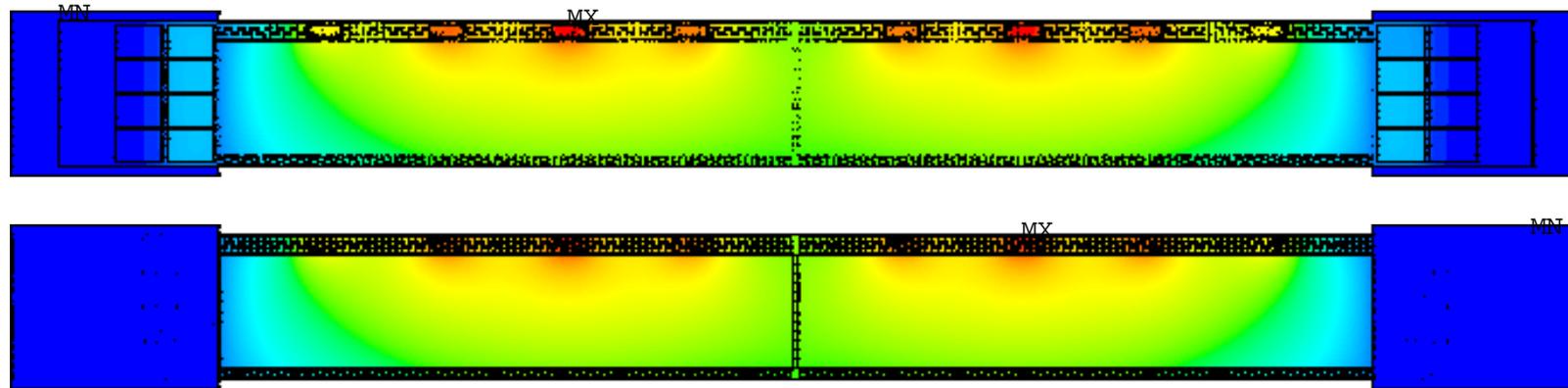


- Water cooling (Ideal world)



$T_{env} = -8^{\circ}\text{C}$ (Cold-dry volume)
 $T_{coolingblock} = 5^{\circ}\text{C}$ (Water-alcohol cooling)
 $P_{sensor} = 1\text{Watt}$

$htc = 27.52\text{ W/m}^2\text{-K}$ | Air speed = 1 m/s
 Sensor thk. = 50 μm
 $T_{env} = -8^{\circ}\text{C}$ | $T_{cb} = 5^{\circ}\text{C}$
 $k_{bumps} = 6\text{ W/m-K}$ | $k_{contacts} = 3\text{ W/m-K}$
 Without TPG



$T_{max} = 20^{\circ}\text{C}$



DEPFET thermal for Belle-II, C. Marinas (IFIC-Valencia)

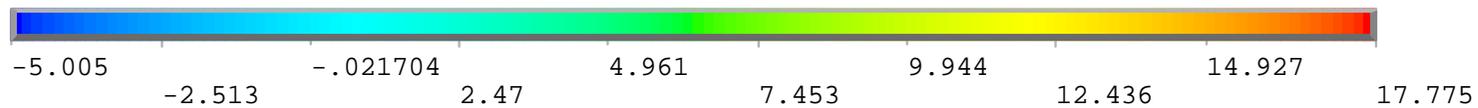
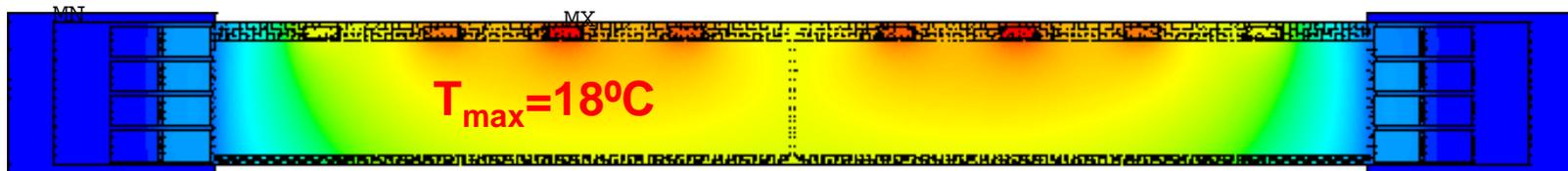
The center of the ladder is always cooled down by the air blowing

- Thermal studies: Up to date power consumption

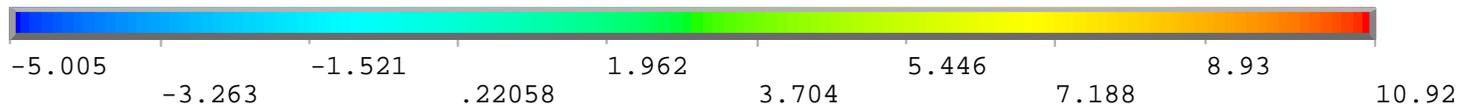
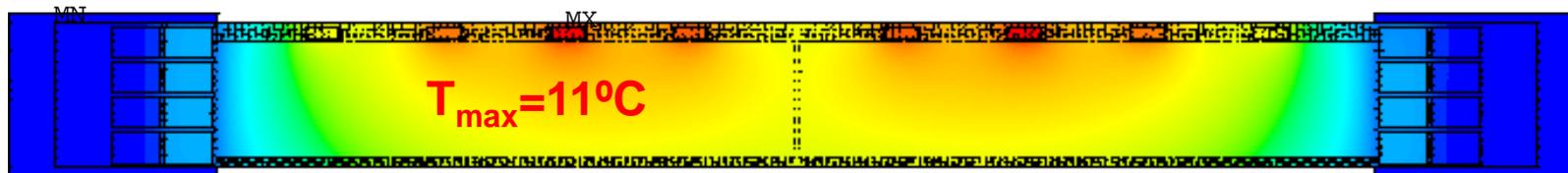


	P_{assumed} (W)	P_{updated} (W)
SW	1	0.7
Sensor	1	0.8 (1600 pixels)
DCD	12	10.08
DHP	4 (?)	4 (?)
Ladder	18	15.58
Full detector	360	311.6

$T_{\text{cb}} = -5^{\circ}\text{C}$
 $T_{\text{env}} = -10^{\circ}\text{C}$
 $V_{\text{air}} = 1\text{m/s}$



DEPFET thermal for Belle-II, C. Marinas (IFIC-Valencia)



- Evaporative cooling **without** cold-dry volume (Ideal)



$T_{env} = 15^{\circ}\text{C}$ (**Without** cold-dry volume)

$T_{coolingblock} = -25^{\circ}\text{C}$ (CO_2 cooling)

$P_{sensor} = 1\text{Watt}$

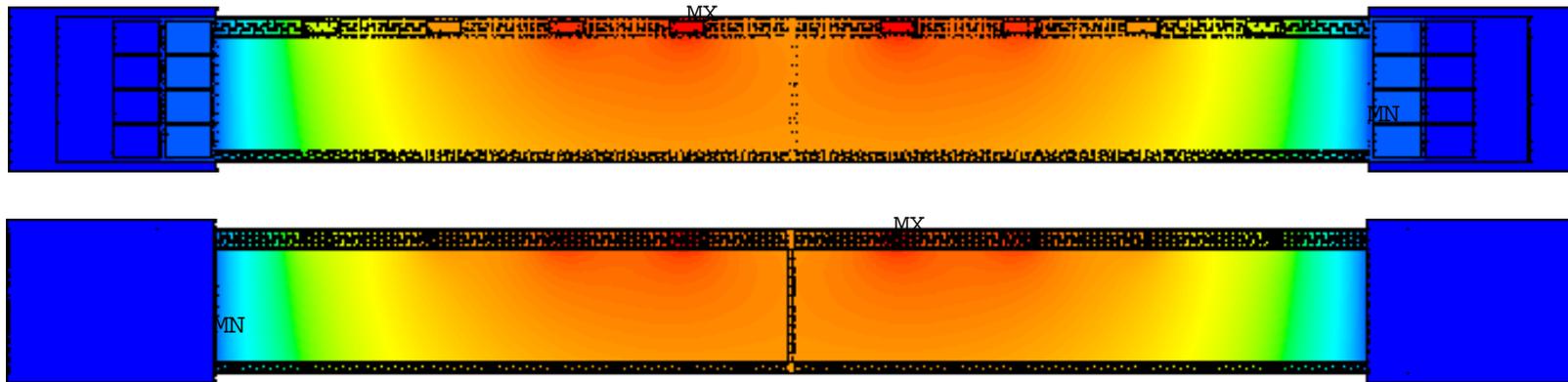
$htc = 27.52 \text{ W/m}^2\text{-K}$ | Air speed = 1 m/s

Sensor thk. = 50 μm

$T_{env} = 15^{\circ}\text{C}$ | $T_{cb} = -25^{\circ}\text{C}$

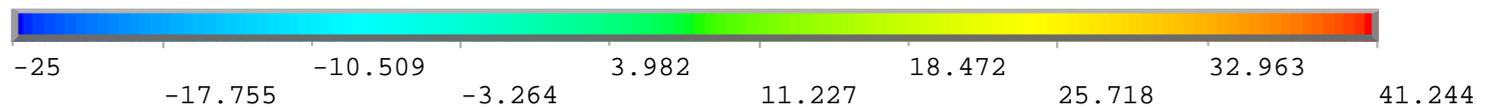
$k_{bumps} = 6 \text{ W/m-K}$ | $k_{contacts} = 3 \text{ W/m-K}$

Without TPG



$\Delta T_{Sensor} = 60^{\circ}\text{C}$

$T_{max} = 41^{\circ}\text{C} !!!$



DEPFET thermal for Belle-II, C. Marinas (IFIC-Valencia)

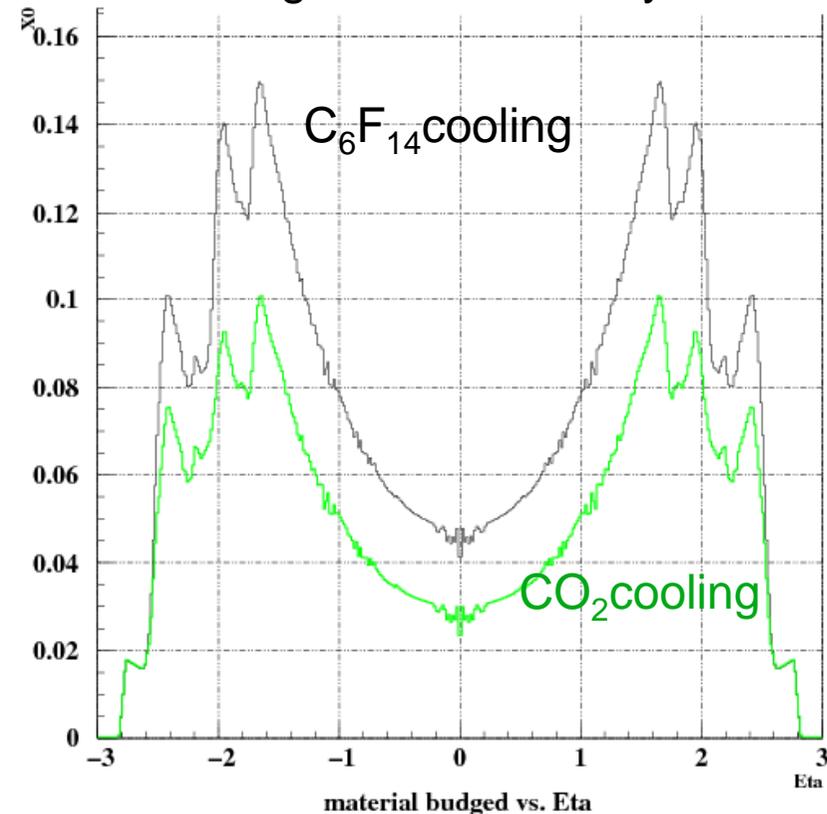
→ Even with CO_2 ... **the cold-dry volume with forced air is mandatory!!!**

- Evaporative cooling (CO_2 or C_3F_8)

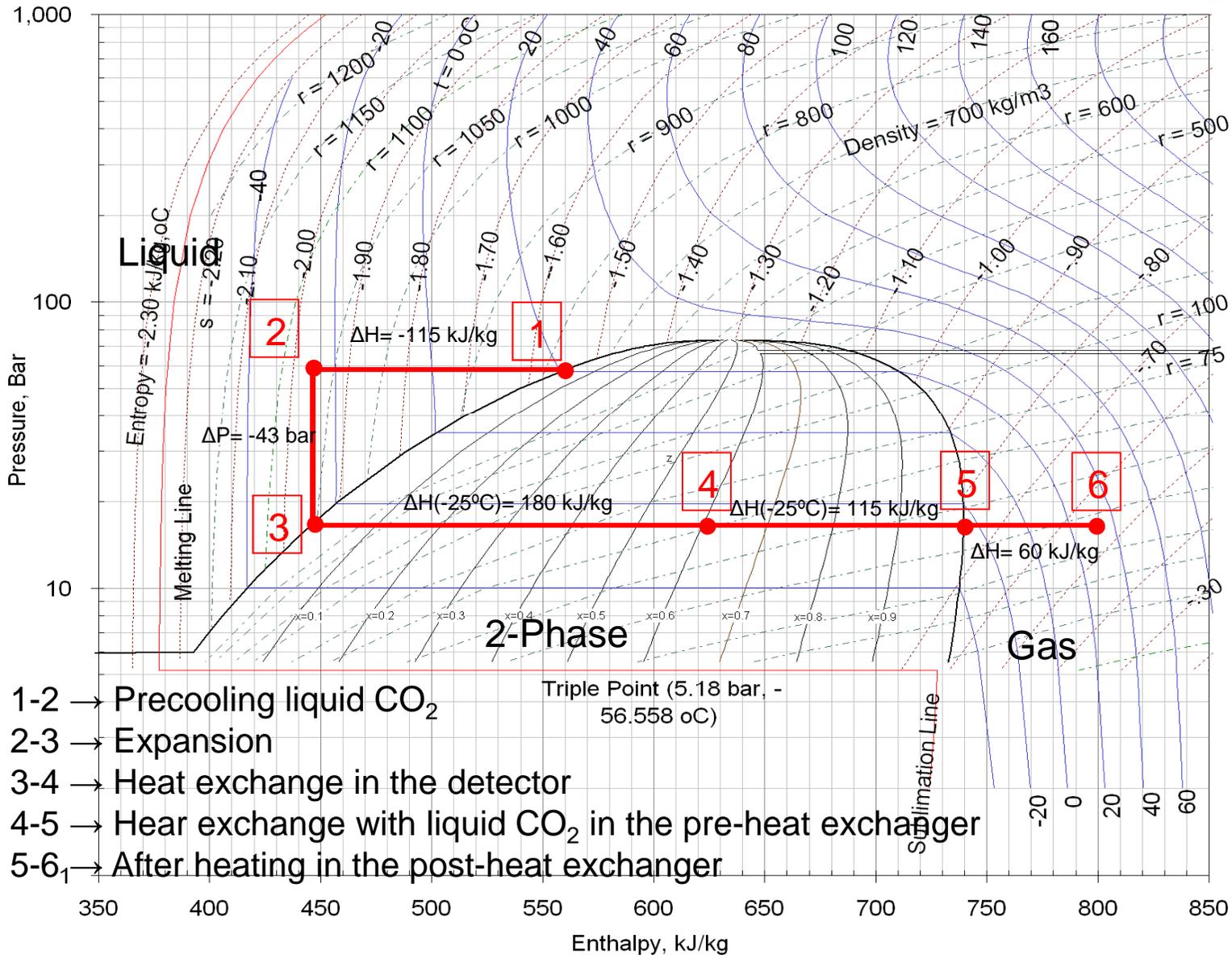


- Cooling loops (radius of 5mm) with very small pipes (outer radius ~1.3mm, wall thickness ~50 μm)
- The material budget is reduced (CO_2)
- LHCb, AMS, CMS, ATLAS, industry → Growing interest in this coolant (CO_2)
- C_3F_8 → Big experience
- Low mass flow needed
- No corrosion
- Bigger engineering studies are required
- High pressures

CMS Material distribution budget for 3 barrel layers



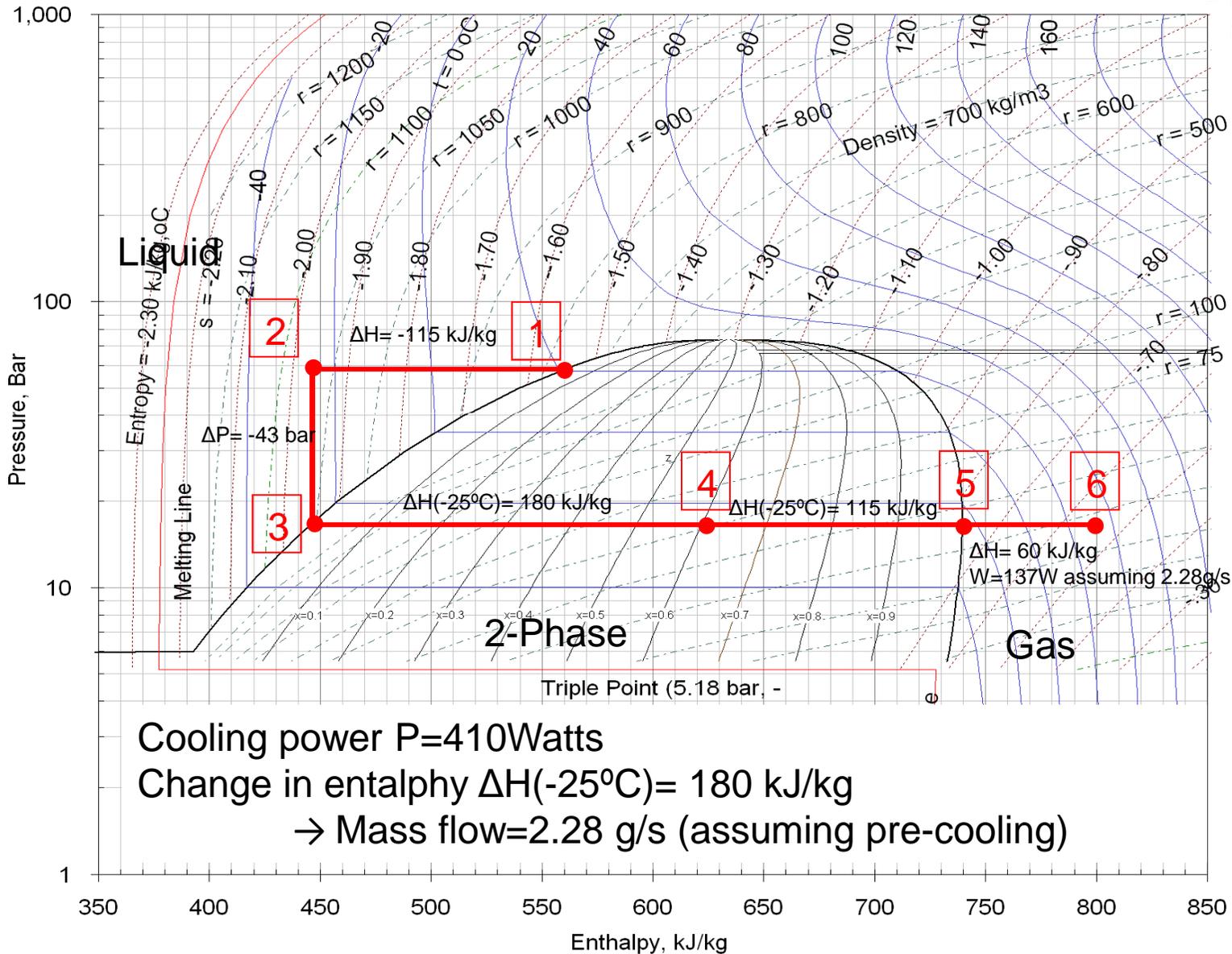
● Easiest CO₂ blow circuit (assuming post-heat exch.)



- 1-2 → Precooling liquid CO₂
- 2-3 → Expansion
- 3-4 → Heat exchange in the detector
- 4-5 → Heat exchange with liquid CO₂ in the pre-heat exchanger
- 5-6 → After heating in the post-heat exchanger



● Easiest CO₂ blow circuit (assuming post-heat exch.)

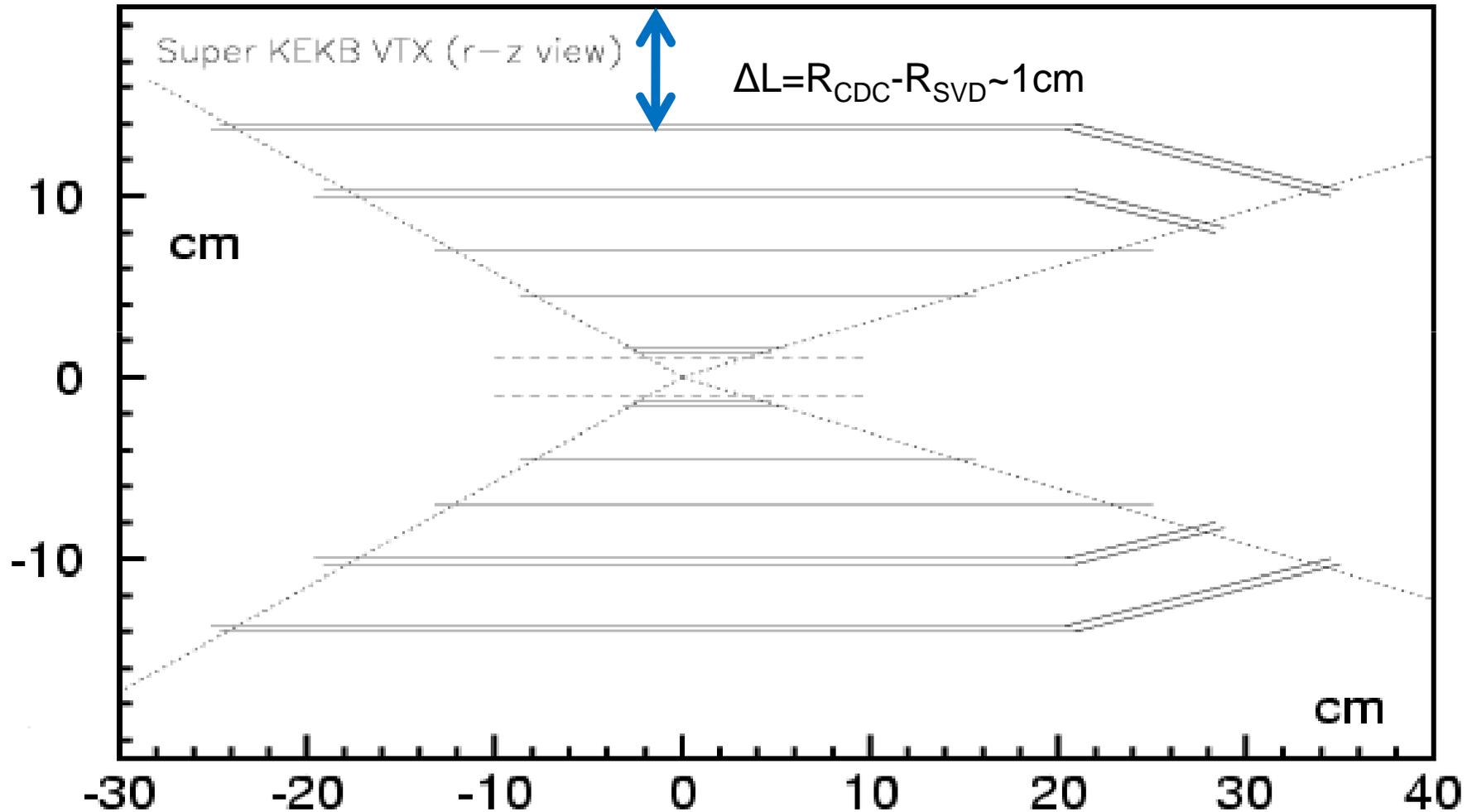


Cooling power $P = 410 \text{ Watts}$
 Change in enthalpy $\Delta H(-25^\circ\text{C}) = 180 \text{ kJ/kg}$
 → Mass flow = 2.28 g/s (assuming pre-cooling)

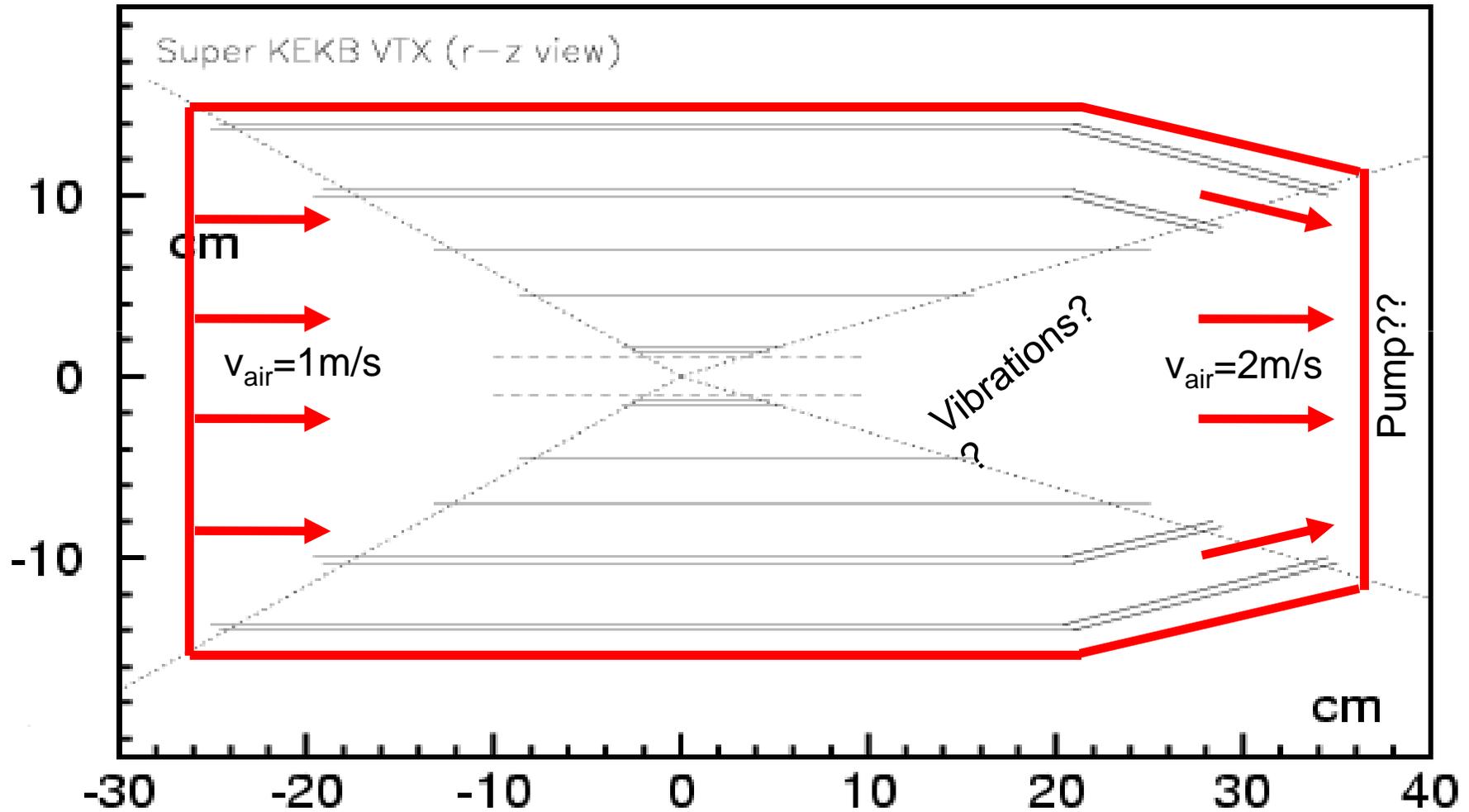
- Common cold dry volume



Very short distance! We need very nice insulation between detectors



- Common cold dry volume



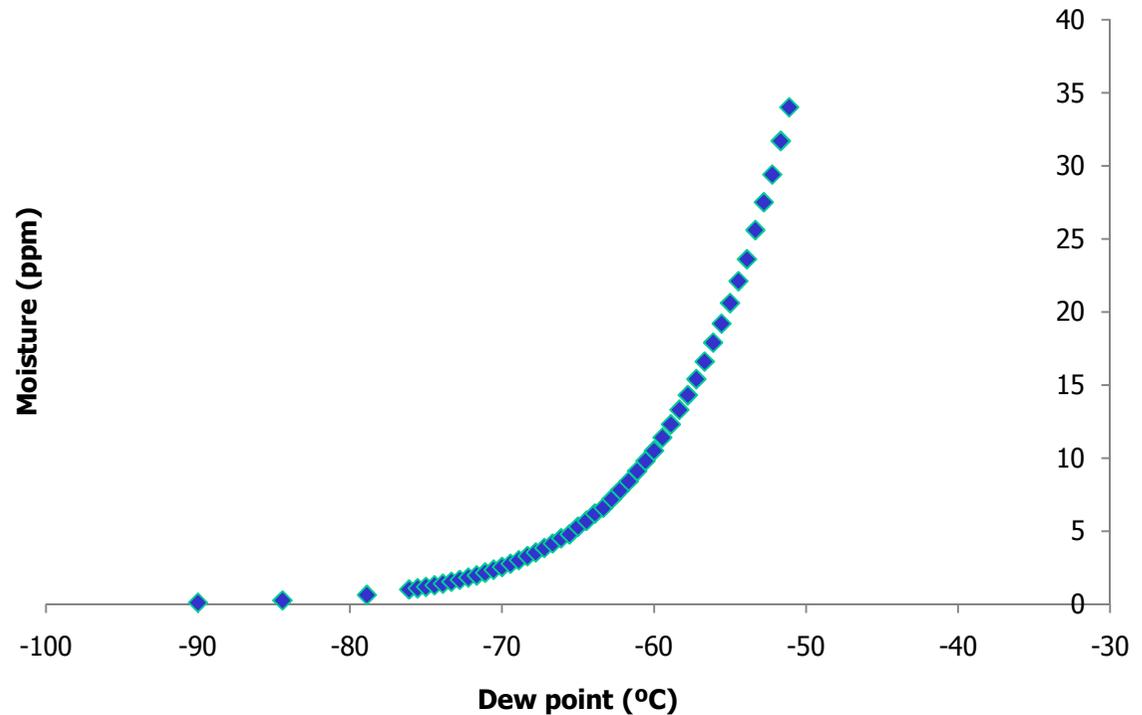
- Common cold dry volume



Assuming a sufficient margin for operation:

$$T_{\text{dewpoint}} < T_{\text{coolant}} - 15^{\circ}\text{C} = -40^{\circ}\text{C}$$

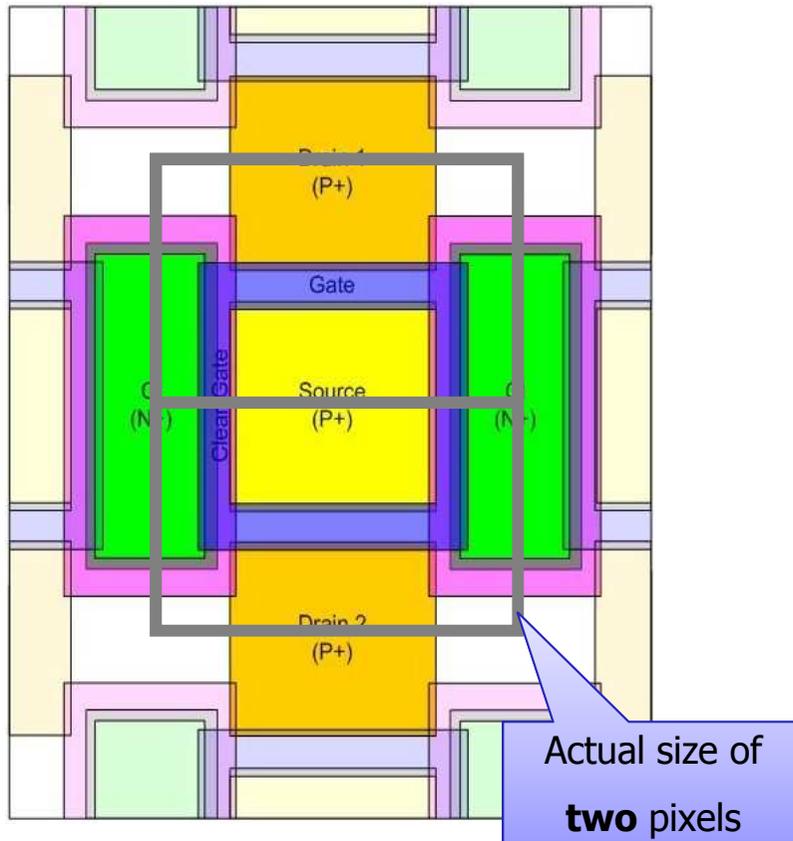
→ Moisture ~ 160ppm



Comparison:

- ATLAS → $T_{\text{dewpoint}} = -30^{\circ}\text{C}$; Moisture = 390ppm
- ATLAS upgrade → $T_{\text{dewpoint}} = -50^{\circ}\text{C}$; Moisture = 39ppm

- Double pixel structure



Merging two pixels (common source) for reduce the size

