The Belle-II Pixel Vertex Tracker at the SuperKEKB Flavour Factory

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Abstract

Building on the success of the current KEKB Flavour Factory and the Belle experiment, which helped to firmly establish the CKM picture of quark mixing and CP violation in the Standard Model, a luminosity upgrade of the asymmetric e^+e^- machine is planned. This new Super Flavour Factory, SuperKEKB, will deliver a luminosity of $8x10^{35}$ $cm^{-2}s^{-1}$, a factor 40 of increase over the present luminosity world record. It is foreseen to begin its operation in 2013. With these increased statistics, a new silicon vertex detector is needed in order to obtain precise decay vertex resolution measurements; these new precise measurements in the flavour sector can probe new physics well beyond the scales accessible to direct observations.

Key words: Belle-II, PXD, DEPFET, vertex detection, material budget, mechanical support, cooling

1. Introduction

The Belle detector has operated successfully during the last 10 years in the KEKB collider, a SuperB factory at the High Energy Accelerator Research Organization in Tsukuba, Japan. This machine is an asymmetric energy e^+e^- collider (3.5 and 8 GeV, respectively), running at the m(Υ(4S)) center-of-mass energy and it delivered the highest luminosity ever achieved in the world ($\mathcal{L}$=2.1 x $10^{34}cm^{-2}s^{-1}$). With these conditions an enormous number of $B\overline{B}$ pairs were created, allowing us to a better understanding of the CKM matrix elements or the CP violation of the B system in the Standard Model.

A KEKB upgrade plan was presented and the new Super Flavour Factory is foreseen to begin operation by the fall of 2013 [1]. An increase of luminosity by a factor of 40 will be achieved by an extreme reduction of the beam size at the interaction point (the so called *nano-beam* option). This new luminosity will result in a higher number of interactions and lead also to an increased occupancy and radiation doses, that will require the replacement of some parts of the detector in order to cope with these new conditions. A new vertex pixel detector for Belle-II is a key component of the upgrade, necessary to maximize the physics return of the increased machine's luminosity. Excellent vertexing is crucial for time dependent measurements of CP violation which requires the precise reconstruction of the decay vertices of B mesons. The new pixel vertex detector is designed to provide improved resolution compared to the present Belle detector while being able to handle the increased luminosity.

2. The Pixel Vertex Detector (PXD)

The Belle-II PXD group has decided on DEPFET (DEpleted P-channel Field Effect Transistor) active pixel technology [2] as baseline. Each DEPFET pixel is a field effect transistor (FET) integrated on a completely depleted bulk (Fig. 1). The full sensor thickness is depleted of charge carriers by applying a bias voltage. A deep *n*-implant under the FET channel acts as an internal gate. The collected signal modulates the current in the FET. Thus, a first stage amplification is achieved. After the drain current readout, all the accumulated charge can be removed by applying a positive voltage to a n^+-contact (called *clear*) placed on the periphery of each pixel. This structure provides particle detection and internal signal amplification while keeping low power consumption and material budget. The excellent performance of this sensors (high S/N ratio and intrin-

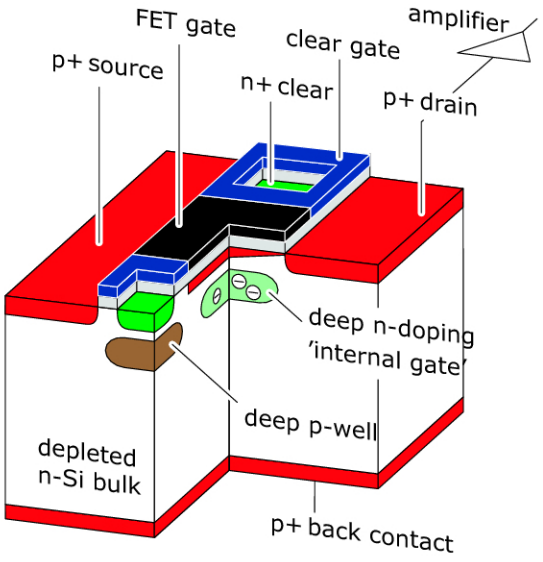

Figure 1: Schematic view of a DEPFET pixel structure.

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sic spatial resolution) has been demonstrated during several test beams developed during the past years [3].

2.1. PXD Layout

The Pixel Vertex Detector (PXD) is the innermost subsystem in Belle-II and consists of two cylindrical thin DEPFET pixel layers placed at a radius of 1.4 cm (inner layer) and 2.2 cm (outer layer). The inner layer uses 8 detector modules, or ladders, and the outer 12. The modules themselves are thinned down to a thickness of 50 μm in the active area, with 450 μm thick silicon rims to provide structural stability. A schematical 3D view of the full detector is shown in Fig. 2.

In order to extend over the full asymmetric angular acceptance of the detector, from 17° to 155°, the outer ladders will have an active length of 120 mm while the inner modules will have 80 mm. The outer ladders will be constructed from two silicon sensors joined in the center. Each ladder will have up to 1600x250 pixels with a size of approximately 75x50 μm in the outer layer and 50x50 μm in the inner layer. They are read out in a continuous rolling shutter mode with four rows being read in parallel on each side. This results in a readout time of 20 μs for a whole frame.

2.2. PXD Ladders

The Belle-II ladder parameters are not yet fixed and are subject to optimization. Properties like the sensor thickness, pixel size or inner/outer layer radius are being studied using full simulation. The simulation code is based on the ILC-framework (Mokka geometry and Marlin tracking packages [4]) and the ionization and signal points are created using a Geant4 based digitizer tuned with test beam data [5].

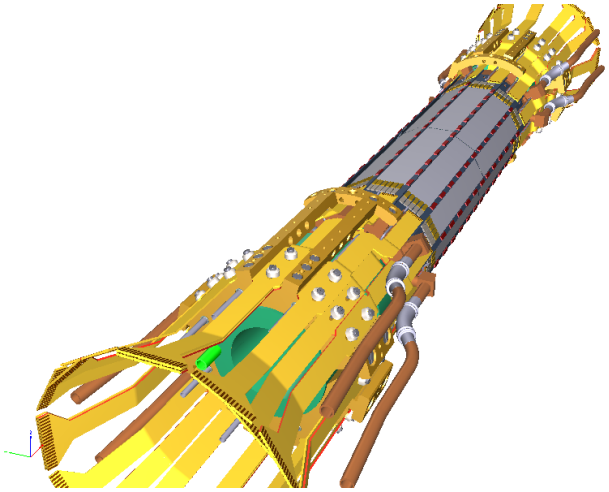

Figure 2: 3D illustration of the full Belle-II Pixel detector (PXD) mechanical design, including the support structures on the beam pipe (green part) and the Kapton cables.

3. The PXD electronics

As already mentioned, each ladder is readout at both sides. The proposed structure for the Belle-II PXD half ladder is shown in Fig. 3. The sensitive area (along the vertical red dash-dotted line in the picture) is thinned down to 50 μm, to minimize the multiple-scattering effects, and is surrounded by a thicker silicon rim that provides the module with the required stiffness and structural stability. This thinning procedure has already shown good results in many other applications [6]. The front end ASICs are mounted on the thicker silicon frame. From Fig. 3 we see on the *balcony* at the side the steering chips (called Gate and Clear SWITCHERs), used to switch on the pixel rows and to clear the data on the internal gates of the pixels. The readout ASICs (DCD and DHP) are located on both ends of the ladder. All the chips will be directly bump bonded to the ladder by using solder balls.

3.1. Data Flow

The full data flow is as follows: the drain current is digitized using the DCD (Drain Current Digitizer) in the first step and then zero-suppression, common mode correction and pedestal substraction operations are performed on the DHP (Data Handling Processor). The data is then sent via a multi-layer Kapton cable to the DHH (Data Handling Hybrid) and from here to the ATCA-based DAQ system (Advanced Telecommunications Computing Architecture) using optical links. In order to reduce the data to be stored in the Event Builder Farm, the silicon microstrip tracker, SVD (Silicon Vertex Detector), information is used to find regions of interest (ROI) in the PXD ladders by extrapolating back the tracks found in the tracker detector. Only the data extracted from the pixels that lay in this regions will be considered to be saved in the farm. Assuming an occupancy of 1%, the data flow from the 8 Mpixel PXD is expected to be 9.6 GB/s.

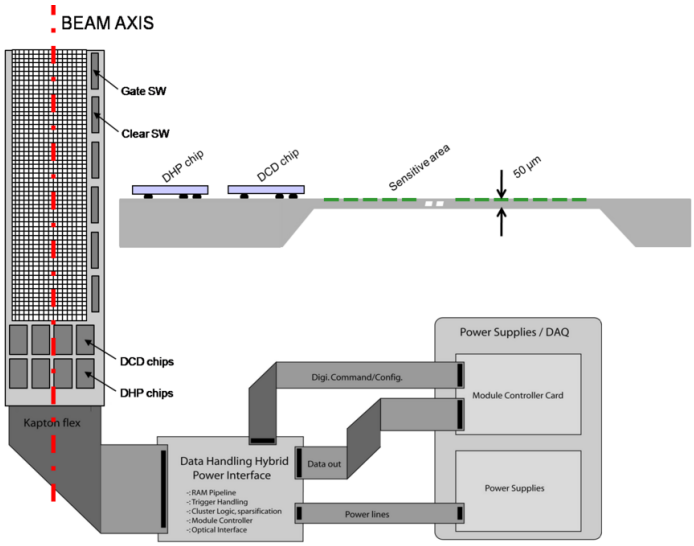

Figure 3: Schematic view of the full readout system. A longitudinal cut view along the beam axis is also shown: the sensitive area will be thinned down to 50 μm while keeping a thick frame to provide mechanical stability to the whole. The ASICS will be bump bonded to the ladder.

4. Integrated Support and Cooling Structure (ISCS)

Given the low momentum of the tracks, multiple-scattering is an issue with severe implications on the material budget. This is particularly true for the cooling system where no active cooling (pipes) along the ladders are allowed. Simulations and measurements have shown that the readout chips must be cooled by conduction through the support, which should cover all the area available underneath the end of stave to minimize the thermal path. The cooling of the center of the ladder, on the contrary, must rely on convection and a cold, dry air flow is needed. Fig. 4 shows the current baseline for the end-flange, or ladder support structure. It will have built-in micro-channels for the coolant and will, therefore, act both as a mechanical support and cooling contact for the detector. The chosen material structure is copper[2], because of its high thermal conductivity and optimal CTE coefficient. This structure, mounted on a support fixed to the beam pipe mask, has, together with the integrated cooling channel, through-going holes to blow air in between the two detector layers.

Both mono-phase and bi-phase cooling systems are studied [7]. The former has the advantage of a simple design and lower operation pressure. The latter allows for smaller pipe diameter and connector size, lower mass flows, but the design has to cope with a pressure of up to 70 bar.

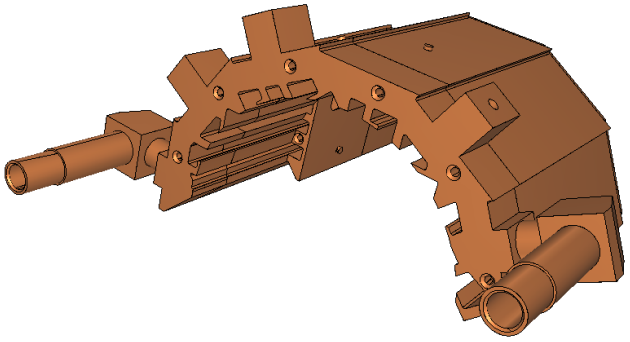

Figure 4: Integrated Support and Cooling Structure (ISCS) A 'two in one' solution for cooling and mechanical support at a time.

5. Thermal performance

As a result of a detailed study of temperature effects on the components and system performance it became clear that the sensors should not exceed a temperature of 30^{o}C to keep the leakage current under control and that the ASICs had to operate below 60^{o}C to prevent electromigration. The collaboration has conducted a set of in-depth, detailed FEA simulations to determine the thermal behaviour of the PXD ladders. The simulations included the real module geometry, with a level of detail that considered both the etching under the lateral balconies as well as the joint between the two half ladders on the outer layer.

[2]in case of a bi-phase cooling system (like CO_2) stainless steel will be used instead

The input for the thermal loads came from predictions on the estimated power consumption of the ASICs. The thermal properties of the different components were obtained from laboratory measurements on real thermal mock-ups which included also the effect of bump bonding on the thermal resistance between the ASICs and the support. Heat transfer by radiation between the two layers has not yet been included in the simulations.

Fig. 5 shows the estimated power dissipation on each element of a second layer ladder. Since the matrix is readout in a continuous mode, the main contribution comes from the readout chips (2 W for the four DHP and 6 W for the four DCD, sitting on each half ladder).

Only the active pixels in the DEPFET matrix consume power, which amounts to 1 W for the 8 rows readout in each cycle (4 on each half). However, we did not perform any transient simulation and a uniform power consumption of 1 W was assumed to be homogeneously distributed on the whole active area. Finally, the steering chips contribute moderately with 0.5 W for each half. Again, this is an averaged value since the actual load varies with time according to the readout cycle. Adding up, each of the PXD ladders, contribute with 18 W, giving a total of 360 W for the whole pixel detector (20 ladders).

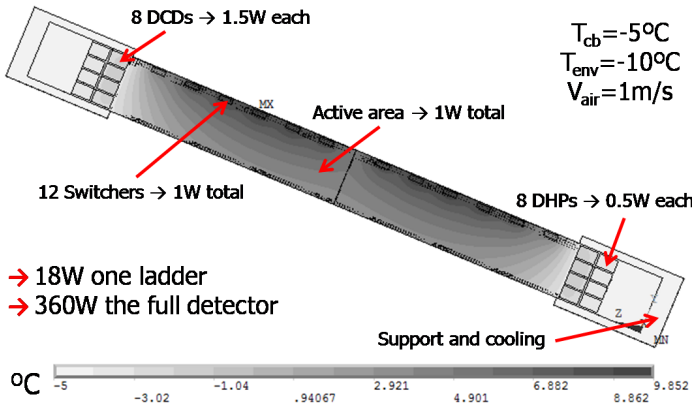

Figure 5: Parameters for the thermal simulation studies. The color code shows the temperature distribution along the ladder as a result from a FEA simulation with a set of reasonable boundary conditions.

Fig. 5 also shows the expected temperature distribution over a Belle-II PDX ladder on the outer layer with a typical set of environmental temperatures. The temperature drop between the coolant and the ladder support in the end-flange was measured to be 20^{o}C. Assuming a coolant temperature of -25^{o}C, the temperature at the ladder support surface will be -5^{o}C, as used in the simulation. To reach the required temperature on the sensor, the center of the ladder has to be chilled by forced convection with very cold air (-10^{o}C and 1m/s). Both simulations and measurements have shown that the temperature in the center of the sensor is proportional to the air temperature. Ambient temperature air blow would result in a sensor temperature of ~40^{o}C, out of the tolerable limits. A more complicated engineering solution is needed and, even, a cold dry envelope encompassing both the SVD and the PSD detectors is under study.

6. Conclusions

An upgrade of the existing Belle detector is ongoing to cope with the new challenging requirements arising from the factor 40 increased luminosity, compared to Belle, that the new SuperKEKB factory will provide. The PXD detector will be based on DEPFET technology because of its high gain, low material budget and good spatial resolution. The full set of the detector parameters are being optimized using single tracks and physics events together with detailed FEA simulations. A mechanical and cooling solution is under study.

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