Detector performance of the ALICE Silicon Pixel Detector

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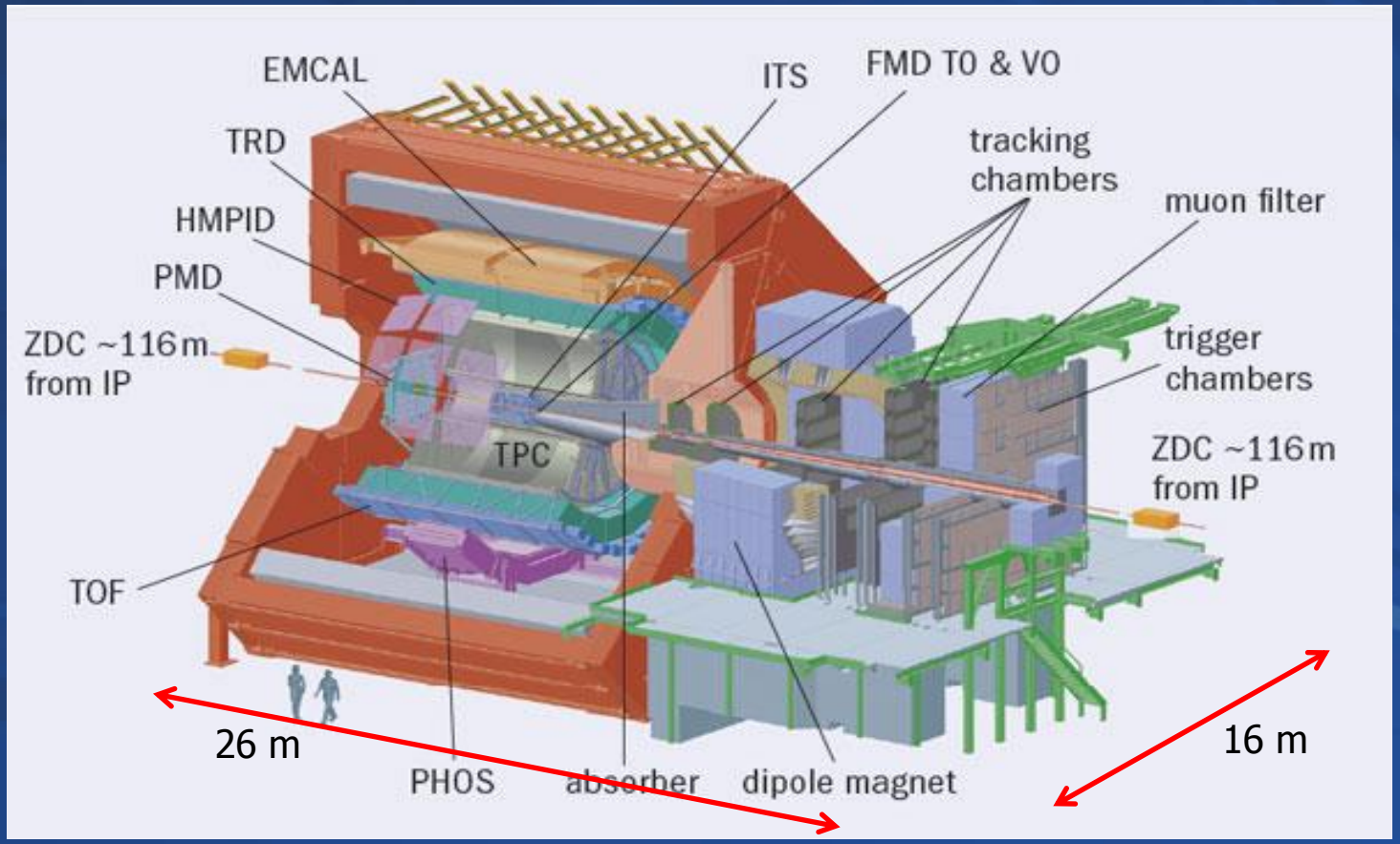
CERN – European Organization for Nuclear Research
on behalf of the SPD project in the ALICE Experiment

ALICE layout

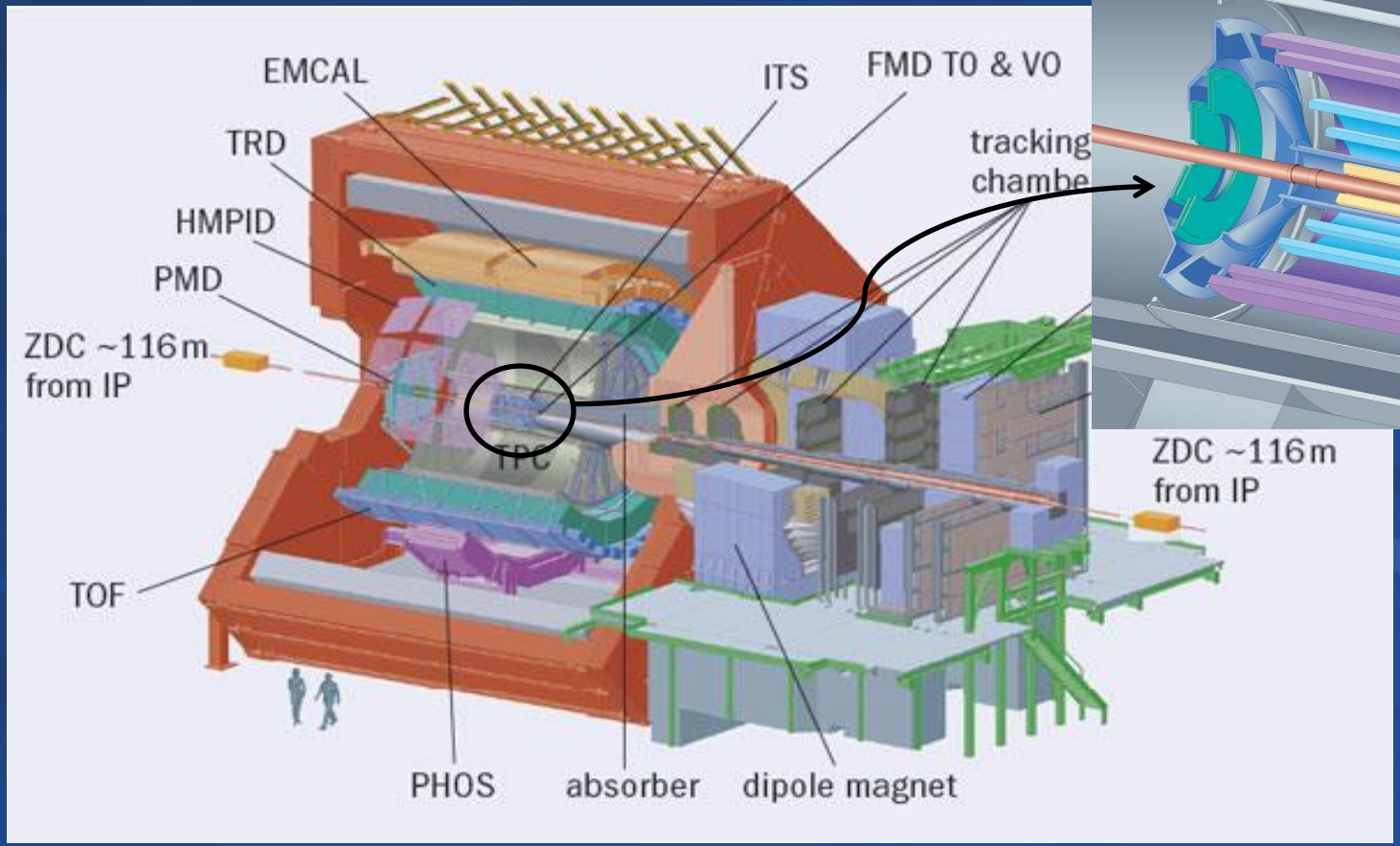
Experiment designed for heavy ion collisions (Pb-Pb @ 2.75+2.75 TeV per nucleon)

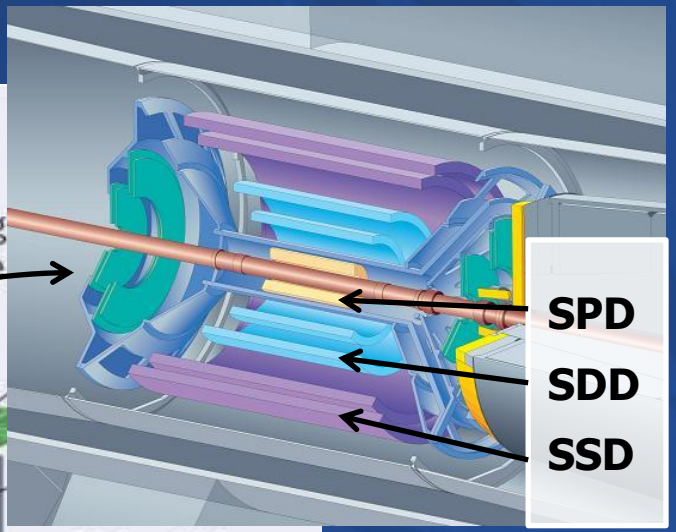
- nucleus-nucleus collisions: study strongly interacting matter
- p-p collisions: reference data for heavy ion program, unique physics



ALICE Inner Tracking System

- 3 different silicon detector technologies in 6 barrel layers
- from interaction point Pixels (SPD), Drift (SDD), double side Strips (SSD)





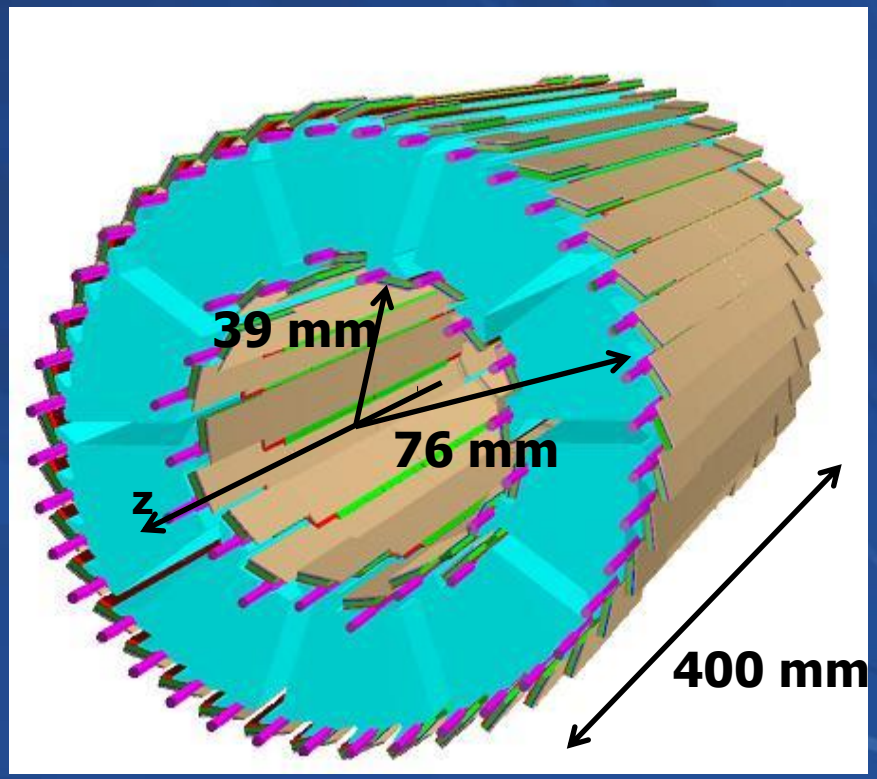
ALICE Silicon Pixel Detector

REQUIREMENTS

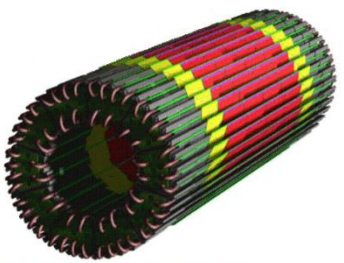
- 2D digital readout (256 μs, no ambiguity)
- high efficiency (> 99%)
- high spatial precision (~12 μm in the bending plane)
- limited material budget (~1% X_0 per layer)
- fast signal for L0 trigger

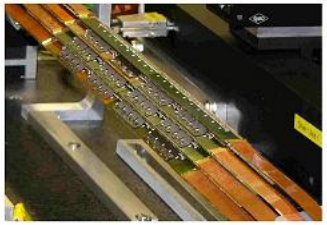
CHARACTERISTICS

- 2 innermost layers, 0.24 m^2
- ~ 9.8 M readout channels
- pixel size 425 x 50 μm^2 (z x rφ)
- sensor thickness 200 μm
- readout chip 0.25 μm CMOS technology
- power consumption ~ 1.35 kW
- internal clock 10 MHz



ALICE Silicon Pixel Detector

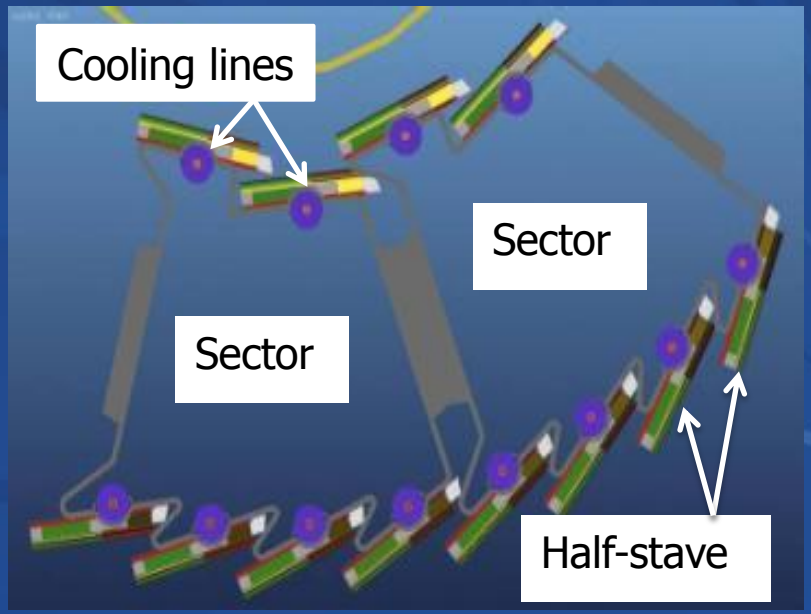




		Total SPD components
SPD	→ 10 sectors	10 sectors
Sector	→ 12 half-staves	120 half-staves
Half-stave	→ 1 multilayer bus	120 multilayer bus
	→ 1 MCM	120 MCM
	→ 2 ladders	240 ladders
Ladder	→ 1 sensor	240 sensors
	→ 5 readout chips	1200 chips
Readout chip	→ 8192 pixels	~ 9.8 x 10^6 pixels

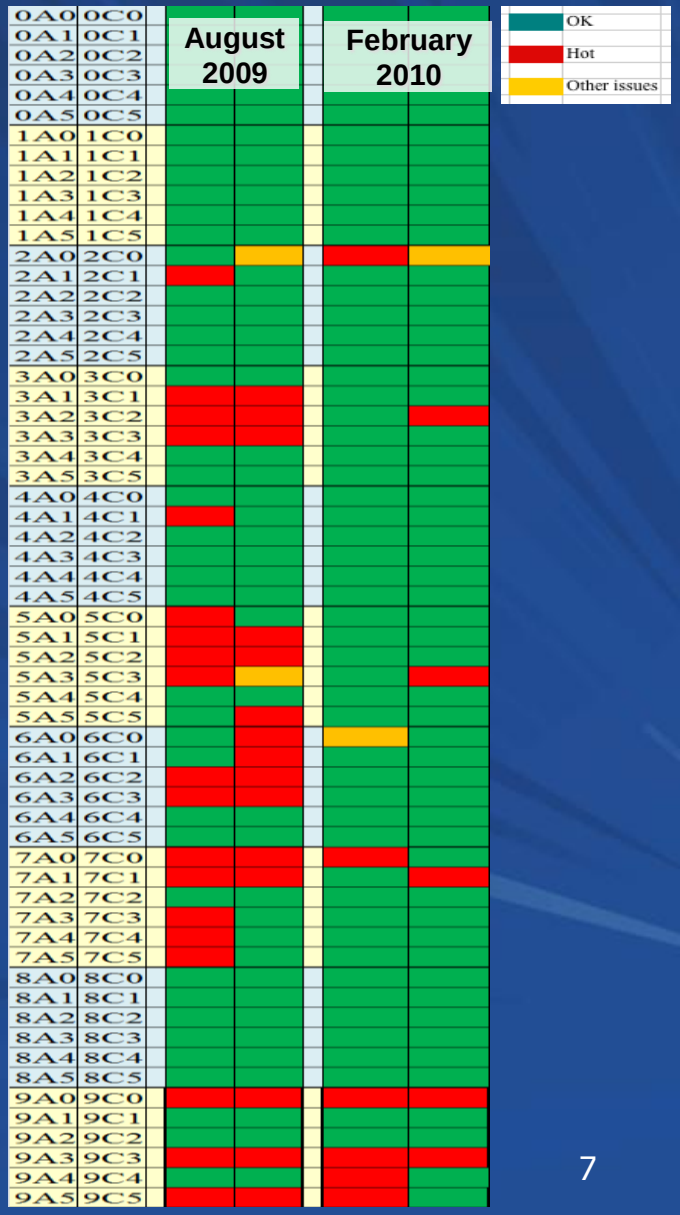
SPD cooling system

- evaporative system with C_4F_{10}
- capillaries under each half-stave, embedded in the carbon fiber support
- monitoring of T-p at the plant and up/downstream the detector
- monitoring of flow per line
- control of liquid pressure per line
- without cooling the SPD temperature would increase ~1°C/s



SPD cooling system

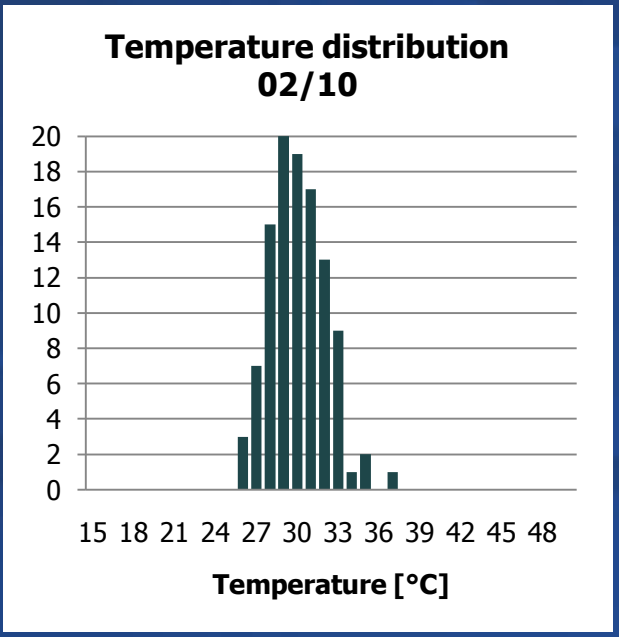
- commissioning started end 2007
- situation in 2009 after the long shut-down: ~30% off
- actions taken:
  - counter-flow-wise cleaning
  - new input lines
  - more T/p monitors
  - flow gauges
  - per-line liquid pressure control
- after the interventions 88% efficiency
- 107/120 modules on, stability test

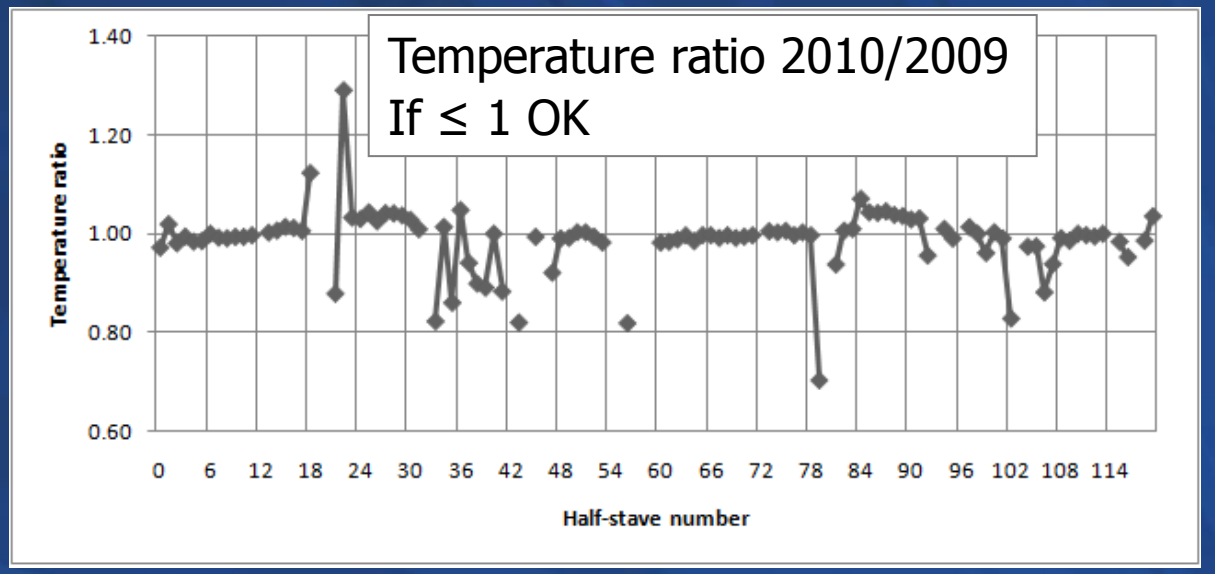


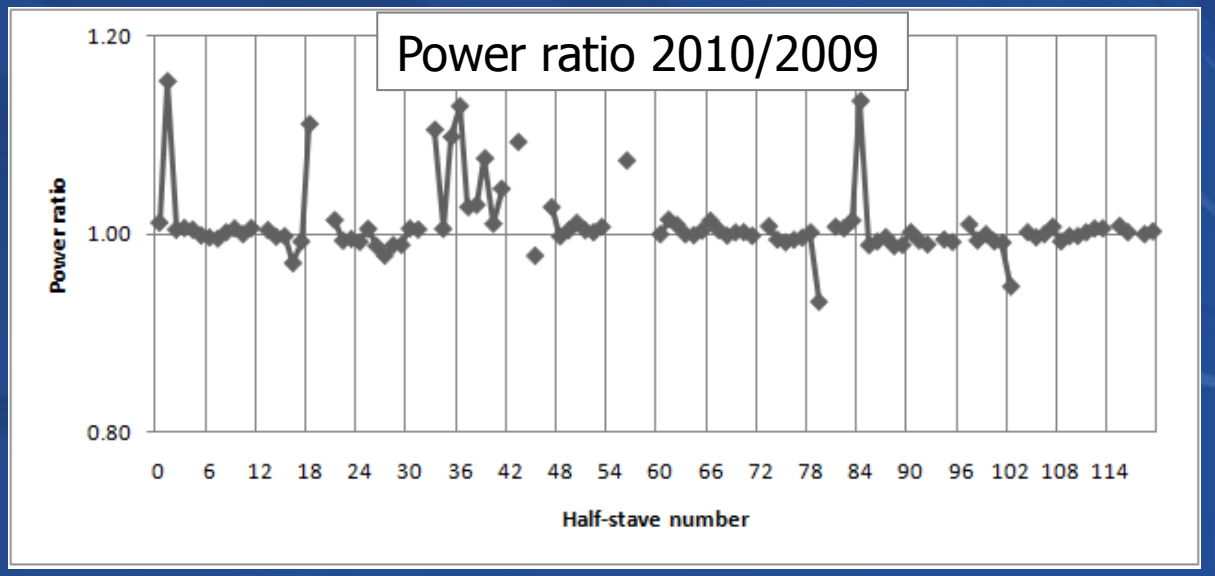
SPD cooling system

Improvements observed after the tuning of the cooling system

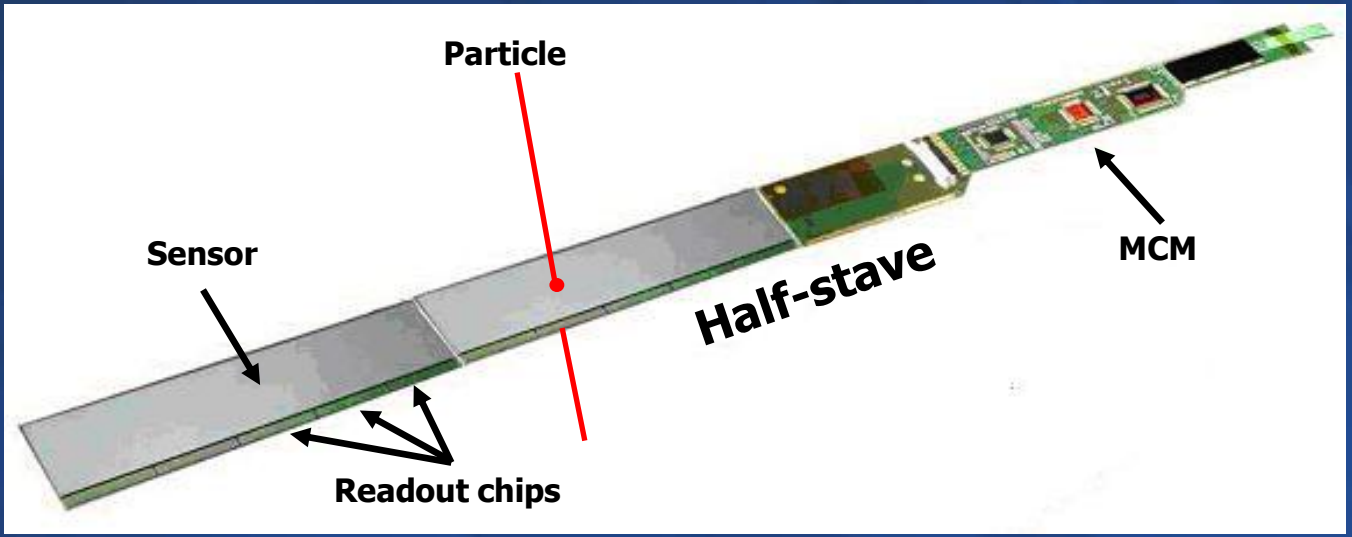
Avg. temperature: 29.4 °C





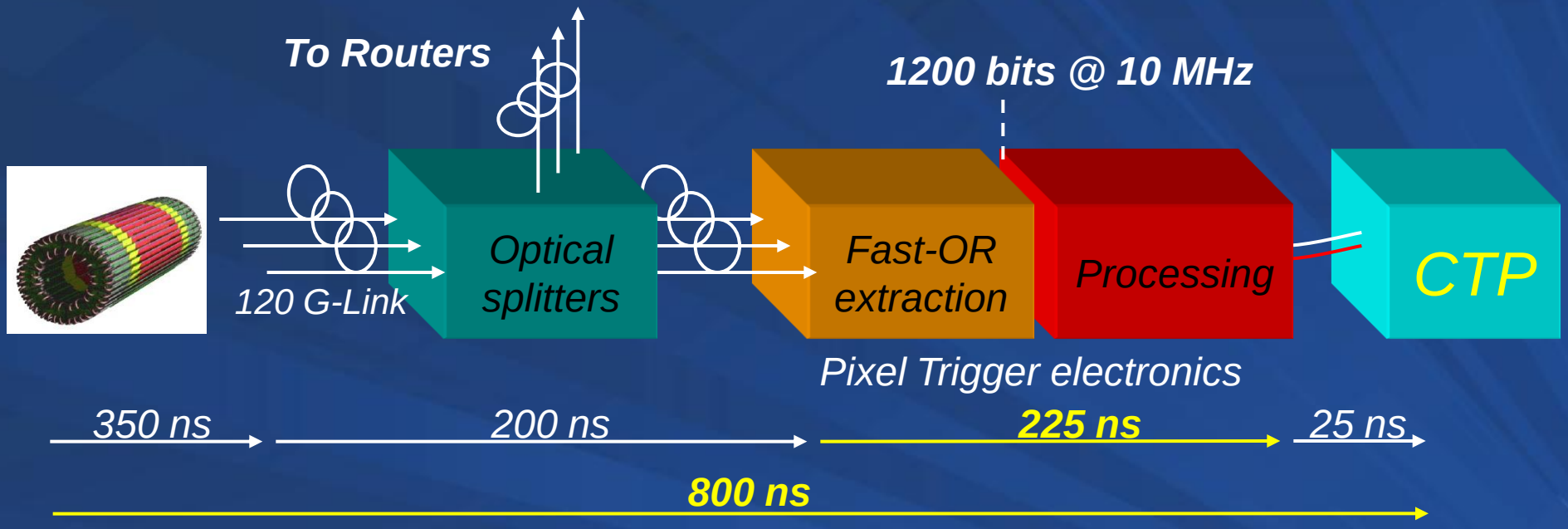


Fast-OR trigger signal



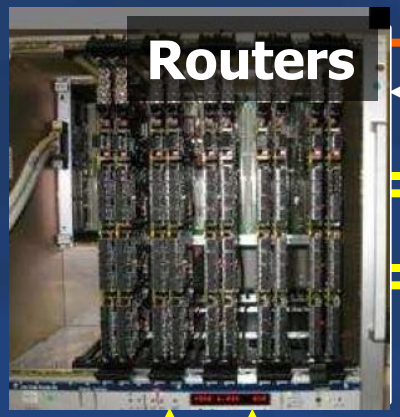
- Fast-OR active on registration of at least 1 pixel hit per readout chip
- 10 chip/half-stave => 1200 Fast-OR bits every 100 ns transmitted on the optical data link to the readout electronics
- first level of trigger in ALICE (L0)
  - unique feature among the vertex detectors of LHC experiments
  - low latency pad detectors (13 x 14 mm^2)

Pixel Trigger system



- Maximum latency = 800 ns => installed at 40 m from SPD
- Deserialization of data and Fast-OR bits extraction
  - Board with optical receivers and FPGA (OPTIN board)
- Processing of the Fast-OR bits
  - Board with large FPGA (BRAIN board)
  - Up to 10 algorithms executed at the same time (processing time = 25 ns!)

Pixel Trigger integration



DAQ connection

DAQ

Clock & Serial (A & C sides)

60

60

G-link

60

60

SPD

TTC connection [Timing, Trigger & Control]

Optical splitters

60

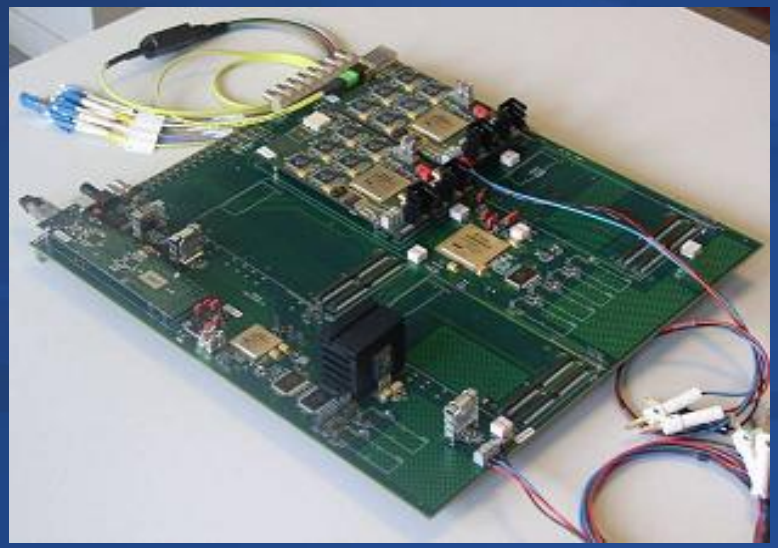
60

10

Central Trigger Processor [CTP]

Pixel Trigger characteristics

- based on boolean functions (AND/OR) of the 1200 FO bits
- minimum bias + multiplicity trigger for p-p collisions
- centrality trigger for Pb-Pb collisions
- programmable thresholds on inner/outer layers
- algorithm flexibility: FW programmable from remote at start of run

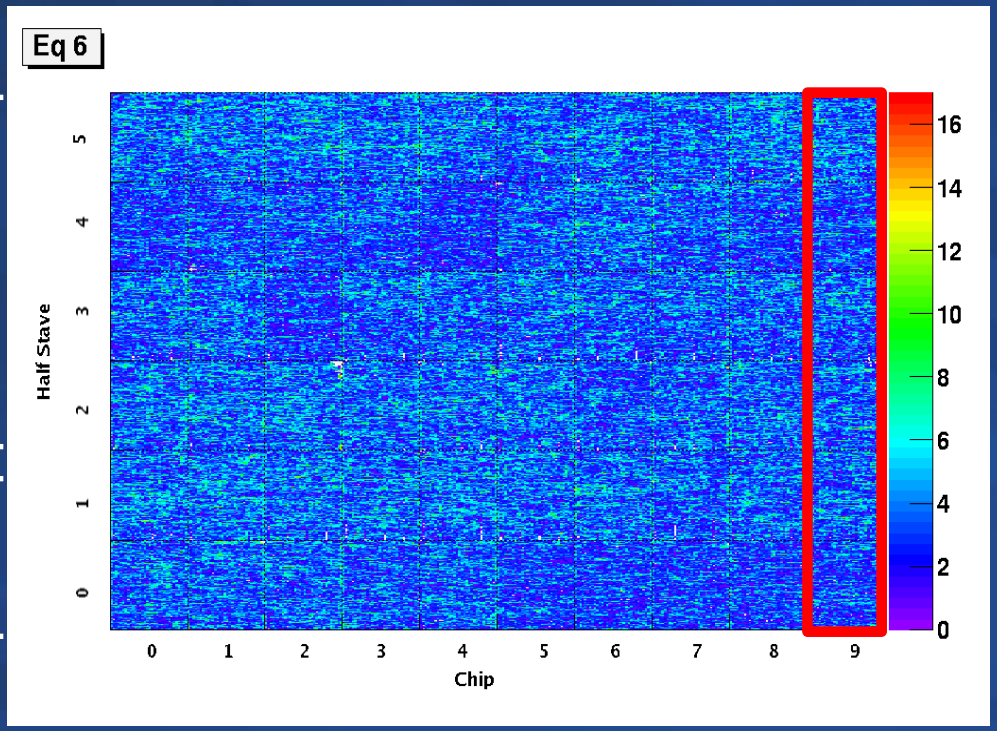


Output	Algorithm
1	Minimum Bias
2	High Multiplicity 1
3	High Multiplicity 2
4	High Multiplicity 3
5	High Multiplicity 4
6	Past Future Prot
7	Background(0)
8	Background(1)
9	Background(2)
10	Cosmic

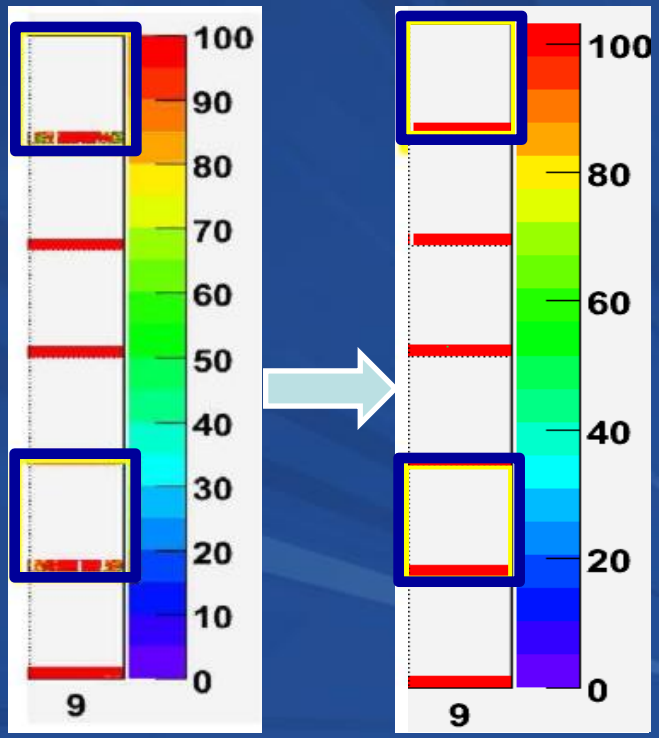
SPD calibration

Uniformity response of chip matrix

- checked with internal pulser of known amplitude to detect noisy/inefficient regions
- injection tests and cosmic data accumulated for cross checking



Matrix response from 6 half-staves (real data from injections)



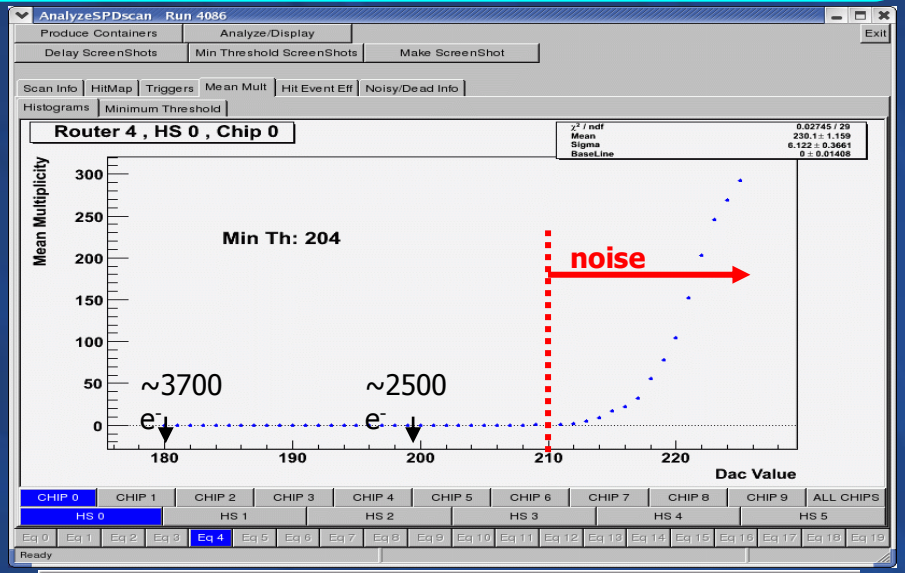
Chip 9 uniformity improved after tuning (test pulse)

SPD calibration

Minimum threshold scan

finds the lowest threshold value at which the chip can be operated without noise

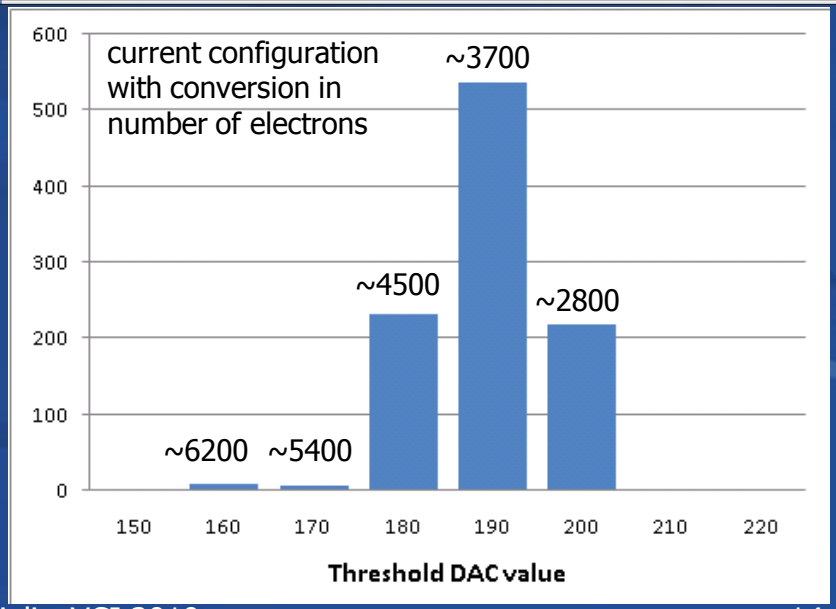
- scans trough threshold values
- finds the closest to the noise area
- applies a safety margin



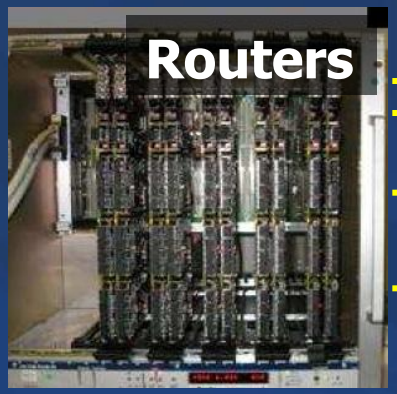
Mean threshold scan

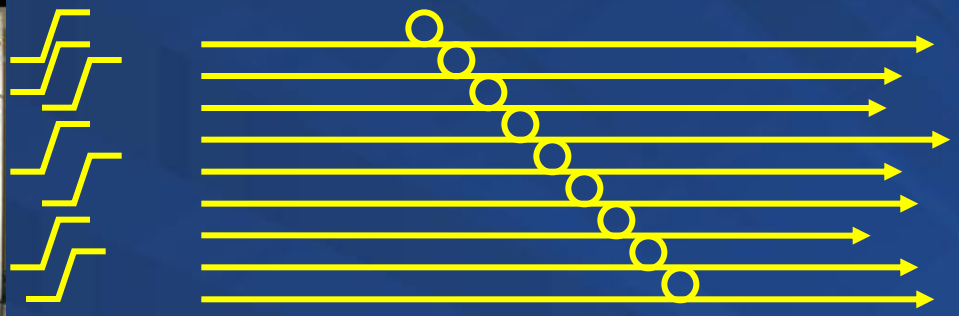
finds the conversion factor between charge deposited on the detector and corresponding DAC value

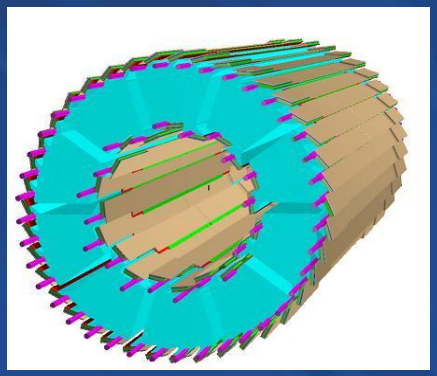
- scans through different amplitudes of internal pulser
- determines an S-curve per pixel
- calculates the mean value per chip



Time alignment of SPD clock phases







Clk outputs **Clk fibers (~100m)**

Alignment of the internal phases of the SPD clock at 10 MHz

Relative phases of 120 clocks of control units: σ = 0.63 ns
Propagation delays due to 120 optical fibers: σ = 0.90 ns

Clock phases at SPD inputs without correction: σ = 1.10 ns

Individual delays added to the clock transmitters to compensate differences
Clock phases at SPD inputs with correction: σ = 0.08 ns

Fast-OR circuit calibration

Required tuning of 5 DACs for every of the 1200 readout chips to

- maximize efficiency
- minimize noise

Automatic calibration procedure implemented

- verifies Fast-OR efficiency in different operating conditions using internal pulser
- scans the DAC values (compref, convpol, fopol, prevth)
- checks the signal rates
- coordinates SPD readout, control system and Pixel Trigger operation

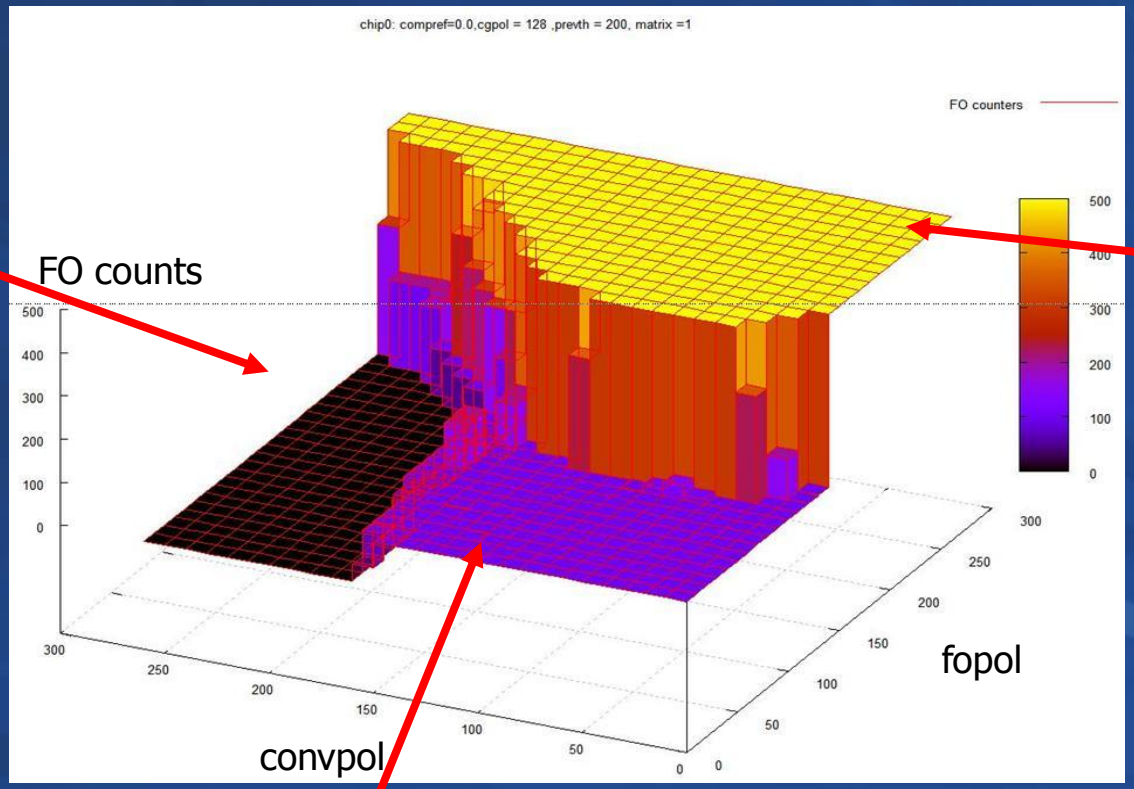
- developed after manual experience to limit the parameter space
- manual vs. automatic procedure: ~600 man-hours vs. 2-4 hours
- efficiency condition on Fast-OR signal: 100%

Fast-OR calibration results

3 DACs are kept fixed, 2 are scanned, the Fast-OR pulses are counted for each value combination

Example: HS025, chip 0, central pixel - COMPREF = 0, Pre-VTH = 200

Inefficiency
--
counts = 0



Noise
--
counts > 500

OK -- region of 100% efficiency
FO counts = # triggers sent= 100

Cosmic data

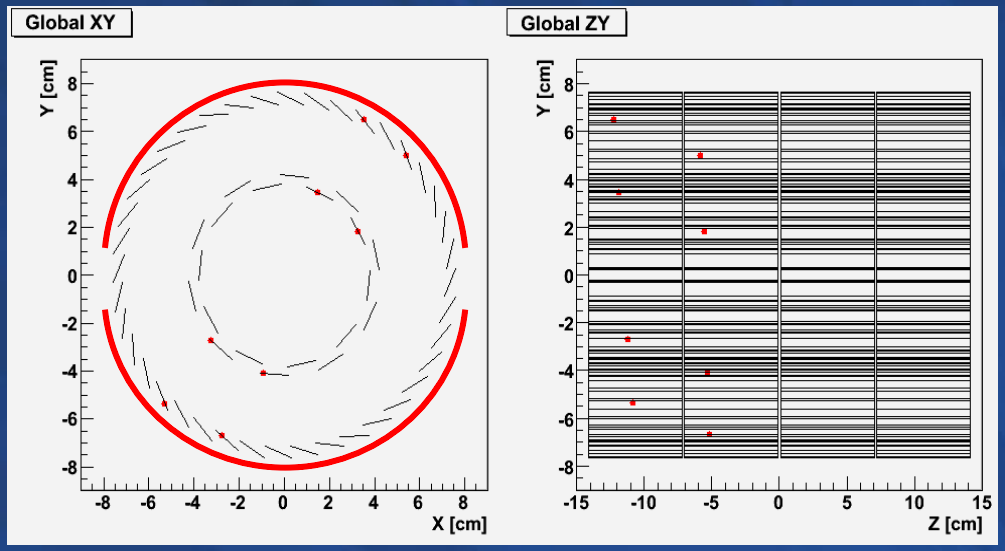
Pixel Trigger used as L0 trigger during ALICE commissioning with cosmic data

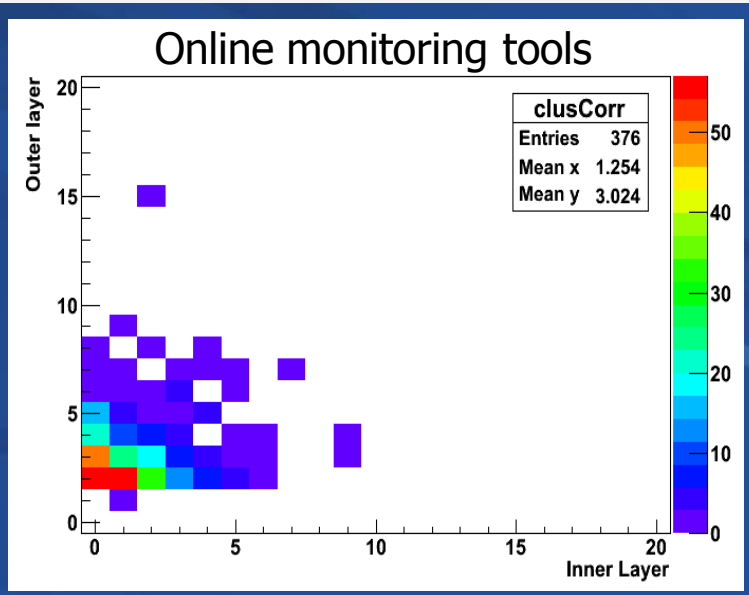
Coincidence algorithm: top/bottom outer layer

Data used for alignment: 10k events with more than 3 clusters on SPD

Rate: 0.12 Hz in agreement with measured flux in the cavern and Monte Carlo simulations

99.6% of events with correct cluster distribution





Cosmic data - alignment

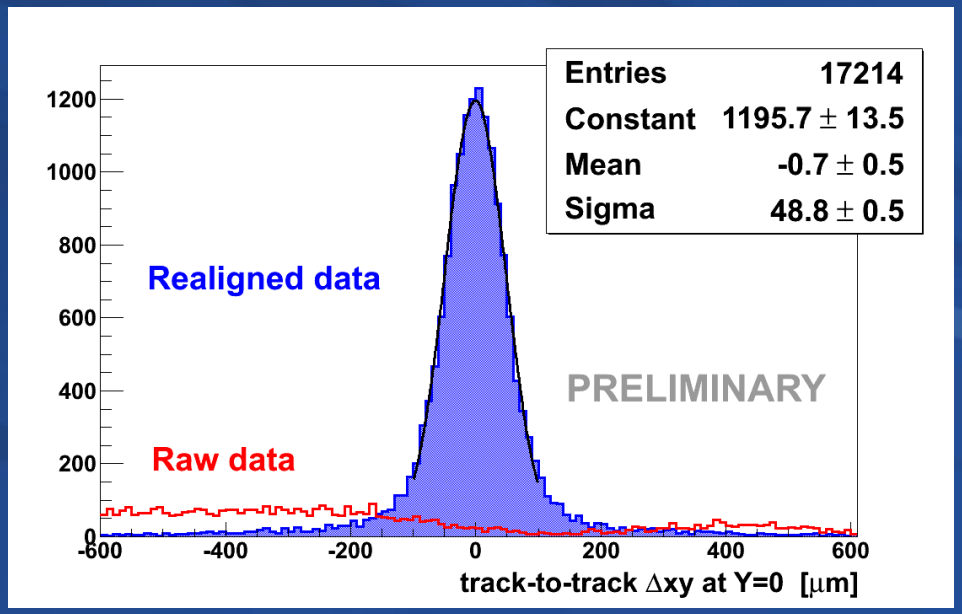
Preliminary results after cosmic runs in summer 2009

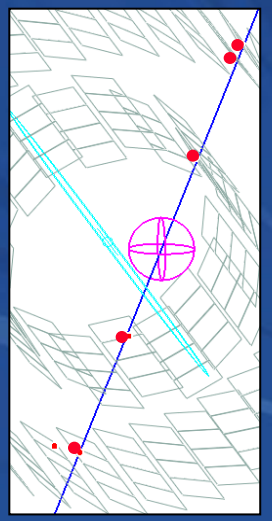
Two track-based methods to extract the alignment parameters (traslations + rotations):

- global minimization with Millipede (default)
- iterative approach module by module

SPD hierarchic approach: barrels -> 10 sectors -> 120 half-staves -> 240 sensors

Track-to-track (top vs bottom) distance in transverse plane



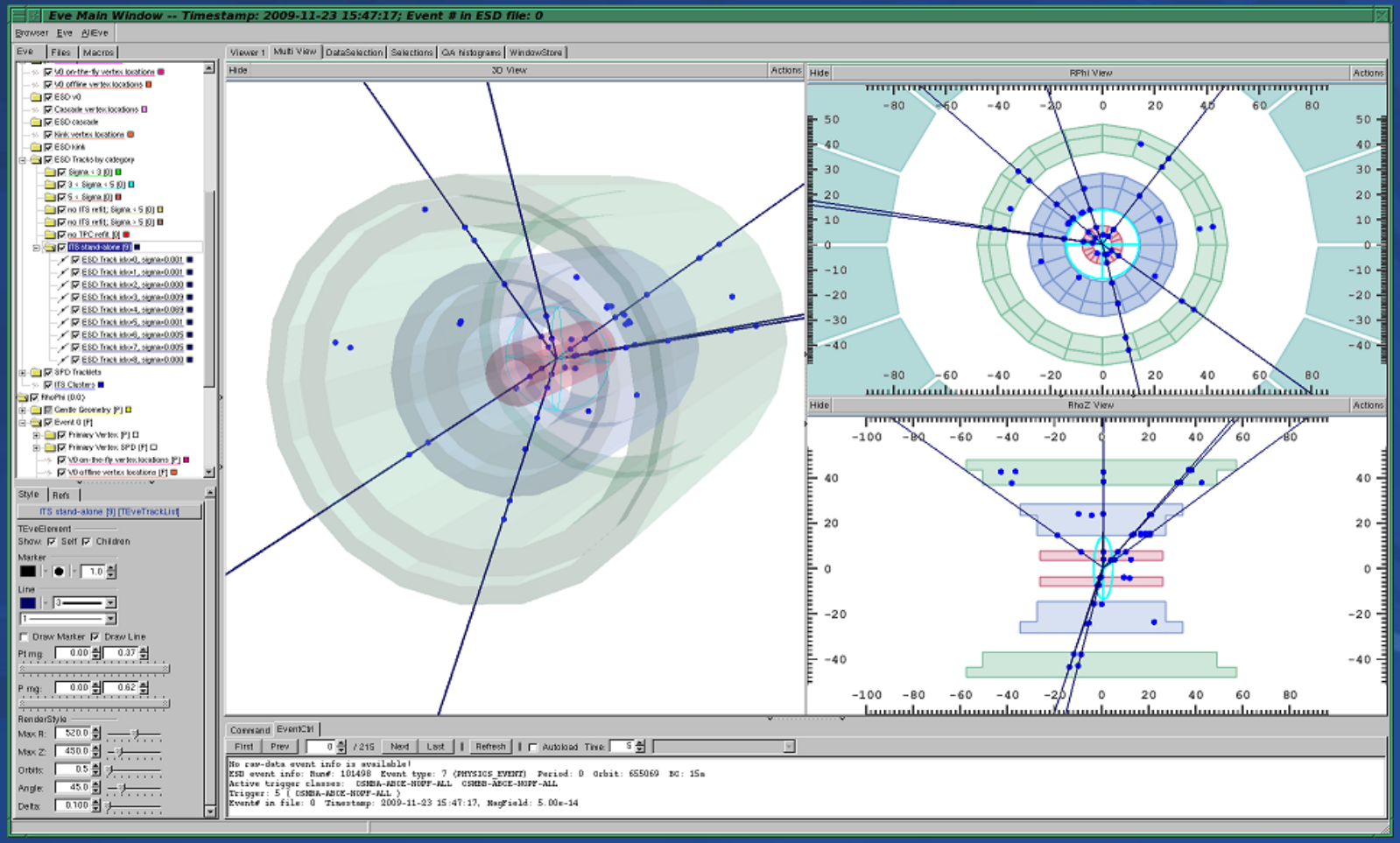


σ = 48 μm
40 μm in simulations with ideal alignment

rφ resolution ~14 μm
nominal in rφ ~12 μm

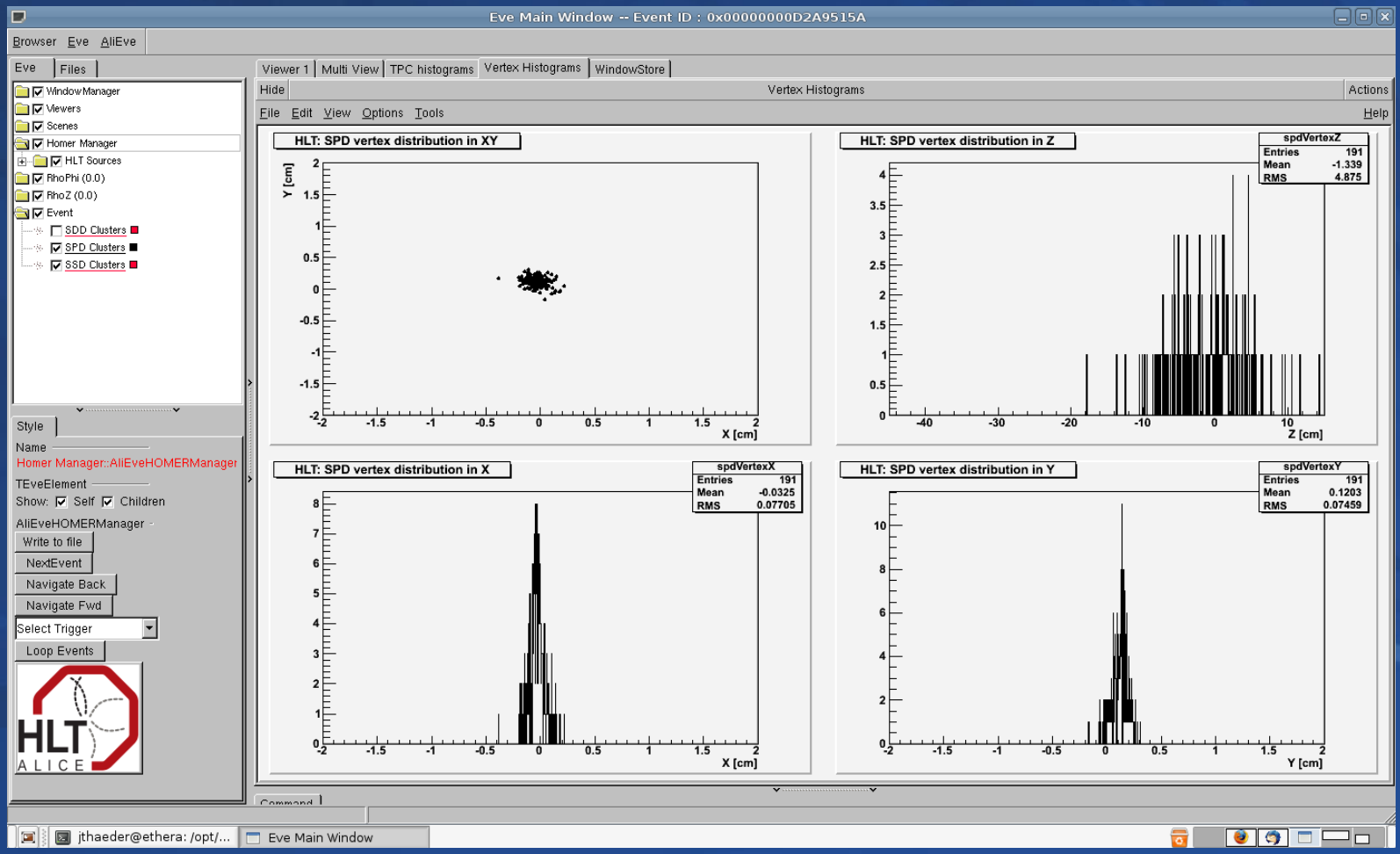
Beam data: first collision

- Detectors ON: SPD, SDD, SSD, V0, ZDC, PMC
- Trigger: Fast-OR minimum bias (threshold = 1) && BPTX beam pickups



Beam data: first collision

- Vertex distribution along z calculated online by High Level Trigger from tracklets in the SPD



Summary

Silicon Pixel Detector & Pixel Trigger are ready for data taking

- L0 trigger for ALICE experiment (cosmic runs and beams)
- first physics paper published by a LHC experiment (ref. EPJ-C Eur.Phys.J.C65:111-125,2010 - 10.1140/epjc/s10052-009-1227-4)

SPD commissioned in 2008

- system integration with ALICE central services (ECS, DCS, DAQ) ok

Optimization during 2009

- upgrades of the cooling system
- calibration scans on the full detector
- new Fast-OR automatic tuning procedure in place

Cosmics campaign in 2008-2009

- collected 10k events for the alignment
- alignment of the ITS modules well advanced

First data with beams collected end of 2009, ready for long run period