The Silicon Vertex Detector of the Belle II Experiment

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Abstract

After ten years of successful operation, the Belle experiment at KEK (Tsukuba, Japan) will be completed in 2010. Thereafter, a major upgrade of the KEK-B machine is foreseen until 2014, aiming at a final luminosity of $8 \times 10^{35}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$, which is about 40 times higher than the present peak value. Consequently, also the Belle experiment needs to be changed and the Silicon Vertex Detector (SVD) in particular will be completely replaced as it already operates close to its limits in the present system.

The future SVD (a.k.a. SuperSVD) will consist of four layers of double-sided silicon strip detectors like the present one, but at larger radii, because it will be complemented by a two-layer Pixel Detector as the innermost sensing device. The SuperSVD will be entirely composed of silicon sensors made from 6" wafers read out by APV25 front-end chips that were originally developed for the CMS experiment at the LHC.

Several years of R&D effort led to innovations such as the Origami chip-on-sensor concept and readout electronics with hit-time finding which were successfully demonstrated on prototypes. These features will be included in the final system which is presently being designed. This paper will give an overview of the SuperSVD and present results from prototype tests ranging from detector modules to back-end electronics.

Key words: Silicon Vertex Detector, Belle II, KEK, B Factory, APV25, Origami
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1. Introduction

Since its commissioning in 1999, the Belle experiment [1] at the KEK laboratory in Tsukuba (Japan), has accumulated more than $1\,\mathrm{ab}^{-1}$ of integrated luminosity mostly at the $\Upsilon(4S)$ resonance in the B system. The precise study of CP violation and related fields has confirmed the theoretical predictions of Makoto Kobayashi and Toshihide Maskawa [2] and consequently, Belle was explicitly mentioned – as well as its American counterpart BaBar – in the announcement of the 2008 Nobel Prize awarded to the aforementioned Japanese physicists.

Already the present luminosity of the KEK-B machine, whose electron and positron beams solely collide in the center of the Belle experiment, sets the world record, peaking at $2.11\times10^{34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$. Nonetheless, observation of rare processes and the demand for high statistics have led to an upgrade program for both the machine and the experiment within the next few years, aiming at an ultimate luminosity that is 40 times higher than present. Naturally, the present detector was not laid out for such intensity and thus needs to be completely refurbished, leading to the Belle II experiment [3].

2. SVD2 – The Present Silicon Vertex Detector

The SVD2 [4], which has been in operation since 2003, is the innermost component of the preset Belle experiment and is composed of four layers of double-sided silicon sensors at radii of 2.0 to 8.8 cm from the beam axis. Similar to other detector sub-systems, it covers polar angles between 17° and 150°, an asymmetry which reflects the forward boost arising from the fact that the electron beam has a higher energy than its positron counterpart. The ladders are built with sensors made from 4" wafers and entirely read out at the edges outside the sensitive region using the VA1TA chip of the Viking family with a shaping time of 800 ns. Thus, the strips of up to three detectors are concatenated (ganged) together in order to achieve this configuration and minimize material budget.

In certain aspects, the present SVD2 already operates at its limits and this clearly shows that it cannot be used after the upgrade in its current configuration: First, due to a significant background, the average occupancy of the innermost layer is in the order of 10%. As the luminosity shall be increased by a factor of 40, it is obvious that this would not work for Belle II. The most efficient way to reduce the occupancy is to decrease the sensitive time window of the front-end amplifier, namely its shaping time. Another approach would be to decrease the sensitive area of each strip, but that would lead to a reciprocal increase in the number of channels and thus complexity as well as cost.

Secondly, the present readout scheme implies a certain dead-time, as the VA1TA has a sample/hold circuit, which renders it blind from the reception of a trigger until all data are read out. Together with some higher-level dead-time, this amounts to a few percent at present, but again would forbid operation at 40 times higher luminosity and thus trigger rate. This issue can be

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overcome by using front-end amplifiers and readout electronics with pipelined data processing which are essentially dead-time free.

3. SuperSVD – The future Silicon Vertex Detector

3.1. Detector Layout

Similar to the SVD2, the future SuperSVD, which is currently being designed, will also be composed of four layers of double-sided silicon sensors, but at larger radii between 3.8 and 14.0 cm and an overall sensitive area of about 1.2 m^2 – more than twice that of the present detector. In the innermost part, the silicon strips will be complemented by two layers of pixel detectors (PXD) made in DEPFET technology [5].

Fig. 1 shows the geometry of the Belle II inner detector including both pixel and strip layers. A common numbering scheme is used to avoid confusion. In the forward region, a slant angle has been introduced in the three outermost strip layers in order to reduce material budget as well as the overall number of channels and at the same time improve the signal-to-noise ratio of forward hits. As the acceptance region is asymmetric, there is no need for a slant angle in the backward region.

3.2. Sensor Design

The entire SuperSVD is composed of only three different sensor types, all made from 6" wafers: two of them are rectangular – where the innermost layer uses a narrower pitch than the outer layers – and the trapezoidal design for the forward region. All sensors are about 300 μm thick and double-sided, i.e. they have orthogonal strips on opposite faces. As the bulk material is of n-type, the n-side strip implants are separated by individual atoll type p-stops in case of rectangular sensors, and by a combined p-stop structure [6] in case of trapezoidal sensors. All strips are AC coupled and biased through poly-silicon resistors. Fig. 2 shows a corner of the design of the trapezoidal sensor's n-side, clearly revealing the combined p-stop structure. All sensors feature one intermediate strip between two readout strips.

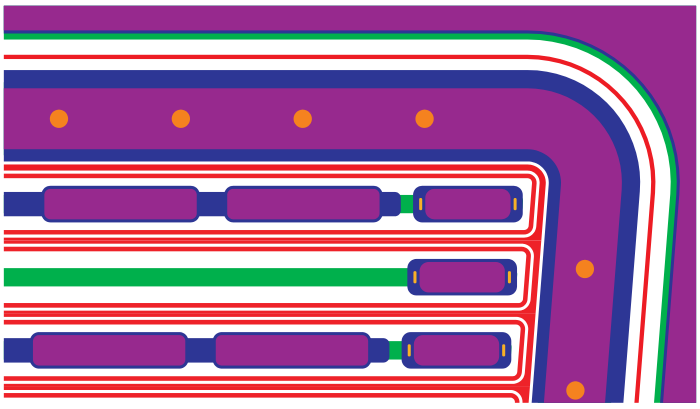

Figure 2: Detail of the trapezoidal sensor design on the n-side.

The dimensions and pitches of the three sensor types can be found in fig. 1. While both the large rectangular sensor (solid lines) and the trapezoidal one (dash-dot lines) feature 768 channels on the p-side and 512 on the n-side, the small rectangular sensor (dashed lines) has 768 channels on both sides.

Prototypes for both rectangular and trapezoidal sensors have been ordered from Hamamatsu Photonics and Micron Semiconductor companies, respectively, and will be delivered by summer of 2010. The main electrical specifications are given in tab. 1. After thorough testing on the sensor level, those devices will be used for building full-size prototype ladders.

3.3. Front-End Readout

As mentioned earlier, the capabilities of the front-end readout amplifier chip play a crucial role for the overall performance of the SVD. Rather than taking the laborious path of designing a new chip, we decided to use the APV25 [7], which was originally developed for the CMS experiment at the LHC, and perfectly fits the needs of Belle II. Referring to the shortcomings of the SVD2 mentioned in section 2, the APV25 has a shaping time of just 50 ns (compared to the 800 ns of the VA1TA) and an internal pipeline of 192 cells which allows a certain trigger latency and to record subsequent triggers while reading out data of previous events.

The APV25 has a built-in feature called "deconvolution" [8] which is used in CMS to narrow down the sensitive time window to a single bunch crossing, but requires clock-synchronous particle hits and thus cannot be used in Belle II because of the quasi-continuous beam collisions. Nonetheless, the APV25 can emit (multiples of) three consecutive samples along the shaped waveform upon the reception of a trigger and thus allow off-detector data processing. As the shaping curve is known, a numeric fit can be applied to the samples of one hit, yielding peak amplitude and timing.

This procedure was tested with several different prototype detector modules at various beam tests. The overall output is a double-logarithmic correspondence between the cluster signal-to-noise ratio and the RMS timing resolution, where the precision is typically 3 . . . 4 ns with cluster signal-to-noise ratios of 12 . . . 15 [9]. It has also been shown that the three highest samples around the peak are sufficient to obtain the peak time, and thus the method can (and will) be implemented in FPGAs using lookup tables for online processing. This procedure aims at an additional reduction of occupancy. While a factor of about 12.5 (measured) is already gained by the faster shaping of the readout chip, another reduction by up to eight (depending on signal-to-noise and trigger jitter) can be achieved by narrowing the sensitive time window through hit time finding. This allows to discard off-time background hits and consequently, the overall occupancy of the SuperSVD will be a few percent in the worst case at full luminosity.

Unfortunately, one drawback inevitably comes along with fast shaping, which is noise. Even though, with a noise figure of 250 e + 36 e/pF, the APV25 performs excellent in its class of fast front-end amplifiers, this is naturally much higher than the VA1TA with 180 e + 7.5 e/pF. One immediate consequence is, due to the steeper slope, that ganging of several sensors is no longer possible as it would multiply the load capacitance and thus the noise. In fact, the slope term dictates that

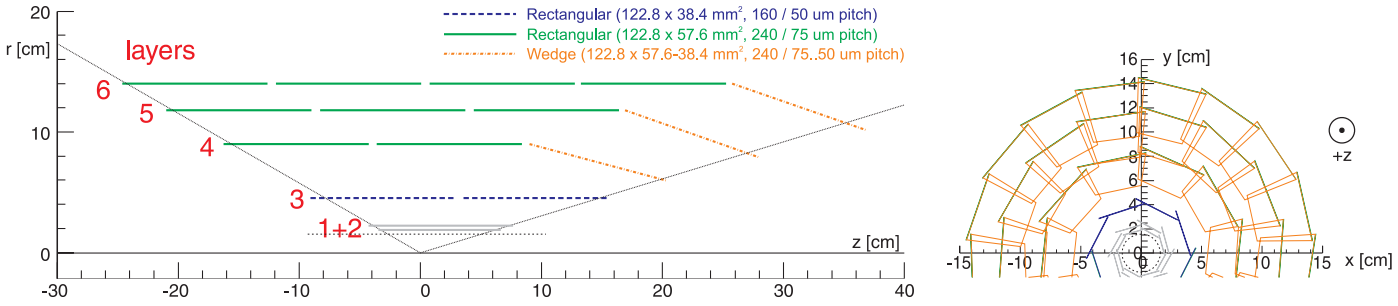

Figure 1: Layout of the SuperSVD including the two innermost pixel layers (PXD). Drawings and dimensions merely show the active areas of the sensors.

Property	Rectangular	Trapezoidal
Resistivity ρ	8 kΩ cm	8 kΩ cm
Depletion voltage V_{FD}	< 120 V	40 V (typ.), 70 V (max.)
Breakdown voltage V_{BD}	≥ FD + 50 V	≥ 2.5 × FD
Polysilicon resistor R_{poly}	4 MΩ (min.), 10 MΩ (typ.)	10 MΩ (min.), 15 ± 5 MΩ (max.)

Table 1: Electrical specifications of the prototype sensors.

capacitance must be kept as low as possible to maintain good signal-to-noise, especially with relatively large sensors made of 6" wafers. This also rules out long fanout lines, which would also add significant capacitance.

3.4. Module and Ladder Design

The only feasible solution to overcome the problems mentioned above is to place the readout chips as close to the strips as possible, leading to what we call the "Origami" chip-on-sensor concept [10]. A prototype module, built around a 4" double-sided sensor, is shown in fig. 3. Eight APV25 chips, all thinned down to about 100 μm for material reduction, are aligned on a flex circuit (hybrid) which sits on the sensor, separated by a 1 mm thick layer of Rohacell (a low density rigid foam) for electrical and thermal insulation. The short strips of the sensor (top side) are wire-bonded to a pitch adapter in front of the central four chips. The long strips on the opposite sensor face (bottom side) are connected through two flex pitch adapters wrapped around the edge of the sensor (hence the name "Origami"). This arrangement allows to place one single, thin cooling pipe on top of all APV25 chips for thermal management.

In case of the SuperSVD, this concept will be applied to each sensor in a ladder except for the ones at the edges of acceptance, which can still be read out from the sides in a conventional manner. This means that the innermost layer 3, whose ladder only consists of two sensors, will not use the Origami scheme, while the outermost layer 6, comprising five sensors per ladder, will apply the chip-on-sensor concept for the central three of those.

A design study for the mechanics of the longest and thus most complicated ladder of the outermost layer is shown in fig. 4. The sensors are mounted on ribs made of a lightweight sandwich structure of carbon fiber and Rohacell, which are held by aluminum pieces at the edges outside of the acceptance volume. The ribs were dimensioned such that the gravitational sag of the structure, regardless of the actual orientation, is less than

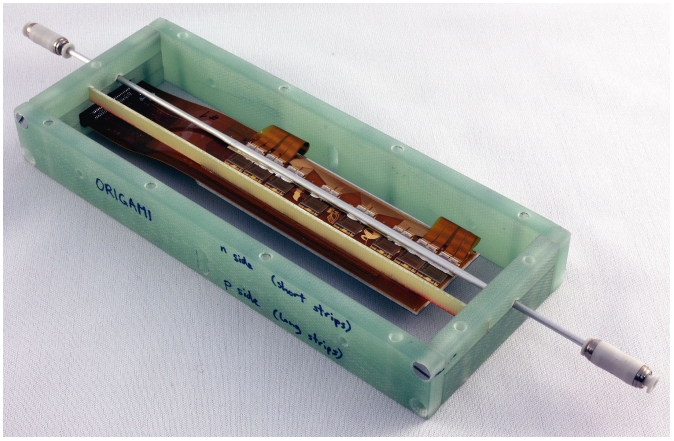

Figure 3: Origami prototype module demonstrating the chip-on-sensor concept.

100 μm. Taking everything into account, the averaged material budget of the central Origami module accounts for 0.58% X_0, with the majority being contributed by the sensor itself.

There are several options for cooling. While simple liquid cooling above the dew point would be sufficient to remove the heat dissipated by the APV25 chips (about 0.35 W per chip), it was measured that the signal-to-noise ratio improves at lower temperatures. Compared to room temperature, about 20% can be gained by operation at −10° C. As the SuperSVD is in close proximity to the PXD [5], a common cooling concept will be devised. At the moment, a dual-phase CO_2 approach seems to be the most attractive solution for such a combined thermal management effort, but this is very preliminary.

Fig. 5 shows the windmill arrangement of the SuperSVD together with evaporation cooling pipes. In order to avoid the congested forward region, each cooling pipe will serve two ladders and thus all cooling services are connected in the backward side only.

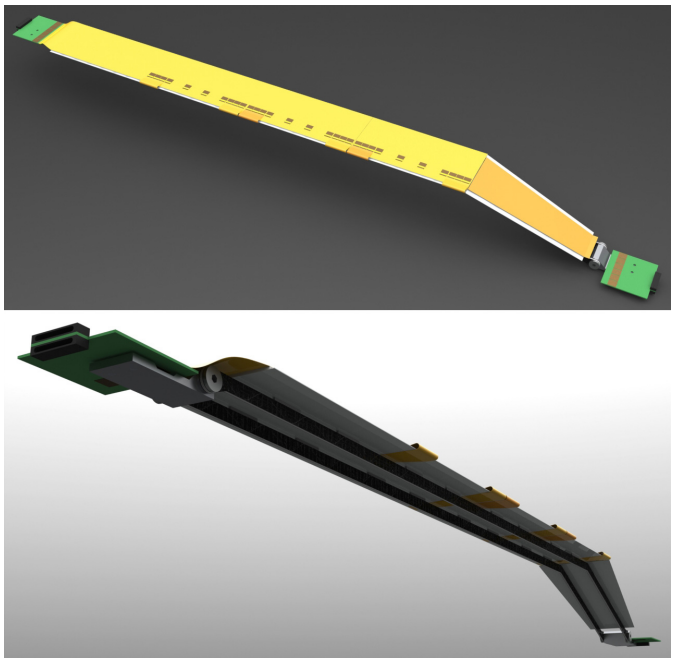

Figure 4: Concept for the longest ladders in the outermost layer 6, shown from two different viewpoints. The top side (top) holds several aligned APV25 chips on its Origami modules, while the bottom side (bottom) reveals the support ribs.

3.5. Readout Chain

Several years of R&D were already spent on the readout scheme for the SuperSVD. A prototype system exists which has been developed for an intermediate upgrade where only the innermost two layers of the SVD2 were to be replaced. Eventually, this plan was dropped in favor of a full upgrade for Belle II. Nonetheless, that prototype system was extensively verified both in the lab as well as in several beam tests [9]. It consists of a repeater box close to the front-end, which takes care of signal buffering and voltage level translation. As the front-end electronics is supplied by low voltages residing on top of the respective bias voltage (typically ±40 V), all signals need to be translated to earth-bound levels for the back-end, which is composed of 9U VME modules, one master controller and several readout boards called "FADC+PROC".

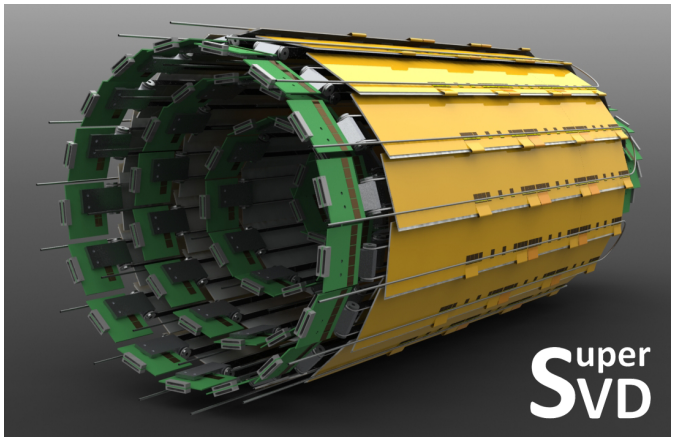

Figure 5: 3D rendering of the SuperSVD.

The SuperSVD scheme will be based on those building blocks, but as the proximity of the detector is considered to be a radiation zone, the repeater part will be replaced by a junction box containing only connectors and rad-hard voltage regulators, while the actual level translation will be merged into the readout boards (see fig. 6). As with the existing "FADC+PROC" modules, these will perform digitization and data processing including zero suppression (sparsification) and hit time reconstruction (see section 3.3). Eventually, the data will be transferred to the common DAQ system by unified optical data links.

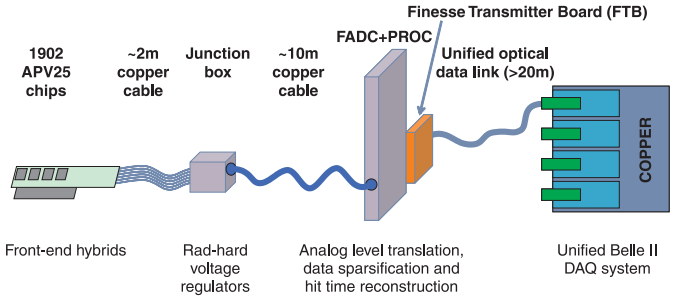

Figure 6: Readout chain of the SuperSVD.

4. Summary

In order to cope with the 40-fold increase in luminosity, the future Silicon Vertex Detector (SuperSVD) will use the fast-shaping APV25 readout chip, which will, together with online hit time reconstruction at a precision of 3 . . . 4 ns, render an occupancy of a few percent at most. The "Origami" chip-on-sensor concept has been proposed for the construction of modules to ensure low-mass readout, achieving an averaged material budget of only 0.58% X_0, while maintaining a good cluster signal-to-noise ratio in the range of 12 . . . 15 despite of using large double-sided silicon sensors made from 6" wafers.

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