The first beam test of a monolithic particle pixel detector in high-voltage CMOS technology☆

I. Perić[a,*], C. Takacs[a], J. Behr[b], F. M. Wagner[c], P. Fischer[a]

[a] *Heidelberg University, Institute for Computer Science, Mannheim, Germany*
[b] *Hamburg University / DESY, Hamburg, Germany*
[c] *Forschungsneutronenquelle Heinz Maier-Leibnitz (FRM II), The Technical University of Munich, Munich, Germany*

Abstract

The results of beam- and irradiation tests preformed on a monolithic particle pixel detector in high-voltage CMOS technology will be presented for the first time. All tested detectors are implemented in a 0.35 μm technology, they utilize high-voltage n-well/p-substrate diodes as pixel sensors and rely on charge drift in diode depletion layers as the main signal generating mechanism. The detector prototype tested in the beam is a system on a chip that contains a 128×128 matrix with $21 \times 21\,\mu m^2$ large pixels, source-follower based- rolling shutter readout and on-chip ADCs that digitize the signal amplitudes with 8-bit precision. Test beam measurements have been performed using EUDET infrastructure. The measured MIP cluster signals are typically 2200 e, spatial resolution approximately 7 μm (RMS), signal-to-noise ratio of a single pixel is 12.3 and detection efficiency more than 85%. To test the radiation tolerance, several detector chips have been irradiated with neutrons up to $10^{14} n_{eq}/\,cm^2$ and with x-rays up to 500 kGy (50 Mrad), they are still functional and the experimental results obtained with these chips will be presented as well.

Key words: Monolithic pixel detectors, high voltage CMOS technology

1. Introduction

A monolithic pixel detector in high-voltage (HV) CMOS technology is a novel detector concept that has a few significant differences compared to a standard MAPS. The HV CMOS detector uses reverse biased (up to 120 V) high-voltage n-well/p-substrate diodes as charge collecting electrodes and relies on drift in roughly 10 μm-thick diode depletion regions as the main charge collection mechanism. This leads to relatively high MIP signals (when compared to a standard MAPS) - typically 2200 electrons per cluster and an improved radiation tolerance. The unique feature of the detector is placing of pixel electronics inside the collecting electrode. This allows 100% fill factor. Both PMOS and NMOS transistors can be placed inside the collecting n-well using *twin-well* option. Since the charge collection occurs in relatively thin depleted regions the detectors can be thinned up to nearly 30 μm without significant signal loss, which allows the construction of low-material particle detectors. Last but not least, we believe that the detector concept can benefit from the new developments in high-voltage technologies that will for instance allow smaller-size transistors. High-voltage technologies are being continuously developed and their long term availability is assured due to their applications in power management circuits for mobile phones, automotive bus transceivers, printer head-, LCD display- and motor drivers as well as dataline drivers for high speed internet or "Voice over IP".

All HV CMOS monolithic detectors we designed [1] can be classified into two following types:

Type A: The pixel electronics are as simple as possible and allow solely selecting of pixel rows, analog rolling-shutter readout and use a source-follower as amplifier. Only PMOS transistors are used inside pixels, which saves space and allows design of relatively small collecting n-well electrodes with low detector capacitance ($C_{det} \sim 10$ fF). The advantages of type A detectors are the small pixel size/capacitance and absence of static current consumption. Typical type A detector in 0.35 μm high-voltage CMOS technology has $21 \times 21\,\mu m^2$ pixel size, matrix readout time of 50 μs and the analog power consumption (mainly caused by the periphery circuits such as readout ADCs) of 3.05 μW/pixel. Since type A detectors are the only available HV CMOS detectors that allow the readout of signal amplitudes, they are suitable for the investigations of signal generation, charge collection and sharing and other signal-related parameters. For this reason, we have chosen a type A detector for the beam test.

Type B: The pixel electronics contain a charge sensitive amplifier with continuous reset, a discriminator, a threshold-tune DAC and allow a fast trigger-based *binary* readout. Both PMOS and NMOS transistors are used inside pixels. The advantages of type B detectors are in-pixel signal processing (zero suppression), the possibility of signal rise time measurements and automated leakage current compensation. Pixel size and capacitance are larger than in the case of type A detectors ($C_{det} \sim$

☆This paper draws on results from an ongoing research project commissioned by the Landesstifftung Baden-Württemberg. We also acknowledge the support of the initiative and networking Fund of the Helmholtz Association, contract HA-101 ("Physics at the Terascale").

*Corresponding author
Email addresses: ivan.peric@ziti.uni-heidelberg.de (I. Perić)

100 fF – 200 fF), despite of that the noise values are relatively low due to absence of pulsed reset and in-pixel noise-filtering (typically ENC ~ 60 e for 125 ns shaping time). Typical type B detector in 0.35 μm HV CMOS technology has $50 \times 50\,\mu m^2$ pixel size, particle hit timing of 125 ns (limited by time-walk) and an analog power consumption (mainly caused by the in-pixel electronics) of 20 μW/pixel. Type B detector has the advantage over type A detector in terms of timing precision for a given power consumption and can be a good choice for the applications where pixel sizes below $50 \times 50\,\mu m^2$ are not mandatory and the particle flux and pixel occupancy are high.

2. Type A Detector used in the Beam Tests

The detector used in the test beam measurements is the first iteration of the demonstrator that should meet the typical requirements for a microvertex detector; it is a system on a chip that contains a 128×128 matrix (easily scalable to a larger size, e.g. 512×512) with $21 \times 21\,\mu m^2$ large pixels arranged as bricks, source-follower based- rolling shutter readout and on-chip ADCs that digitize signal amplitudes with 8-bit precision. The chip has digital outputs, which allows fast readout - typically 50 μs/matrix. Due to FPGA limitations, we have achieved so far the readout of a half of the matrix in 82 μs.

2.1. Chip Architecture

Figure Fig. 1 shows the block schematic and the photograph of the chip. The pixels are arranged as bricks in order to minimize the charge sharing. The transistor-level schematic, the cross-section and the layout of four pixels are shown in Fig. 2. Note that the spacing between n-wells is larger that the n-well size itself. In the region between the n-wells, the effective thickness of the depleted region seen by incident particles is larger than underneath the n-wells and the electric field is radial.

The pixels are readout in the rolling-shutter mode. For this purpose, a shift register is used to select the pixel row to be readout. Only one row is selected at a time. The voltages stored on the sensor diodes in the selected row are then transmitted to the end-of-column circuitry via column readout lines. The end-of-column electronics contain amplifiers, sample-and-hold circuits, single-slope ADCs and the readout registers. The sensor voltages are amplified, offsets can be subtracted, and analog voltages digitized using 128 single-slope ADCs that operate in parallel. The ADC codes are read out using eight LVDS output links.

All analog parts of the chip are implemented using radiation-hard layout techniques - all NMOS transistors are implemented with annular gates and the guard rings are used to separate n+ regions having nonequal potentials.

The total power consumption of all analog circuits in all 128 channels is 42 mW. Since only one selected pixel-row conducts DC current at a time, the static power consumption of the pixel matrix is low - typically 8 mW. This gives the total power consumption of the detector of 3.05 μW/pixel.

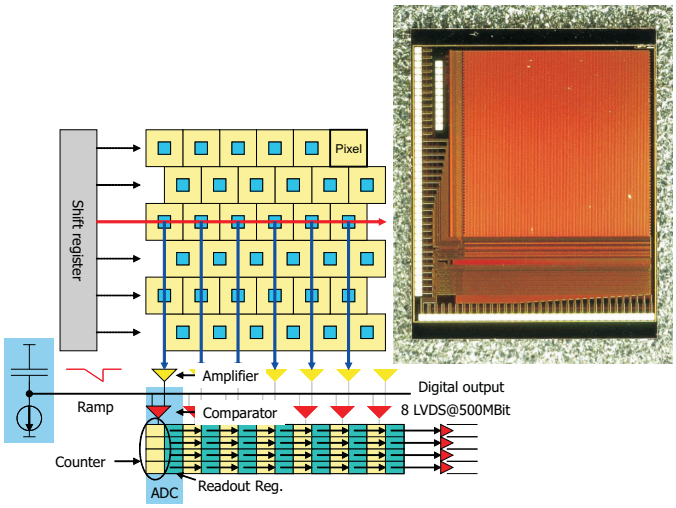

Figure 1: Block schematic and photograph of the chip.

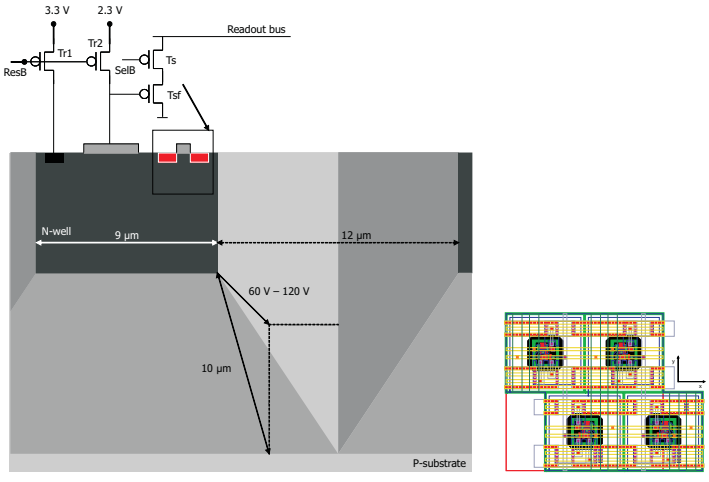

Figure 2: Pixel schematic, cross-section and the layout of four pixels.

2.2. Noise

The major drawback of the detector prototype is its relatively high noise - the measured ENC is 90 e. This overall noise is dominated by the noise of the end-of-column readout amplifiers, not by the detector itself. (Due to non-optimal design, the readout amplifiers are unstable under the nominal bias conditions; by reducing the gain, stability can be restored, however the result is a relatively high noise.) The second detector prototype with optimized amplifier design is already in production and we hope to reduce the overall noise by factor of two.

2.3. Test System

Since the detector chip has only digital outputs, it can be directly readout by the programmable digital chip - FPGA. The processed data are sent to the data acquisition computer via USB. The used system achieves the readout speed of up to 200 MBytes/s.

The pixel signals/voltages can be readout in two modi - the *frame mode* and the *zero suppression* mode. In the frame mode, the entire frames received from the sensor chip are readout via USB. In the zero suppression mode, only the coordinates of the pixels with sufficiently high signal amplitudes are transmitted by the FPGA.

3. Experimental Results

The beam measurements have been performed using EUDET infrastructure; that is a telescope based on MimoTEL chip (CNRS-IHPC institute in Strasbourg, France), EUDAQ data acquisition software and EUTel data analysis software. The measurements have been carried out at DESY and CERN (SpS).

To summarize the results: we measure a most probable MIP cluster signal of 2200 electrons, spatial resolution of approximately RMS = 7 μm, single pixel signal-to-noise ratio of 12.3 and detection efficiency of more than 85%.

3.1. MIP Signal

The MIP spectrum measured at CERN (120 GeV hadrons) is shown in the left plot of Fig. 3. The most probable signal is in the range from 1200 e (single pixel) to 2200 e (6-pixel cluster). The measured S/N ratio varies from 12.3 (single pixel) to 9.8 (6-pixel cluster).

The right plot of Fig. 3 shows the comparison between the most probable ^{60}Co-beta and 120 GeV-hadron signals. ^{60}Co-beta signals are higher by nearly 10% which can be expected due to lower particle energy. The seed pixel collects about 50% of the total signal. The next most significant pixel collects only 25% of the seed pixel signal. Cluster size is six pixels. Although the gaps between n-wells are large, we measure just moderate charge sharing.

The explanation for the rather low charge sharing can be the following: The primary signal is generated in the depleted region and collected by drift; this signal portion is not shared between pixels, it is collected in the pixel nearest to the particle hit point. The diffusion of the electrons generated in the non-depleted bulk is the secondary signal mechanism. This signal is shared between six neighboring pixels.

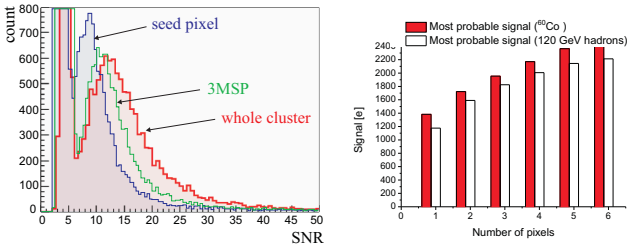

Figure 3: Spectrum of 120 GeV hadrons measured at CERN (left). Comparison between the most probable ^{60}Co-beta and 120 GeV hadron signals (right).

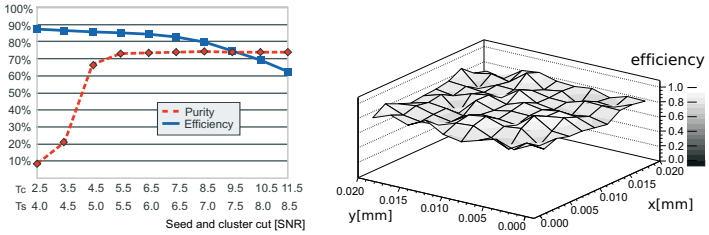

Figure 4: Detection efficiency and purity of the detector as function of the chosen seed and cluster cut (left). Detection efficiency as function of the in-pixel hit point (right).

3.2. Detection Efficiency

The left plot in Fig. 4 shows the detection efficiency and the purity of the detector as function of the chosen seed- and cluster cut. Efficiency is homogenous over the matrix area and saturates at 86% for low seed/cluster thresholds. Efficiency is lower than 100% probably due to timing issues. The readout of the telescope and the DUT is not synchronous. The DUT integration (readout) time was 164 μs (half of the maximal speed) and the telescope integration time was 800 μs. We observe a large cluster and track multiplicity in the telescope planes due to high beam intensity and long integration time. On the other hand there is much lower cluster multiplicity in the DUT which can be explained by shorter integration time. Therefore some of the "out of time" particles that hit the telescope after the trigger moment and during the telescope readout are not seen by the DUT since they arrive after the readout of the DUT is completed. Off-line neglecting of all multiple track events increased efficiency from 72% to 86%. Unfortunately, a part of the scintillator was outside the telescope area. Sometimes a particle which is not visible for the telescope triggers the readout. A certain number of "out of time tracks" can be then seen as the single tracks by the telescope and they can not be distinguished from the real in-time tracks and excluded in the off-line analysis.

3.3. Sub-Pixel Measurements

Excellent spatial resolution of the EUDET telescope allows the investigation of DUT properties as function of the in-pixel hit coordinate. We performed series of such in-pixel measurements.

The right plot in Fig. 4 shows the detection efficiency as function of the in-pixel hit point. The efficiency is homogenous, there are no particularly insensitive regions, *e.g.* between the pixels. This result can be understood as a confirmation of the

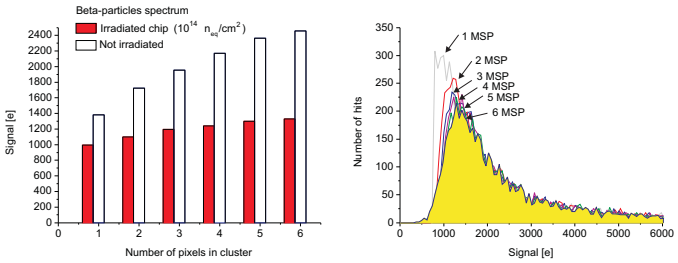

Figure 5: Comparison between the most probable ^{60}Co-beta signals measured with a not irradiated and irradiated chip (left). Spectrum of beta particles measured with the irradiated chip at 0^0 C (right).

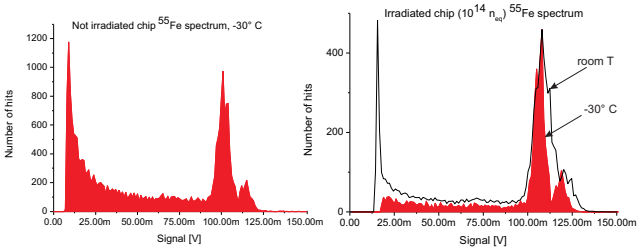

Figure 6: ^{55}Fe spectrum measured with an not irradiated and irradiated chip (left). The same spectrum measured with the irradiated chip (right).

assumption that the efficiency deficit is caused by the timing issues and not by the detector-related insensitivity.

3.4. Spatial Resolution

Spatial resolutions in x and y direction are 7.3 μm and 8.6 μm respectively (RMS of the residuals). The x-y difference is probably caused by the bricked pixel geometry, see Fig. 2. The spatial resolution is not as good as in the case of a standard MAPS due to lower charge sharing and weak CoG correction. The hit point measured by the telescope ("fitted") is sometimes outside of the seed pixel. This mismatch worsens the spatial resolution and occurs more probably when fitted point is near the pixel boundary. The mismatch seems, however, not to be caused by the electronic noise since the affected clusters almost always have by far largest portion of the charge in the seed pixel. One explanation for the seed pixel-hit point mismatch could be multiple scattering. The used PCB does not have an opening below the sensor chip, moreover it contains 1.3 mm long PCB vias filled with copper underneath the chip. The multiple scattering through 1.3 mm of copper could be enough to deflect the particles by a few micrometers.

3.5. Irradiation with Neutrons and X-Rays

A few chips of type A and B have been irradiated with neutrons up to $10^{14} n_{eq}/\,\mathrm{cm}^2$ at Forschungsneutronenquelle Heinz Maier-Leibnitz (FRM II), Technische Universität München, Garching, Germany.

All measured chips are functional. The leakage current increased typically from 350 fA pro pixel before irradiation to 130 pA pro pixel after irradiation (type A). The left plot of Fig. 5 shows the most probable ^{60}Co-beta signals measured by a type A detector before and after irradiation. The most probable signal after irradiation is in the range from 1000 e (single pixel) to 1300 e (6-pixel cluster). The measurement has been performed at $0^{\circ}C$ to reduce the leakage current. Before irradiation, we measured 1300 e (single pixel) to 2400 e (6-pixel cluster). The right plot of Fig. 5 shows ^{60}Co-beta spectra after irradiation.

Fig. 6 shows ^{55}Fe spectra measured with a type B test pixel. The noise increased slightly after the irradiation. The increase is measurable only at the room temperature (ENC at room temperature equals 60 e after irradiation). Spectra show significantly lower number of low energy events after irradiation. These events probably occur when the photons are absorbed in the undepleted bulk regions, the signal charge is then partially collected by diffusion. After neutron irradiation, the sensor bulk is damaged and the charge collection by diffusion become inefficient. A test pixel of type B has been irradiated with x-rays at the Institute of Experimental nuclear Physics (IEKP) of the Karlsruhe Institut für Technologie (KIT), Karlsruhe, Germany, up to 500 kGy (50 Mrad). Before irradiation ENC was 70 e, immediately after irradiation 300 e and after 3 days of annealing at room temperature 130 e.

3.6. Conclusion

We presented the results of beam- and irradiation tests preformed on monolithic particle pixel detectors in high-voltage technology. Test beam measurements have been performed using EUDET infrastructure. The detector prototype used for the test-beam measurement contains a 128×128 matrix with $21 \times 21\,\mu\mathrm{m}^2$ large pixels. The measured MIP cluster signals are typically 2200 e, spatial resolution approximately 7 μm (RMS), signal-to-noise ratio of a single pixel is 12.3 and detection efficiency more than 85%. The non ideal efficiency is probably caused by discrepancy between DUT and telescope readout times in the case of large beam intensity. To test the radiation tolerance, several detector chips of type A and B realized in HV CMOS technology have been irradiated with neutrons up to $10^{14} n_{eq}/\,\mathrm{cm}^2$ and with x-rays up to 500 kGy (50 Mrad).

Acknowledgments

Many thanks to Ingrid Gregor (DESY, Hamburg), Michael Deveaux (Frankfurt University, Frankfurt, Germany), Alexander Dierlamm (IEKP, KIT, Karlsruhe, Germany) as well as EUDET Collaboration for their help. We thank also Landesstiftung Baden-Württemberg for the financial support.

References

[1] I. Perić, A novel monolithic pixelated particle detector implemented in high-voltage CMOS technology, Nucl. Instrum. Meth. A582 (2007) 876–885.