Pixel Readout ASIC for an APD Based 2D X-ray Hybrid Pixel Detector with Sub-Nanosecond Resolution☆

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Abstract

The fast response and the short recovery time of avalanche photodiodes (APDs) in linear mode make those devices ideal for direct X-ray detection in applications requiring high time resolution or counting rate. In order to provide position sensitivity, the XNAP project aims at creating a hybrid pixel detector with nanosecond time resolution based on a monolithic APD sensor array with 32×32 pixels covering about 1 cm^2 active area. The readout is implemented in a pixelated front-end ASIC suited for the readout of such arrays, matched to pixels of $280\,\mu$m $\times$ $280\,\mu$m size. Every single channel features a fast transimpedance amplifier, a discriminator with locally adjustable threshold and two counters with high dynamic range and counting speed able to accumulate X-ray hits with no readout dead time. Additionally, the detector can be operated in list mode by time-stamping every single event with sub-nanosecond resolution. In a first phase of the project, a 4×4 pixel test module is built to validate the conceptual design of the detector. The XNAP project is briefly presented and the performance of the readout ASIC is discussed.

Key words: pixel detector, readout electronics, APD, photon counting

1. Introduction

The goal of the XNAP project is to develop a X-ray pixel detector for synchrotron radiation applications based on a custom APD sensor array. At a pixel pitch of $280\,\mu$m, the planned 32×32 pixel device will have an active area of ≈ 1 cm^2, covered by 1 k pixels. The APDs operate in linear amplification region (contrary to Geiger mode, in which SiPMs operate) in order to achieve a very short recovery time actually limited by the width of the single photon pulses and therefore by the drift time of the charge carriers across the sensor volume. By using sensors about $100\,\mu$m thick, the charge pulses are $\lesssim 3$ ns wide. The ultimate time resolution of the device depends also on the thickness of the silicon due to the uncertainty in the penetration depth of the X-rays, and can be in the order of 1 ns with < 100 ps possible for very thin sensors. That is achieved routinely with discrete APDs and one of the challenging goals is reaching such a time resolution with a 1 k pixel two-dimensional device.

The detector is built by bump bonding the pixelated APD sensor matrix (32×32 pixels), a custom device built by PerkinElmer, and four readout CMOS ASICs (16×16 pixels each) to the two sides of a ceramic interposer. The stackup shown in Fig. 1 solves construction problems, such as high voltage isolation, and provides a certain level of radiation shielding for the readout chips.

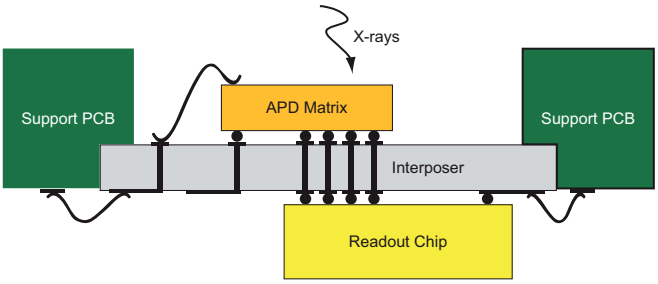

Figure 1: Cross section of the 4×4 prototype system, which will be expanded to hold the 32×32 device.

Each X-ray photon absorbed in one of the pixels produces a current pulse that is amplified twice: First in the sensor through the avalanche process and second in the transimpedance amplifier contained in the front-end chip. The low input impedance amplifier converts the current pulses from the APD pixel element to a voltage signal by applying a variable gain. Then, the signal is passed to a fast leading-edge discriminator to suppress noise and provide a certain level of energy selectivity. The noise level is low enough to obtain sufficient S/N for efficient detection of 5.9 keV photons at moderate internal avalanche gains, estimated to be in the order of 100×. The front-end signal path also includes a polarity switch to allow using various types of APD structures and the differential comparator offers a programmable hysteresis to avoid ringing. Its threshold is set globally using on-chip reference circuitry and can be fine tuned

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on the pixel level to compensate for component mismatch and APD gain dispersion.

The readout chip implements two main modes of operation, list mode and counting mode, but it can also be used in mixed modes that combine both in various ways.

In *list mode* the system allows to timestamp individual photon hits by driving out the hit signals towards external TDCs with sub-nanosecond resolution. The position of each hit is determined by a fast XY readout scheme that also allows for detection of double hit conditions.

In *counting mode*, the number of hits can be accumulated at variable time scales by using one of two 32 bit counters in each pixel. The time window is controlled externally with nanosecond resolution to accommodate a wide range of applications and operating conditions. While one counter accumulates incoming X-ray hits, the other can be read out serially, such that no dead time is introduced. The effective counter depth is variable up to 32 bits and the detector is expected to be operated continuously up to Megahertz frame rates.

All the fast digital processing on the chip uses a low swing differential current mode logic to reduce cross coupling between sensitive analogue and digital parts. Communication between the chip and the subsequent readout electronics is solely done through differential lines. Power consumption has been minimized by reducing supply voltages as much as possible, by designing the subcomponents to match the required speed grade and by biasing the differential logic according to the respective operating speed requirements.

The first phase of the XNAP project aims at building a series of 4×4 prototype systems with various pixel designs before going for the final 32×32 detector. Several test readout chips with individual channels and small 4×4 arrays have been designed and manufactured in the 180 nm UMC 1P6M mixed mode technology.

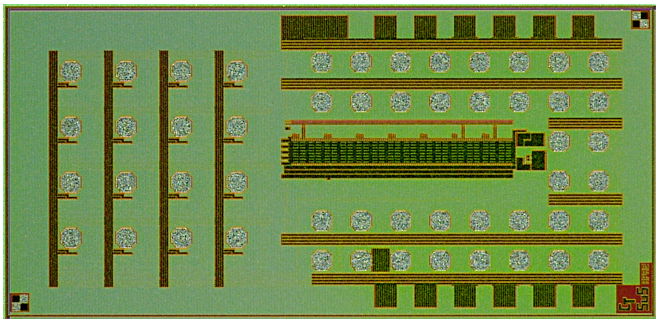

Figure 2: Micrograph of 16 channel test chip. The left half contains the 16 bump bond pads for sensor connection, whereas the right part holds the 36 bump pads for power and I/O connection.

In Fig. 2, a micrograph of the unpackaged silicon die, with the size of $3240\times1525\,\mu$m, is shown.

2. Chip Architecture & Implementation

The APA 2 chip contains an array of 4×4 identical pixels, as well as shared infrastructure blocks consisting of position decoding logic, a bandgap reference and biasing DACs. In Fig. 3, a block diagram of the pixel architecture is shown.

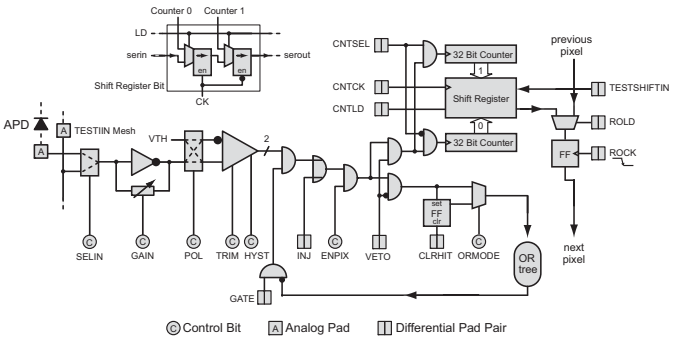

Figure 3: Block diagram of the pixel architecture. The insert in the upper-left edge shows the internal architecture of the per-pixel counter slice. The gating mechanism using the global Or-tree is not shown in detail. On the right hand side, a single bit slice of the fast readout shift register is shown.

2.1. Analog Front-End

The APD current pulses are amplified by transimpedance amplifiers with programmable gain. These amplifiers are based on a simple NMOS gain stage with resistive feedback in order to get maximum signal bandwidth in the given technology. To optimize device matching, the feedback resistor is subdivided into unit devices of 2 kΩ resistance. Through the use of bypass gates, this feedback resistance, equal to the input gain, can be adjusted to four discrete values between 2 mV/μA and 14 mV/μA.

The detection threshold is set globally for all pixels with an on-chip DAC, able to source and sink a current of up to 50 μA with 12 bit resolution. This current is fed into a global transimpedance amplifier, identical to the per-pixel ones, in order to convert the current to a global threshold voltage.

The voltage of the per-pixel transimpedance amplifier and the global threshold voltage are fed via a polarity switch into a differential leading-edge discriminator. Bipolar threshold fine-tuning in every pixel via 7 trim bits with globally adjustable per-bit current allows to cope with device (chip as well as APD) mismatches. In addition, a programmable hysteresis reduces the risk of ringing on the output signal.

The fast hit signal from the comparator is a differential signal having a pulse width in the order of nanoseconds.

2.2. Digital Processing

Depending on the required operation mode, the discriminator output is either routed to a bypassable hit flipflop (list mode) or to a counter structure (counting mode). In list mode, the signal of the hit flipflops is combined to a single output signal by a global Or-tree to drive an external TDC, as well as used internally to gate the pixels to prevent double hits. The hit flipflop can be bypassed to allow for time-over-threshold measurements, which gives access to analog input signal properties. In counting mode, the hit signal increments one of two remotely selectable 32 bit counters. These counters can be incremented

and read out independently allowing for double-buffered counting without losing any events.
Counter selection is done through the use of a dedicated fast input signal. Switching back and forth between these two counters allows for internal discrimination, e. g. prompt and delayed events. Changing between list and counting mode is also done using a dedicated fast input signal, so any combinations of these two modes can be selected with very high time precision.

2.3. Data Readout

Data readout uses a high-speed serial shift register chain clocked at 400 MHz, containing the XY bits at the very beginning of the data stream, followed by the counter bits. Corrupt XY information due to double hits can be detected by the readout system through invalid position patterns. A prepended header pattern allows for clock-data synchronization and a fixed trailer built of logical ones allows to check for complete readout. The shift register can be loaded at any time, allowing for fast partial (XY coordinates) readout.
To read out one XY frame, a typical sequence length of 25 ns is estimated in the 4×4 chip. For the same chip, a 4 bit counter readout of all pixels will have an estimated duration of 260 ns.

3. Measurements

For first tests, a simplified version of the readout chip (APA 1.2) with four channels and additional test ports has been wire bonded to a PCB. This PCB serves as mechanical support and houses the electrical interface to an existing FPGA-based control board. Digital signal buffering and translation between ASIC and FPGA as well as power supplies and conditioning are included on the PCB. Data transfer between the ASIC and a host computer is implemented by an USB FIFO, which is a limiting factor for the data rate.
This PCB is equipped with a connector to link different sensor and injection modules to the board. Three different add-on boards have been developed: A current injection board, a discrete APD board and a APD matrix board.

3.1. Threshold Generator and Trim Circuit

The test PCB, equipped with the current injection add-on, allows for determined current injection. For verification of the threshold generator and the per pixel trim circuit, a constant current was injected. While observing the hit output for switching logic levels, the treshold as well as the per-pixel trim was swept over the full range from high to low and vice versa.
The global threshold generator exposes a perfect linear behaviour in the expected range with a slight constant offset shifted towards lower input current. The per-pixel trim circuit has been proven to work within the expected range of ±64 trim counts whereas the unit trim count current matches well the global threshold range.

3.2. Dynamic Pulse and Counter Testing

Using the same current injection add-on with a high speed digital pulse generator, well determined and precisely timed current pulses can be injected in the transimpedance amplifier. For validation of the ASIC's dynamic behaviour, 10,000 pulses of various pulse lengths in the nanosecond range have been injected for all threshold settings. After pulsing, the number of counted events were read out.

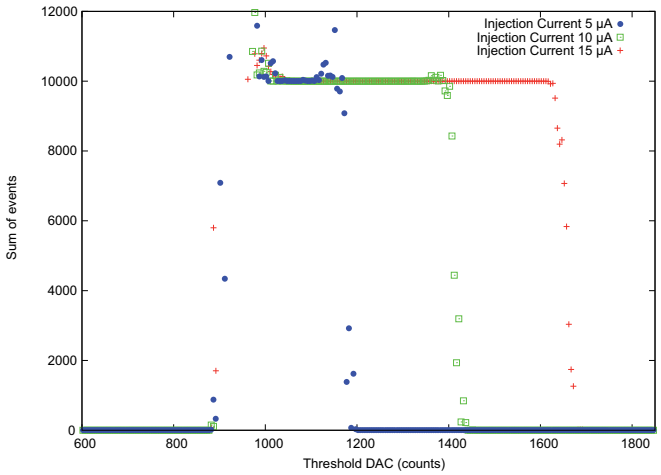

Figure 4: Hit rate as a function of threshold current using current injection. 10.000 pulses with a pulse length of 10 ns each were injected into channel 3 with a transimpedance of 2 kΩ.

The plot in Fig. 4 shows a plateau at 10,000 events. At the plateau's lower boundary (left), the number of counted events exceed the number of injected hits, due to noise effects. The differential width of the plateau (in DAC counts), corresponding to the upper threshold limit, scales well with doubling or tripling the injected current.

3.3. Testing with a ^{55}Fe-irradiated Discrete APD

The readout ASIC was also evaluated with real APD devices. As at that time the APD matrix was not yet available, discrete devices based on the C30817 design by PerkinElmer were used. They have an active area of 0.5 mm^2 and an internal small signal gain of 120× when biased at 360 V. The silicon structure has a thickness of 110 μm.
X-rays with an energy of 5.9 keV from a radioactive ^{55}Fe source were used. These photons are expected to generate a current pulse of about 10 μA at the APD output terminal.

Fig. 5 shows the digital time over threshold hit signal obtained with a ^{55}Fe source. Rise and fall times are in the expected range of 1 ns.
Fig. 6 demonstrates how the hit rate changes with increasing threshold current. The clearly visible plateau at about 40 events per second well matches the expected amount of 63 events per second for the given X-ray source activity and demonstrates nearly full efficiency over a comfortable threshold range. This demonstrates that reliable detection of 5.9 keV X-ray photons is possible, which is very close to the minimum target energy of 5 keV.

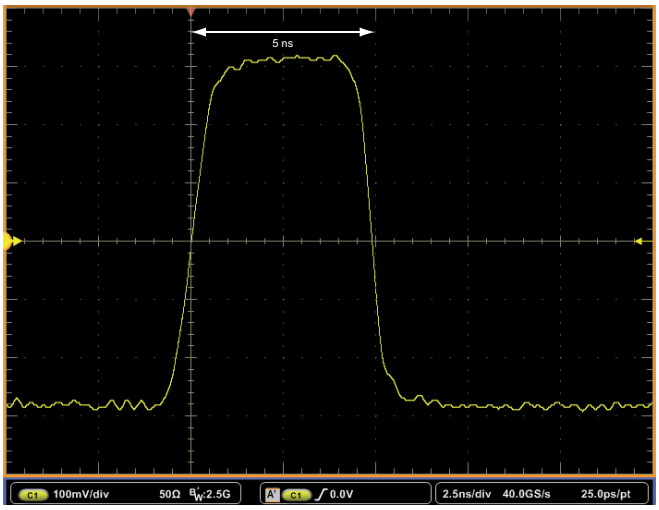

Figure 5: Time over threshold output signal of the TIA for a ^{55}Fe source.

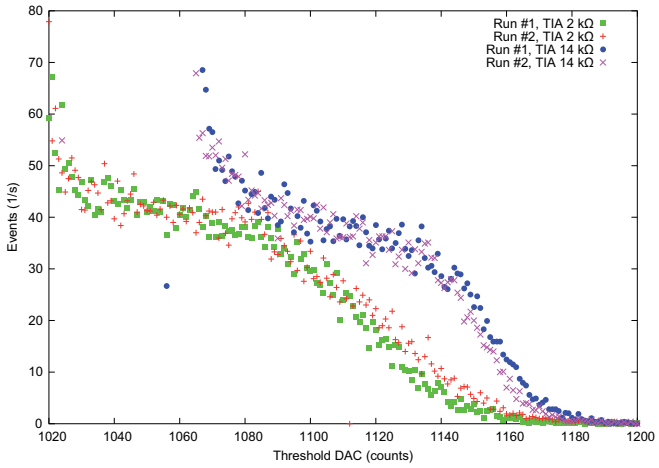

Figure 6: Hit rate for ^{55}Fe irradiation as a function of threshold current during a 10 s capture window. The APD was biased with 340 V. Two runs with two different transimpedance settings were performed.

4. Summary & Outlook

Using a simplified readout chip, by the reliable detection of low energy ^{55}Fe X-ray photons the correct function of the analog front-end part has been proven.
The 4×4 pixel readout ASIC (APA 2) as well as the 4×4 APD matrix arrived from fabrication in February 2010. First tests of the ASIC as well as the sensor showed a very promising behaviour in accordance to simulation data. In addition, extensive tests on previous ASICs proved the correctness of the analog part of the readout chain.
Furthermore, the interposer as well as the mechanical and electrical support and the data acquisition board have already been designed and are currently built. In the following months, the 16 pixels prototype system will be built. First test beam results are expected in mid 2010.

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