Pixel Readout ASIC for an APD Based 2D X-ray Hybrid Pixel Detector with Sub-Nanosecond Resolution

Ch. Thil[1], A.Q.R. Baron[4], P. Fajardo[2], P. Fischer[1], H. Graafsma[3], R. Rüffer[2]

[1]Heidelberg University, Germany; [2]ESRF, France; [3]DESY, Germany; [4]SPring-8, Japan

Abstract

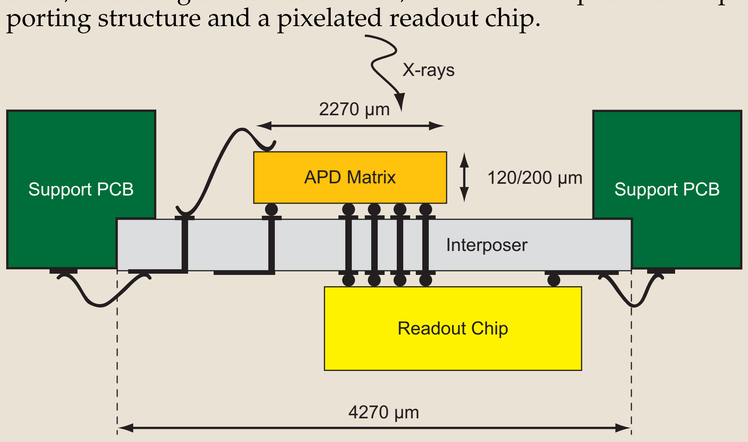
The fast response and the short recovery time of avalanche photodiodes (APDs) in linear mode make those devices ideal for direct X-ray detection in applications requiring high time resolution or counting rate. In order to provide position sensitivity, the XNAP project aims at creating a hybrid pixel detector with nanosecond time resolution based on a monolithic APD sensor array with 32 × 32 pixels covering 1 cm² active area. The readout is implemented in a pixelated front-end ASIC suited for the readout of such arrays, matched to pixels of 300 µm × 300 µm size. Every single channel features a fast transimpedance amplifier, a discriminator with locally adjustable threshold and two counters with high dynamic range and counting speed able to accumulate X-ray hits with no readout dead time. Additionally, the detector can be operated in list mode by time-stamping every single event with sub-nanosecond resolution. In a first phase of the project, a 4 × 4 pixel test module is built to validate the conceptual design of the detector.

Experimental Goal

For applications like nuclear resonant scattering (NRS) or X-ray photon correlation spectroscopy (XPCS), a novel detector for X-rays, starting at very low beam energies of 10 keV, needs to be developed. Today, detectors starting at such low energies and being able to detect very short pulses in the nanosecond time scale are only available as linear arrangements of fast, discrete avalanche photodiodes.
The XNAP project aims at developing a two-dimensional counting X-ray detector based on a novel avalanche photodiode matrix, which will combine the advantage of highly responsive and fast APDs with the ability of two-dimensional photon counting and timestamping.
A prototype system with 16 pixels will be built by the end of 2010. The 32 × 32 pixel system will be used as both technology demonstrator and detector system for different experiments.

System Realisation

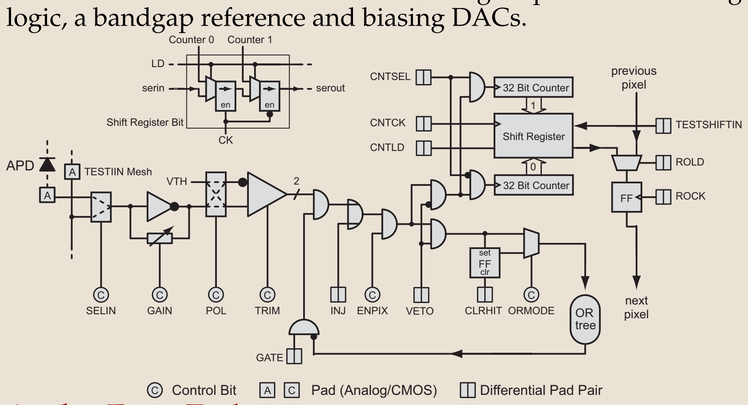
The detector system is built as a hybrid pixel detector using a stack, consisting of the APD matrix, a ceramic interposer as a supporting structure and a pixelated readout chip.



The sensor matrix, a custom device built by PerkinElmer Inc. (Canada), is manufactured in a special fabrication process. Instead of using the APD in Geiger Mode, it is used in Linear Mode which decreases the internal amplification to about 100× but allows for a much shorter dead time.
The readout ASIC was submitted to UMC using their Analog/Mixed Mode 180nm 1P6M technology.
Sensor and readout chip are bump bonded on a ceramic interposer which connects the chips electrically with the applied gold traces and vias. The ceramic is mounted within a hole in the detector PCB and connected to the data acquisition system via common technique wirebonds.

Chip Architecture

The APA2 chip contains an array of 4 × 4 identical pixels, as well as shared infrastructure blocks consisting of position decoding logic, a bandgap reference and biasing DACs.

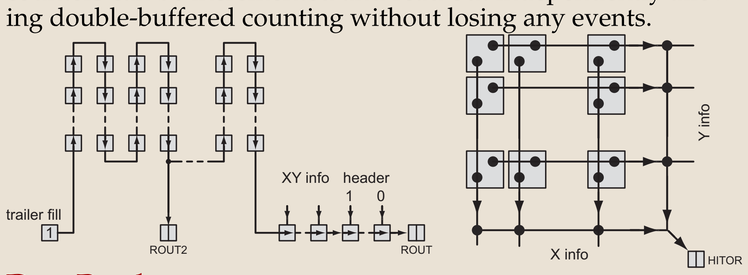


Analog Front-End

The APD current pulses are amplified by transimpedance amplifiers (current to voltage converters) with programmable gain. The detection threshold is set globally for all pixels with an on-chip generated voltage and can be fine-tuned in every pixel to cope with device (chip as well as APD) mismatches. A polarity switch allows for the usage of different APD types. The fast hit signal from the comparator is a differential signal having a pulse width in the order of nanoseconds. It is further processed with low swing differential constant current logic to minimize cross talk and noise induction.

Digital Processing

Depending on the required operation mode, the discriminator output is either routed to a bypassable hit flipflop (list mode) or to a counter structure (counting mode). In list mode, the signal of the hit flipflop is combined to a single output signal by a global Or-tree to drive an external TDC, as well as used internally to gate the pixels to prevent double hits. In counting mode, the signal increments one of two remotely selectable 32 bit counters. These counters can be incremented and read out independently allowing double-buffered counting without losing any events.

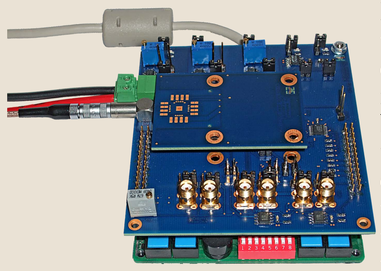


Data Readout

Data readout uses a high-speed serial shift register chain, containing the (x,y) location bits at the very beginning of the data stream, followed by the counter bits.
For power saving, all parts have been optimized to fit the requirements of speed and draw the least possible current using advanced circuit topologies and different biasing voltages.

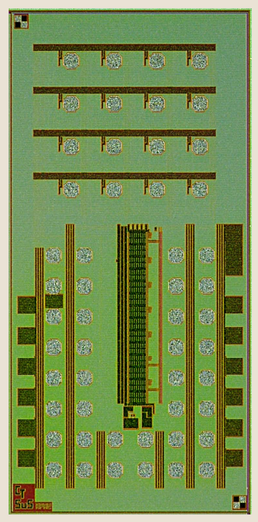
Test Setup

For first tests, a simplified version of the readout chip (APA 1.2) with four channels and additional test ports has been wirebonded to a PCB. This PCB serves as mechanical support and houses the electrical interface to an existing FPGA-based control board. Digital signal buffering and translation between ASIC and FPGA as well as power supplies and conditioning are included on the PCB. Data transfer between the ASIC and a host computer is implemented by an USB FIFO, which is a limiting factor for the data rate.



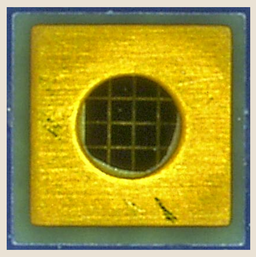
This PCB is equipped with a connector to link different sensor and injection modules to the board. Three different add-on boards have been developed: A current injection board, a discrete APD board and a APD matrix board.

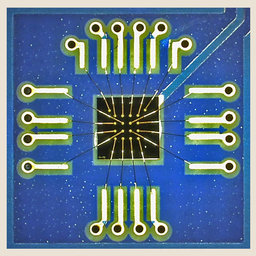
4 × 4 Devices Layout



Left micrograph: APA 2 readout chip

Right micrographs: APD matrix, wirebonded to the APD matrix board, seen from light entry (top) and connection side (bottom)



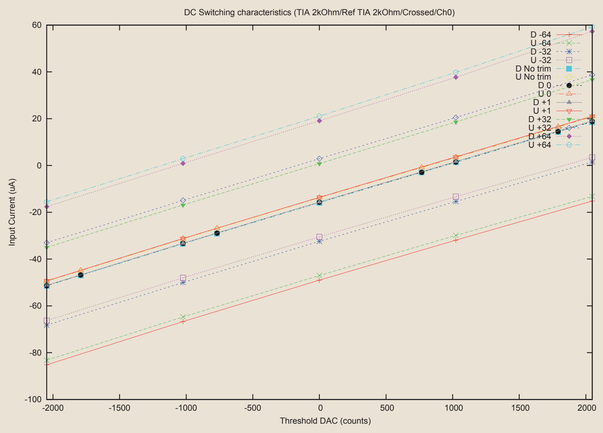


Chip Testing

Prior to testing the whole detector system, each component in the ASIC has been verified separately.

Reference Voltage Generator and Trim Circuit

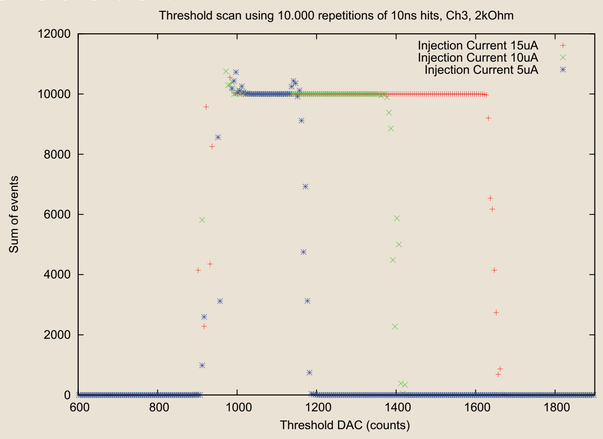
The test PCB, equipped with the current injection add-on, allows for determined current injection. For verification of the reference voltage generator and the per pixel trim circuit, a constant current was injected. While observing the hit output for switching logic levels, the threshold as well as the per-pixel trim was swept over the full range from high to low and vice versa.



The plot shows a perfect linear dependency of the input current and the switching point (in DAC counts). As the sweep was performed in both directions, the difference between the low-to-high (labeled 'U' in the plot) and high-to-low (labeled 'D') switch can be identified with the total noise induced by the analog front-end and reference circuitry, which is about 1 uA.
The per-pixel trim has been verified to be within the expected range of ±64 trim counts.
There is an unexpected offset between the points where the injected current and the reference current change polarity. To understand this behaviour, further investigation is required.

Dynamic pulse and counter testing

Using the same current injection add-on with a digital pulse generator, well determined and precisely timed current pulses can be injected in the transimpedance amplifier. For validation of the ASIC's dynamic behaviour, 10,000 pulses have been injected for all threshold settings. After pulsing, the number of counted events were read out.

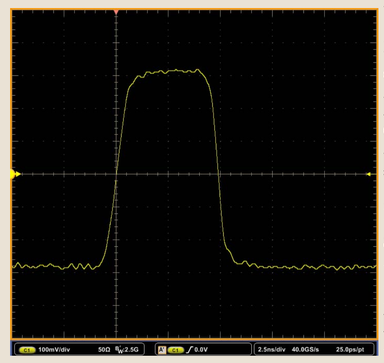


The plot shows a plateau at 10,000 events. At the plateau's lower boundary, the counted events exceed the number of injected hits, due to noise effects. The differential width of the plateau in DAC counts, corresponding to the upper threshold limit, scales well with doubling or tripling of the injected current.

Sensor Readout

The readout ASIC was also evaluated with real APD devices.
The first sensor board was equipped with discrete APD devices, readily available as C30817 APDs from PerkinElmer. These APD dies were glued and bonded to the sensor board to avoid intensity loss at the glass window found in packaged diodes. The diodes are 110 µm thick and provide an active area of 0.5 mm². Like the APD matrix, the internal gain is estimated to be 120× at about 360 V APD bias voltage.
As an X-ray emitter, a Fe-55 calibration source has been used to irradiate the APD with 5.9 keV X-rays at 140 kBq. Assuming isotropic radiation and a distance of 5 mm between source and detector, the photon rate is 63 per second on the APD surface.

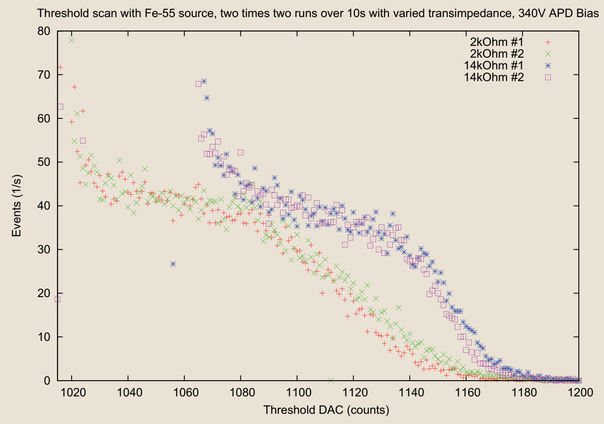
^{55}Fe Pulse Shape



Using the differential discriminator output on the test chip, the pulse shape was sampled with a high bandwidth oscilloscope for visualisation purpose.
With the chosen transimpedance of 2 kOhm and a moderate threshold setting, the typical pulse width is 5 ns FWHM, which is due to the hole drift time in the 120 µm thick device.

^{55}Fe Pulse Counting

Using the integrated pulse counters, the amount of X-ray photons emitted by the Fe-55 source can be determined.



The plot shows four scans, each counting the amount of events during a capture window of 10 s for different threshold DAC settings. For two different transimpedance settings (2 kOhm and 2 kOhm), each scan was carried out twice.
There is a plateau at about 40 events per second, which well matches the calculated number of 63 events per second for 100% APD sensitivity. This demonstrates that reliable detection of 5.9 keV X-rays is possible, well below the 10 keV target energy.

Outlook

The 4 × 4 pixel readout ASIC arrived from fabrication in the first week of February 2010. This year, the 4 × 4 detector system will be built, including a control board for ASIC to host communication, mechanics for housing, cooling and host software. First test beam results are expected in the second half of 2010.