Contribution ID: **243** Type: **Poster (Session A)**

Pixel readout ASIC for an APD based 2D X-ray hybrid detector with sub nanosecond resolution

The fast response and short recovery time of avalanche photodiodes (APDs) in linear mode make those devices ideal for direct X-ray detection in applications requiring high time resolution or counting rate. In order to provide position sensitivity, the XNAP project aims constructing a hybrid pixel detector with nanosecond time resolution based on a monolithic APD sensor array with 32x32 pixels over a 1cm2 active area. The readout is implemented by a pixelated front-end ASIC suited for the readout of such arrays, matched to pixels of 300um size. Every channel contains a fast transimpedance amplifier, a discriminator with locally adjustable threshold and two counters with high dynamic range and counting speed able to accumulate X-ray hits with no readout dead time. In addition to counting mode the detector can also operate in list mode by time-stamping every single hit with sub-nanosecond resolution. A 4x4 pixel test module is being built in a first phase of the project to validate the conceptual design of the final detector. The status of the project will be briefly presented and the performance of the readout ASIC will be discussed.

Summary (Additional text describing your work. Can be pasted here or give an URL to a PDF document):

The goal of the XNAP project is to develop a X-ray pixel detector for synchrotron radiation applications that is based on and APD sensor array. The APDs operate in linear amplification region (not in Geiger mode as the SiPMís for instance) in order to achieve a very short recovery time actually limited by the width of the single photon pulses and therefore by the drift time of the charge carriers across the sensor thickness. By using sensors with thickness in the range of 100 micrometers the charge pulses are about ˜3 ns wide. The ultimate time resolution of the devices depends also on the thickness of the silicon through the uncertainty in the penetration of the X-rays, and can be of the order of 1 ns or less for very thin sensors. That is achieved routinely with discrete APD diodes and one of the challenging goals is reaching such a time resolution with a 1 kpixel (32x32) device.

The detector is constructed by bump bonding the pixelated Si APD sensor and four readout CMOS ASICs (16x16 pixels each) at each side of a ceramic interposer that solves some construction problems (such as high voltage isolation) and provides a certain level of radiation shielding for the readout chips. The pixel pitch is ˜300 micrometers. Every X-ray absorbed in one of the pixels produces a charge pulse that is amplified twice: first in the sensor (avalanche process) and next in the front-end chip with a moderate-gain but very fast transimpedance amplifier. This is the key point for the fast response of this detector. The low input impedance amplifier converts the current pulses from the APD pixel element to a voltage with programmable gain. The voltage output pulse goes through a fast leading-edge discriminator to suppress noise and provide a certain level of energy selectivity. The noise level is low enough to obtain sufficient S/N for efficient detection of 5keV photons at moderate internal avalanche gain in the APD.
The electronic front-end includes a polarity switch to allow using various types of APD structures and the differential comparator offers a programmable hysteresis to avoid ringing. Its threshold is set globally using on-chip circuitry and can be fine tuned on the pixel level in order to compensate for component mismatch and APD gain dispersion.

The readout chip implements two main modes of operation: list mode and counting mode, but it can also be used in mixed modes that combine both in various ways. In list mode the system allows to timestamp individual photon hits by driving out the hit signals towards external TDCs with sub-nanosecond resolution. The position of each hit is determined by a fast (x,y) readout scheme that also allows for detection of double hit conditions. In case of counting mode the number of hits can be accumulated at variable time scales by means of two 32 bit counters implemented in every pixel. The time windows are controlled externally with ns resolution to accommodate a wide range of applications and operating conditions. While one counter accumulates incoming X-ray hits, the other counter can be read out serially, so that no dead time is introduced. The counter depth is variable and the detector is expected to be operated continuously up to MHz frame rates.

Communication between the chip and the subsequent readout electronics is solely done through low voltage differential lines to reduce noise pickup and crosstalk. All fast digital processing on the chip uses a low swing differential logic to reduce the risk of cross coupling between analogue and digital parts. Power consumption has been minimized by reducing supply voltages as much as possible, by reducing the number of

‘fast’ components in the digital part and by biasing the differential logic according to the respective speed requirements.

The first phase of the XNAP project aims to build a series of 4x4 prototypes with various pixel designs before going for the final 32x32 detector. Several test readout chips with individual channels and small 4x4 arrays have been designed and manufactured in the 0.18um UMC technology. The very first results will be presented and an outlook to the final devices will be also given.

Primary author: Mr THIL, Christophe (Heidelberg University)

Co-authors: Dr BARON, Alfred Q.R. (RIKEN SPring-8 Center); Dr GRAAFSMA, Heinz (DESY); Dr DAUTET, Henri (PerkinElmer Inc.); Dr FAJARDO, Pablo (ESRF); Prof. FISCHER, Peter (University of Heidelberg); Dr RÜFFER, Rudolf (ESRF)

Presenter: Mr THIL, Christophe (Heidelberg University)