R&D on novel sensor routing and Test Structure development

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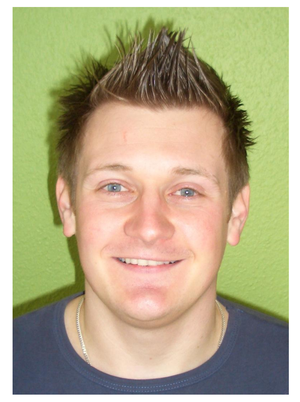

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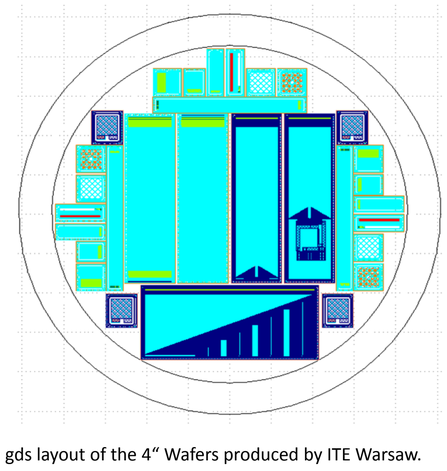
To allow standard monitoring of the process quality of any given vendor, even during a long production circle of several years, the Central European Consortium (CEC) designed and prototyped generic test structures (TS). On the same wafer submission sensors with different routing strategies have been applied to achieve an implementation of a pitch adapter (PA) directly in the silicon sensor in the first metal layer or in a second additional metal routing layer. Such PA on the sensor would allow the design of sensors with short strips, necessary to cope with the much increased particle occupancy at the super-LHC and would also result in a substancial material budget saving for a super-LHC tracking detector.

In summer 2009 a second batch of new TS was produced by the Institute of Electron Technology (ITE), in Warsaw, Poland. We are interested in the process quality compared to the first batch produced by ITE in 2007 and we also wanted to evaluate the impact of the on-sensor PA on the signal-to-noise ratio.

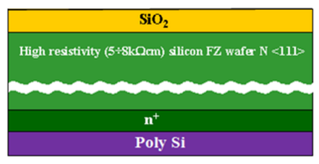
The first section describes the **Manufacturing Process** implemented by ITE Warsaw. The produced structures with the three halfmoons and the sensors and PAsensors will be presented in the **Layout** section. The **Simulation** section shows the 3D model and the results from electric field simulations. In the **Electrical Characterization** section are some of the results of the second generation TS measurements compared with the first generation and the characterization of the sensor and PAsensors. The **Testbeam** setup in presented in section V and finally the first **Results** of the signal-to-noise performance for sensors with integrated Pas is shown.



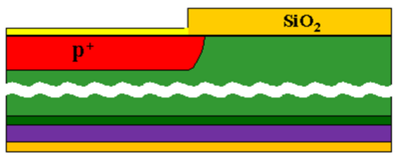
The gds layout of the 4“ Wafers produced by ITE Warsaw.

I. Manufacturing Process

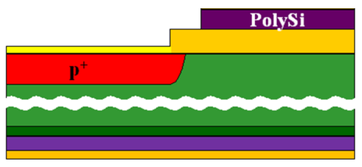
These drawings will give you a rough overview of the manufacturing process (by ITE Warsaw) of silicon sensors. The thickness of the layers are not to scale and we omitted many of the smaller steps in the fabrication process.



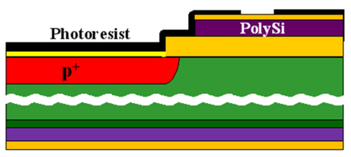
A silicon wafer is oxidized, on the backside the oxide removed and polysilicon deposited and doped to form an extrinsic getter layer and backside n^+ contact.



After following oxidation and photolithography, windows for the p^+ doping are opened. After boron implantation a thin thermal oxide is grown over the implanted areas.

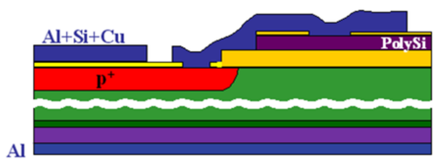


Deposition of a polysilicon layer on top, doping it with boron and pattering defines the polysilicon resistors.



The contacts to the resistors are defined by photolithography and boron implantation lowers the resistivity of the contacts.

Annealing in nitrogen tunes the resistivity of the resistors. A thin insulation is deposited between polysilicon and metal, a photolithographic process defines the opening to the p+ contacts.



Metal is deposited on the front- and backside of the wafer. A photolithographic process defines the pattern of the metallization.

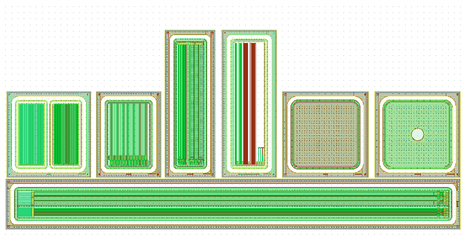
A single metal AC coupled detector is almost ready, only a passivation layer is missing, while for a double metal detectors, a thick oxide with vias would cover the front with a second metal layer above.

II. Layout

On each Wafer are three full halfmoons with improved TS and five AC coupled sensors with innovative sensor-to-readout-connections: Integrated Pitch Adapter

The TS on the halfmoon from left to right and their purpose:

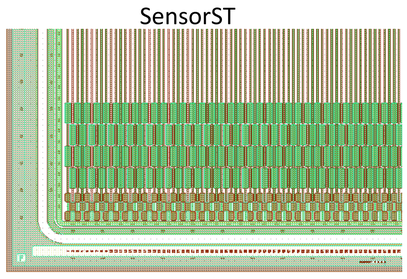
GCD: Surface Current I_{surf} and Flatband Voltage V_{fb}
TS-CAP: Coupling Capacitance C_{ac} and Dielectric Breakdown I_{diel}
CAP-TS-DC: Interstrip Resistance R_{int}
Sheet: Polysilicon Resistance R_{poly} and Resistivity of aluminum and p+
MOS: Flatband Voltage V_{fb} and Oxide Capacity C_{ox}
Diode: Leakage Current I_{leak} and Full Depletion Voltage V_{depl}
CAP-TS-AC: Interstrip Capacity C_{int}

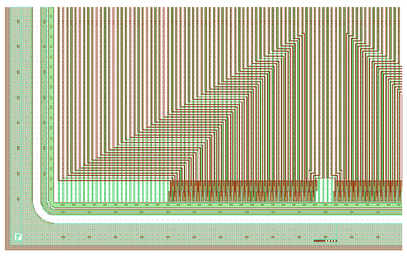


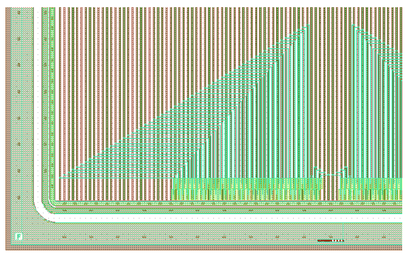
- CAP-TS-AC has been elongated
- Sheet has been elongated and the contact pads enhanced to allow 4-wire-measurements
- Diode with single guard ring (increase breakdown Voltage)

The sensors on the Wafer: 4x 128 strips (double and single metal) and 1x 512 strip double (metal). All sensor have a Pitch of 80um, implant width of 20um and 5um metal overhang.

SensorST







Sensor2MPA

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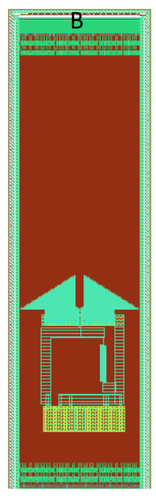
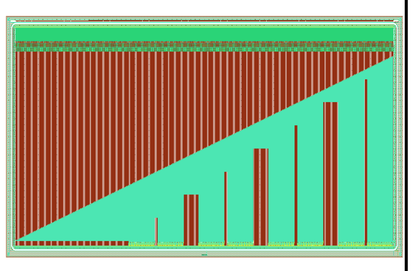


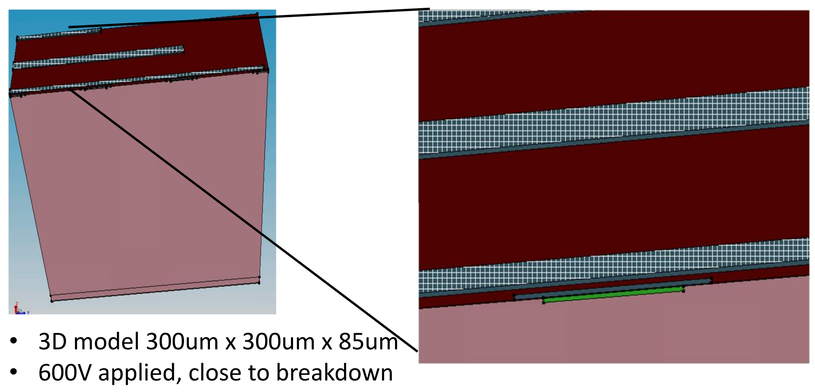
SensorPA



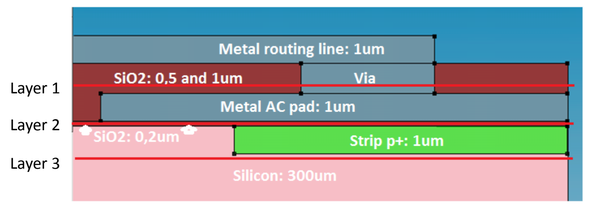
Sensor2MPA90

III. Simulation

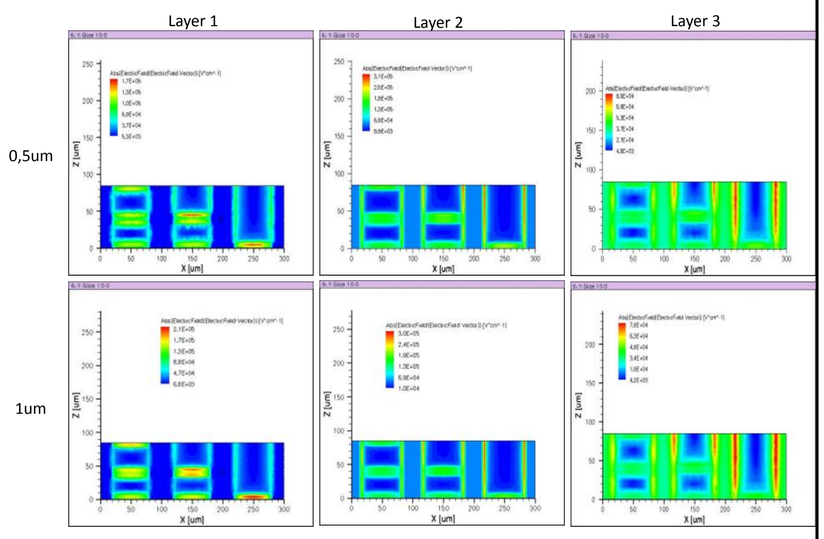
To extract the breakdown voltage and compare the electric field in different layers depending on the insulation layer thickness (0,5um or 1um), we create a 3D model representing a section of a sensor with double metal layer.



- 3D model 300um x 300um x 85um
- 600V applied, close to breakdown
- Using insulation layer of 0,5um and 1um
- Looking at the electric field in 3 layers:



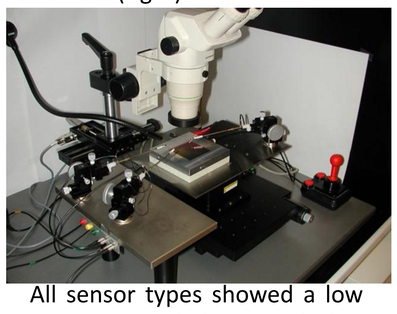
Comparison of the electric fields:



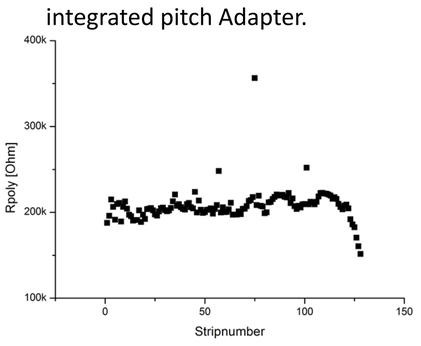
The electric field in the silicon oxide seems not to be improved by changing from 0,5um to 1um.

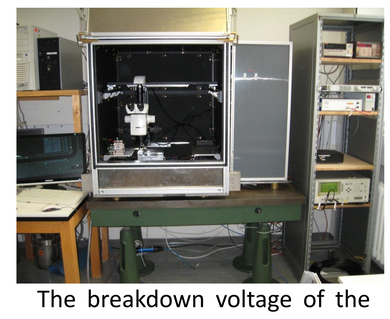
IV. Electrical Characterization

The TS and the sensor have been qualified in Vienna (left) and in Karlsruhe (right).

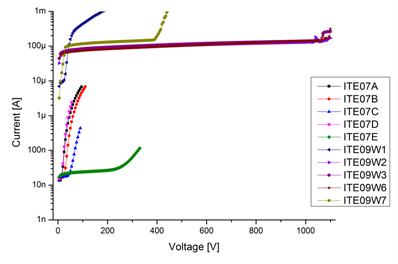


All sensor types showed a low Biasresistor of about 200kOhm and also 10-20 pinholes per sensor. The plot below shows the Biasresistors of ITE09W8PAS a sensor with integrated pitch Adapter.





The breakdown voltage of the diodes is significantly higher in the new design, compared to the 2007 run. The design is stable up to and beyond 1000V (see below).



Measuring the C_{ac} we can calculate the thickness of the readout oxide that should be 177nm. But with the measured value of 37,6pF we calculate a thickness of about 700nm!

$C=e_0 \times e_r \times A/d$; $e_0=8{,}85 \times 10^{-12}$ F/m ; $e_r=3{,}9$ (SiO_2) ; $A=760 \times 10^{-9}m^2$

$\Rightarrow d= e_0 \times e_r \times A/C = 698 \times 10^{-9}m$

=> This implies problems during the wafer processing

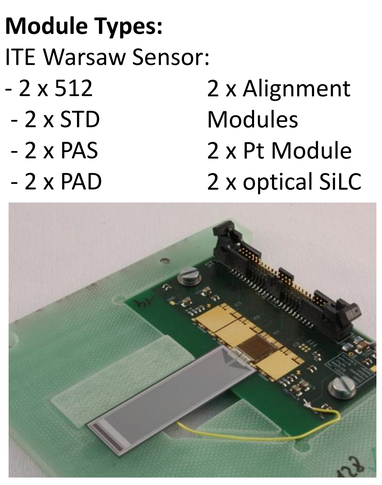
V. Testbeam

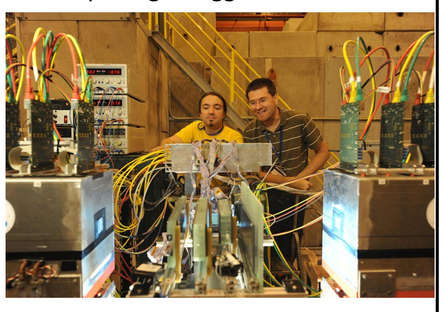
The Testbeam took place from 19. to 26. August 2009 at CERNs SPS Area: H6B, using the EUDET Beam Telescope to get triggers and tracks.

Module Types:

ITE Warsaw Sensor:
- 2 x 512
- 2 x STD
- 2 x PAS
- 2 x PAD

2 x Alignment Modules
2 x Pt Module
2 x optical SiLC

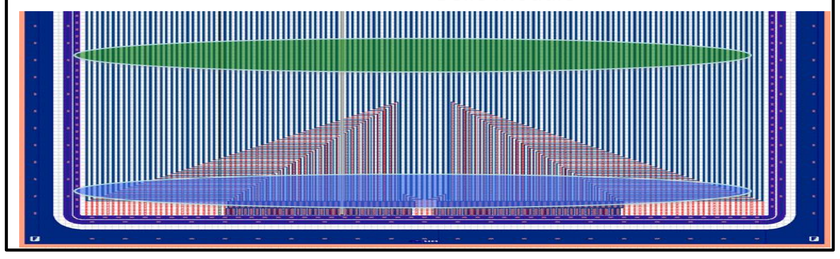




Above is the setup at H6B with two colleagues from Vienna. On the left is one of the PAS moduls.

Details:
- 3.2 million events
- 1 TB of data
- Full Logbook at http://elog.hephy.at/testbeam-SPS09/

Runs:
- ITE Sensor with integrated PAs (see below)
- ITE Sensor with 512 Strips
- Pt Module
- Alignment Module
- Belle Module

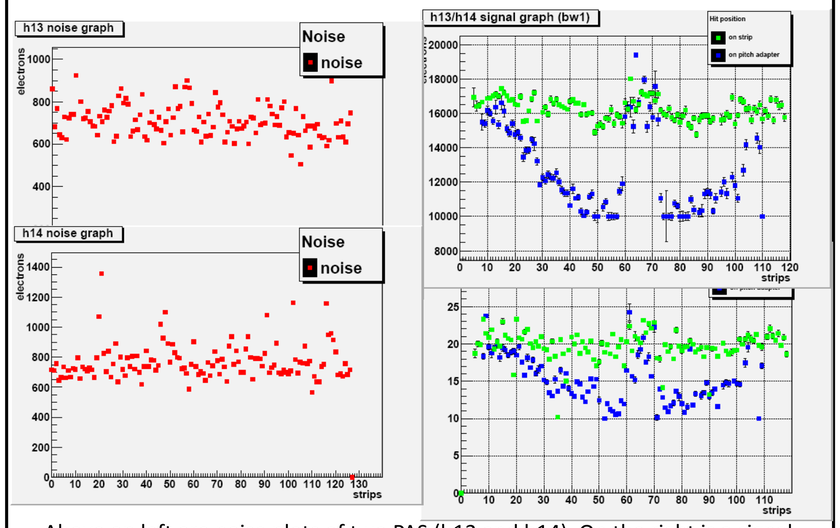


VI. Results

Having still a lot analysis to do some first results are shown for the sensor with integrated pitch adapter single metal layer.

Signal-to-Noise-Ratio on PAS sensors:

No metallization over strip in PA region
- If a PAS is hit in a region with no routing (green region) the signal-to-noise behaviour is similar to the STD sensor
- If the PAS is hit in the routing region (blue region) the SNR suffers from lower efficiency, caused by crosstalk.
- The noise is similar on all strips, the routing has no additional impact.
- The PAD does not suffer from that problem. It still shows some crosstalk, but low. The large number of pinholes makes the data analysis more complicated.



Above on left are noise plots of two PAS (h13 and h14). On the right is a signal and signal-to-noise plot taking both PAS in account.

Data analysis is continuing to get more meaningful and significant plots