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Semi-Digital Hadronic Calorimeter Using GRPCs for Future Linear Collider Experiments

A new concept of high granularity hadronic calorimeter using thin GRPCs as sensitive medium with embedded semi-digital readout electronics to be used in the future linear collider experiments is under development within the CALICE collaboration. Based on this concept, a small prototype was built and tested with success at CERN PS test beam in 2008. To validate completely this new concept a prototype of 1m3 is being conceived. Few GRPCs as large as 1m2 were built with a new design reducing the dead zones and improving on the gas distribution system. The GRPCs were tested with an electronics board of the same size. The board containing 144 of 64-channel ASICs was conceived and built for this purpose. It represents the largest ever built with the embedded electronics scheme.

Summary (Additional text describing your work. Can be pasted here or give an URL to a PDF document):

Development of a Semi-Digital Hadronic Calorimeter
Using GRPCs for Future Linear Collider Experiments
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On behalf of the CALICE collaboration

Abstract–A new concept of high granularity hadronic calorimeter using thin GRPCs as sensitive medium with embedded semi-digital readout electronics to be used in the future linear collider experiments is under development within the CALICE collaboration. Based on this concept, a small prototype was built and tested with success at CERN PS test beam in 2008. To validate completely this new concept a prototype of 1m3 is being conceived. Few GRPCs as large as 1m2 were built with a new design reducing the dead zones and improving on the gas distribution system. The GRPCs were tested with an electronics board of the same size. The board containing 144 of 64-channel ASICs was conceived and built for this purpose. It represents the largest ever built with the embedded electronics scheme
I. INTRODUCTION
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o apply successfully the PFA techniques, granular calorimeters are needed[1]. Calorimeters with gaseous detectors can provide high granularity in addition to excellent homogeneity. This high granularity implies however a tremendous amount of electronic channels. To eliminate the problem of holes related to readout cables and keep the calorimeter as hermitic as possible, readout electronics should be embedded on the detector. In addition, the huge number of electronic channels makes the electrical consumption a major issue. To overcome this difficulty, readout electronics based on power pulsing system using the ILC duty cycle is proposed.

In order to face the previous challenges, the CALICE collaboration is pursuing a new development aimed at constructing a high granular gaseous hadronic calorimeter prototype based on a semi-digital readout and a transverse segmentation of 1 cm2.
In addition to the tracking capacity it offers, a semi-digital readout HCAL can provide very good energy resolution which can be, according to the simulation, as good as the analogue one with an appropriate choice of threshold values. The Semi-Digital HCAL prototype is intended to come as close as possible to the hadronic calorimeters of the future ILC experiments in terms of resolution, efficiency and compactness. .Few gaseous detectors are being investigated to become the sensitive medium of such HCAL: GRPC, GEM and Micromegas. New readout electronics satisfying the ILC constraints was developed and successfully tested on small GRPC detectors and more recently on 1 m2 detector.
II. DETECTOR DEVELOPMENT
W GRPC are well tested detectors. They have been successfully used in BELL for almost a decade and more recently in OPERA and ALICE. Nonetheless, GRPCs to be used as sensitive medium in the future HCAL need to be thinner than the standard ones in order to reduce the total radius of the hadronic calorimeter and hence the cost of the magnet coil inside which the HCAL should be placed. For this reason, GRPC of 3 mm thickness were conceived and built.
In addition to the thickness constraint, dead zones due to spacers used between the two glass plates of the GRPC are to be reduced. New schemes using tiny ceramics balls were elaborated. This reduces the dead zones from few percents to negligible amount. Another important point is the gas consumption in such a detector. New gas distribution designs were studied with the goal to renew the gas efficiently increasing

the homogeneity and at the same time reducing the needed gas flow. Another R&D activity concerning the resistive coating of GRPC is going on. Different coatings were tested to reduce the number of pads associate to one mip. This number was found to go from 1.6/mip in case of standard graphite coating to 1.3/mip for more resistive products like the Licron and Statguard products. To guarantee the homogeneity of the painting on detectors of large surface silk screen printing techniques were successfully used. Stability of high voltage connections were also improved by using new gluing materials. Although the accumulated charge on the HCAL GRPCs in the future ILC experiments is expected to be very small, few GRPC are being exposed to high irradiation in the GIF facility at CERN to discover any eventual aging effect.

A recent development has started recently to improve on the detection rate capacity. Due to the float glass resistivity (1013 Ω.cm) standard GRPC can operate efficiently only with rates below 100 Hz/cm2. New semi-conductive glass (1010 Ω.cm) developed by Chinese group of Tsinghua was used to build small GRPC. Exposure to pions beam at CERN has shown that the new GRPC can operate up to 30 KHz/cm2 with the same efficiency. This breakthrough in GRPC technique is an important achievement not only for future ILC experiments but also for ones like SLHC where very high rates are expected.

Using cosmic rays benches or test beams at CERN, the efficiency of the different GRPCs was found to be more than 90% when operated in the high voltage range between 7 and 8 KV.

III. ELECTRONICS DEVELOPMENT

Use To readout the gaseous detectors mentioned above an electronic chip called HARDROC[2] with a semi-digital readout was developed and successfully tested. The chip has three thresholds (2-bit readout). It has 64 channels and each of the 64 channels is made of:

1-Fast low impedance preamplifier with a variable gain over 6 bits per channel

2-Variable shaper (50-150ns) and Track and Hold to provide a multiplexed analogue charge output up to 15pC.

3- Three variable gain fast shapers (15ns) followed by 3 low offset discriminators which allow handling wide dynamic range from 10fC up to 15pC. The thresholds are loaded by three internal 10-bit DACs.

In addition, the chip has a 128 deep digital memory to store the discriminators outputs and bunch the crossing identification coded over 24 bits counter. It is equipped with a power pulsing system which allows to reach a consumption lower than 10μW/channel with a 0.5% duty cycle. The cross-talk among the 64 channels was measured and found to be less than 2%.

IV. PROTOTYPE

To validate the concept of a semi-digital hadronic calorimeter, a Printed Circuit Board was conceived to host 4 HARDROC. The board provides the connection between adjacent chips as well as the first chip to the readout system. For simplification reasons the readout system using FPGA device was also implemented on the same PCB as well as a USB device responsible of the communication between the FPGA and an external server.

The PCB is an 8-layer, 800-microns thick circuit. On one of the two PCB faces, 256 cooper pads of 1X1 cm2 were printed. The distance between two adjacent pads was chosen to be 500 microns. The cross-talk among adjacent pads was tested before other electronics components were fixed on the PCB by injecting a charge of 1 pc on one pad using an appropriate probe. The charges induced on the adjacent pads were then measured and found to be less than 0.3 %. Acquisition software was also developed. It permits to download the configuration parameters to the different chips and to collect data from these chips through the FPGA device. Two readout modes were implemented. The first one is an ILC-Like one where events are recorded during the bunch crossings and the readout takes place after.

The other mode was conceived for cosmic rays and beam test studies. In this mode the acquisition and data taking is stopped when an external trigger occurs. The memory of the different chips is then read out. In both modes each event is associated with a time stamp. In the external trigger mode the time difference between the external trigger and the last recorded event is also given. This determines the time occurrence of each event with respect to the external trigger one. The time precision is given by the HARDROC internal clock which runs at 5 MHz frequency. The electronics boards described above were attached to small GRPCs and assembled together to form a small prototype of 5 chambers. The acquisition system was extended to deal with the DATA coming from each chamber and assemble them in events. A LABVIEW-based graphic interface was developed. This allowed an easy gain correction of all the channels. The setup was exposed first to cosmic rays and then to beams at CERN. The whole system performed very well and allowed to study the GRPC efficiency and multiplicity. Completed with 2cm stainless steel plates, the setup was exposed to pions at PS to study the first phase of hadronic showers (Fig1).

Fig. 1. The small SDHCAL prototype exposed to pions beam in the PS at CERN.

V. TECHNOLOGICAL PROTOTYPE

The success of the small prototype was the first step towards the construction of the technological prototype. The second and decisive one was to build a fully equipped detector of 1 m2. For this purpose, a new PCB hosting 24 ASICs was designed with the possibility to connect few of them together. Independent interface board (DIF) connecting the PCB to the acquisition system was also produced and tested. Six such PCB were produced and equipped. Every two PCBs were connected to each other and connected to one DIF. The six boards were fixed to a mechanical support made of stainless steel plate and then attached to a 1m2 GRPC. The three DIF connected to the PCBs are chained together and connected to a monitoring computer. An

acquisition system using the Xdaq system[3] developed by the CMS collaboration is used to build events from the collected data. A cosmic ray test bench was used to study the whole system. After a debugging period, the whole system works adequately. Few variants of GRPC were tested using the large electronic board in test beam at CERN in June and August 2009 (Fig2). The collected data were analysed. Synchronization among the different DIF was successful and the data coherence demonstrated (Fig3). The measured efficiency of the 1m2 GRPC was found to be in the same range of those of small GRPC chambers (>90%). This success constitutes an important milestone in the validation of the SDHCAL. To complete this study an improved electronic board equipped with the new version of the HARDROC chips is under construction. The board will be attached to 1m2 GRPC and inserted into a cassette. This will be the first unit of the technological type to be built in 2010. The technological prototype will be made of 40 detectors interleaved with 2cm stainless steel plates. The mechanical structure of the prototype is being currently conceived. The aim is to have a self-supporting structure like the one proposed in the ILD and SiD concepts. The detectors with their readout boards will be cast into cassettes that will be inserted between the Stainless Steel plates.
The readout system will include data concentrators which will connect the DIF mentioned above to the general CALICE acquisition system. The development of data concentrators is almost finished and the whole readout system will be tested very soon to validate the whole chain. Gas distribution system controlling both the gas flow and pressure in the different chambers is under construction in collaboration with the CERN Gas Service. High voltage power supplies using the Cockcroft-Walton were designed and will be produced very soon. The construction of the technological prototype is expected to start at the end of 2009 and to be completed by 2010. In addition to the hardware development, a software activity is going on in order to prepare properly the comparison between data and the hadronic shower models used in the simulation.

Fig. 2. A fully equipped 1m2 GRPC exposed to pions beam in the SPS at CERN.

Fig. 3. Profile of the pions beam as seen by the 1m2 equipped GRPC in SPS at CERN.
VI. CONCLUSION
A small prototype of hadronic calorimeter with semi-digital readout and using GRPCs was built. Tests with pions beams at CERN proved the principle of such calorimeter. 1m2 GRPC fully equipped with the same electronics readout was built and successfully tested. This is the first step in building 4,5 λI hadronic calorimeter which is intended to be as close as possible to the one proposed for the future ILC experiments
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