

Beam Test Results of Different Configurations of Deep N-well MAPS Matrices Featuring in Pixel Full Signal Processing.

We report on further developments of our proposed design approach for a full in-pixel signal processing chain of deep N-well (DNW) MAPS sensor, by exploiting the triple well option of a CMOS 130 nm process. We implemented two different versions of the analog circuits (namely “Apsel 3T1” and “Apsel 5T”) and we optimized the collecting electrode geometry to improve the charge collection efficiency.

We will present the simulation tool that we developed to optimize the collecting electrode geometry and the criteria we adopted to choose the best ones. Two different geometries of the collecting electrode have been implemented in 3 x 3 matrices with analog outputs for each pixel.

The results of the characterization of the various versions of pixel matrices with a pion beam of 120 GeV/c at the SPS H6 CERN facility will be presented, comparing the charge collection efficiencies.

The performances of an “Apsel 3T1” chip irradiated with a dose up to 10 MRad (Co 60) was also measured. Comparison will be presented among the irradiated and the new chip showing the impact of radiation damages on tracking efficiencies.

Summary (Additional text describing your work. Can be pasted here or give an URL to a PDF document):

<http://www.pi.infn.it/~paoloni/VIPIX.pdf>

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