The Gigatracker: an ultra fast and low mass silicon pixel detector for the NA62 experiment

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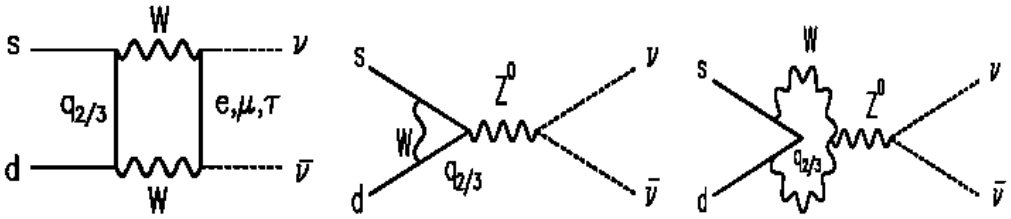
Outline

- The NA62 experiment at the CERN SPS
  - Principle of the experiment and detector layout
- The Gigatracker system
  - Requirements from the experiment
    - Resolution, material budget, radiation hardness
  - Sensor and detector assembly
  - Cooling system
  - Read-out electronics
    - On-pixel Time-to-Digital Converter (TDC)
    - End of Column TDC
  - Status of the R&D
- Conclusions

The $K^+ \to \pi^+ \nu\bar{\nu}$ decay

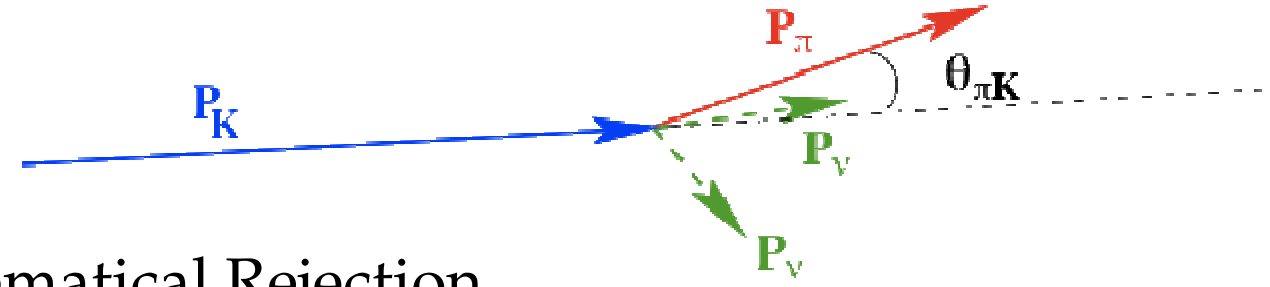
- FCNC loop processes



- Theoretically very clean: hadronic matrix element can be related to measured quantites
- SM predictions (uncertainties from CKM elements):
  - BR($K^+ \to \pi^+ \nu\bar{\nu}$) $\approx (1.6\times10^{-5}) |V_{cb}|^4 [\sigma\eta^2 + (\rho_c - \rho)^2]$ $\to$ **$(8.5 \pm 0.7)\times10^{-11}$**
  - BR($K_L \to \pi^0 \nu\bar{\nu}$) $\approx (7.6\times10^{-5}) |V_{cb}|^4 \eta^2$ $\to$ **$(2.6 \pm 0.4)\times10^{-11}$**
- The $K \to \pi\nu\bar{\nu}$ decays represent a theoretically clean environment sensitive to new physics

- The NA62 Collaboration (former NA48) aims to measure $\mathcal{O}(100)$ $K^+ \to \pi^+ \nu\bar{\nu}$ events with ~10% background at the CERN SPS in two years data taking period

Principle of the experiment

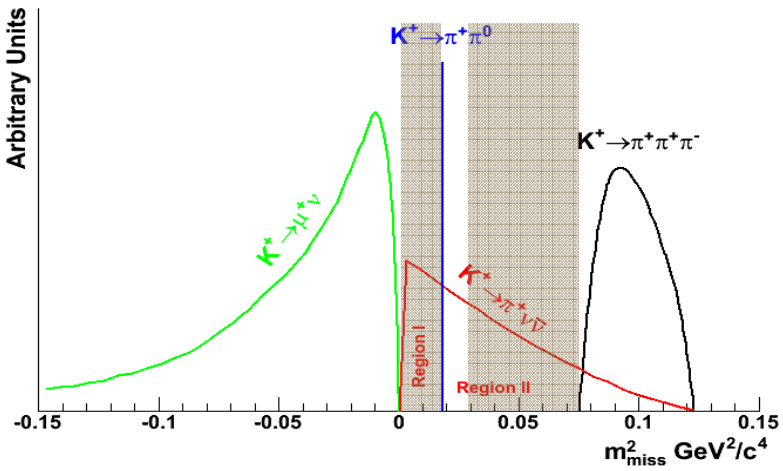


- Kinematical Rejection

$$m^2_{miss} \approx m^2_K\left(1-\frac{|P_\pi|}{|P_K|}\right)+m^2_\pi\left(1-\frac{|P_K|}{|P_\pi|}\right)-|P_K||P_\pi|\vartheta^2_{\pi K}$$

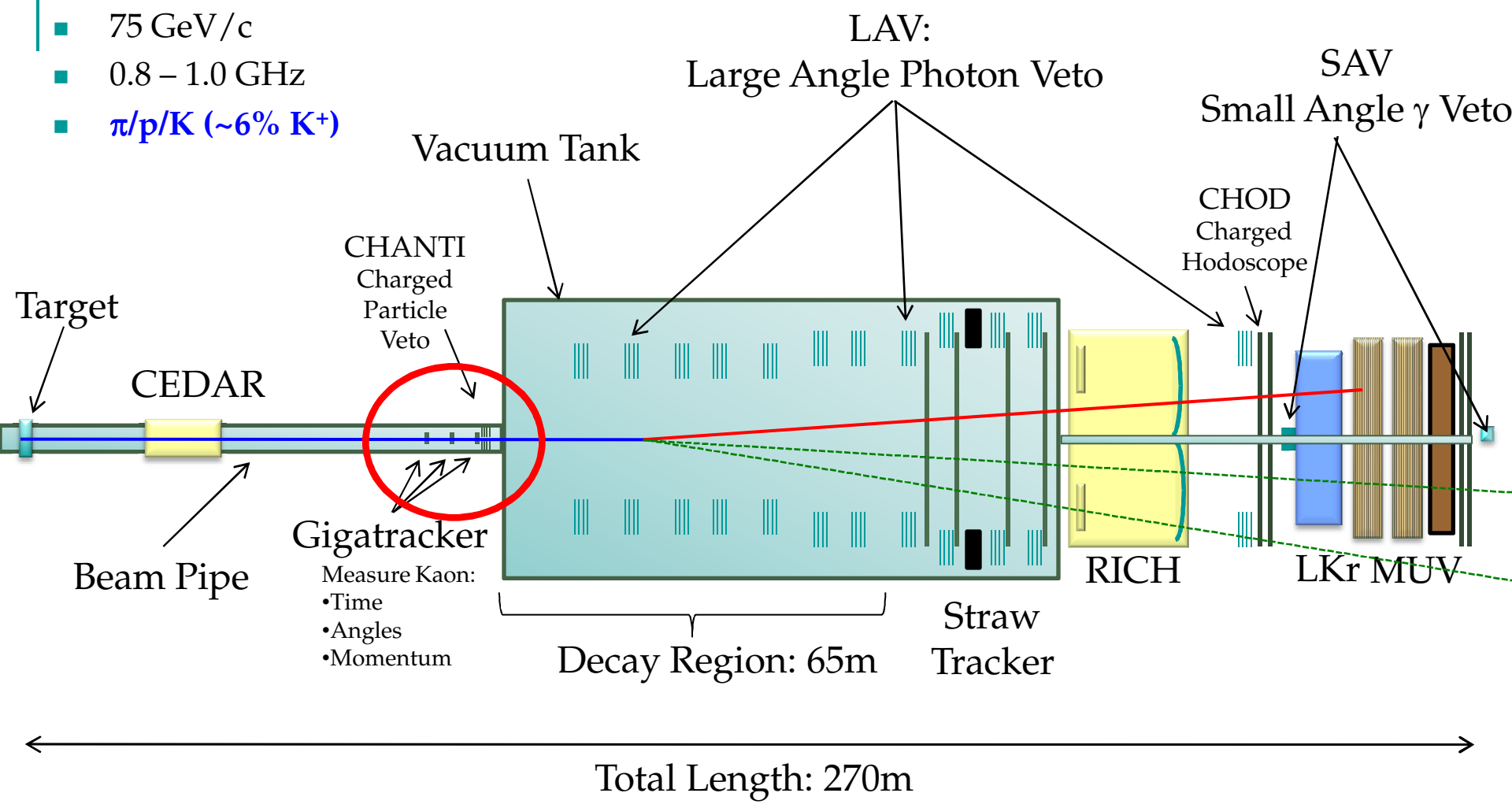
- Photon vetoes to reject $K^+ \to \pi^+\pi^0$
  - $p(K^+) = 75$ GeV/c
  - Requiring $p(\pi^+) < 35$ GeV/c
  - $p(\pi^0) > 40$ GeV/c

  It can hardly be missed in the calorimeters
- PID for $K^+ \to \mu^+\nu$ rejection

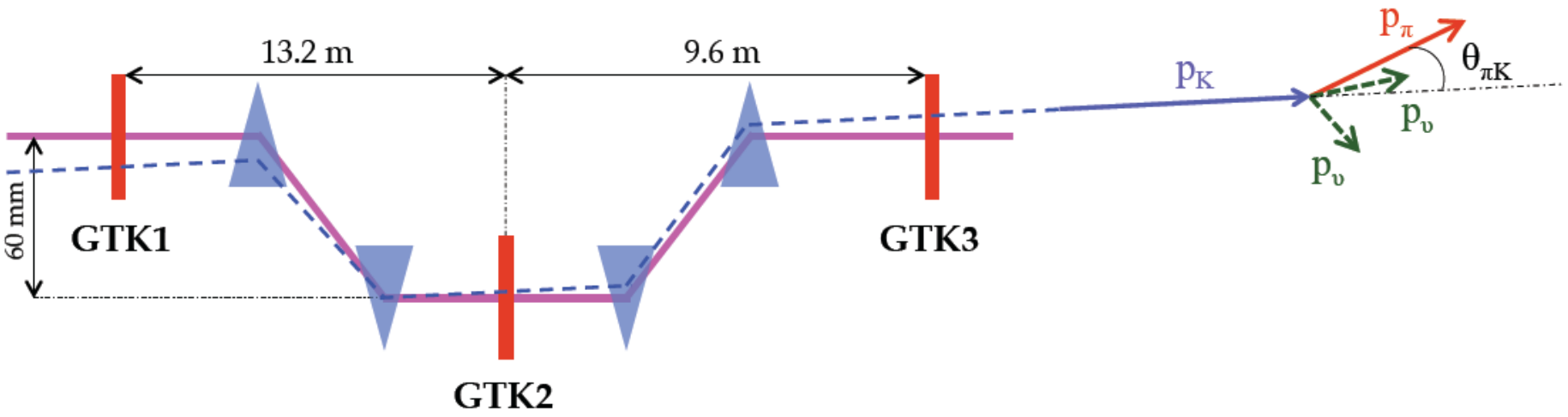


NA62 detector layout

- Un-separated hadron beam
- 75 GeV/c
- 0.8 – 1.0 GHz
- **π/p/K (~6% K⁺)**



The GigaTracKer (GTK)

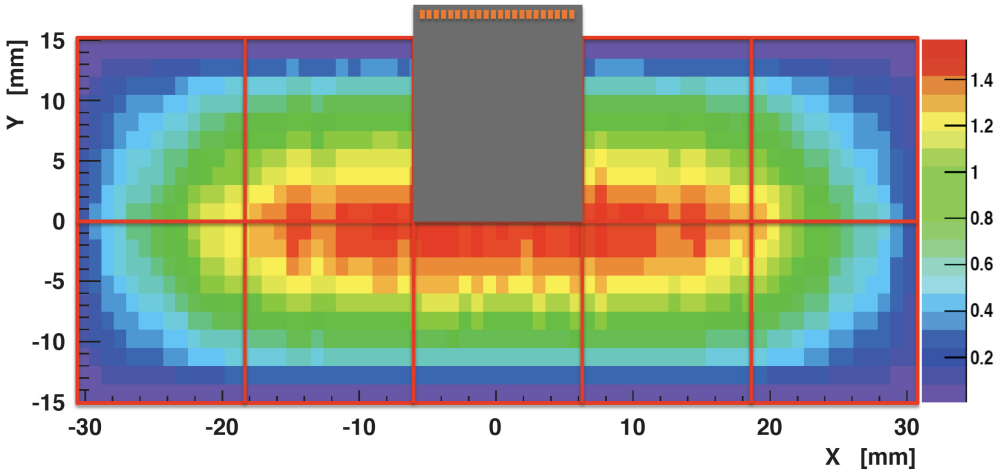


- Beam spectrometer
  - provide precise momentum, time and angular measurements on all beam tracks
  - sustain high and non-uniform rate (~1.5 MHz/mm^2 in the center, 0.8-1.0 GHz total)
  - preserve beam divergence for precise momentum and angular downstream measurements and limit beam hadronic interactions

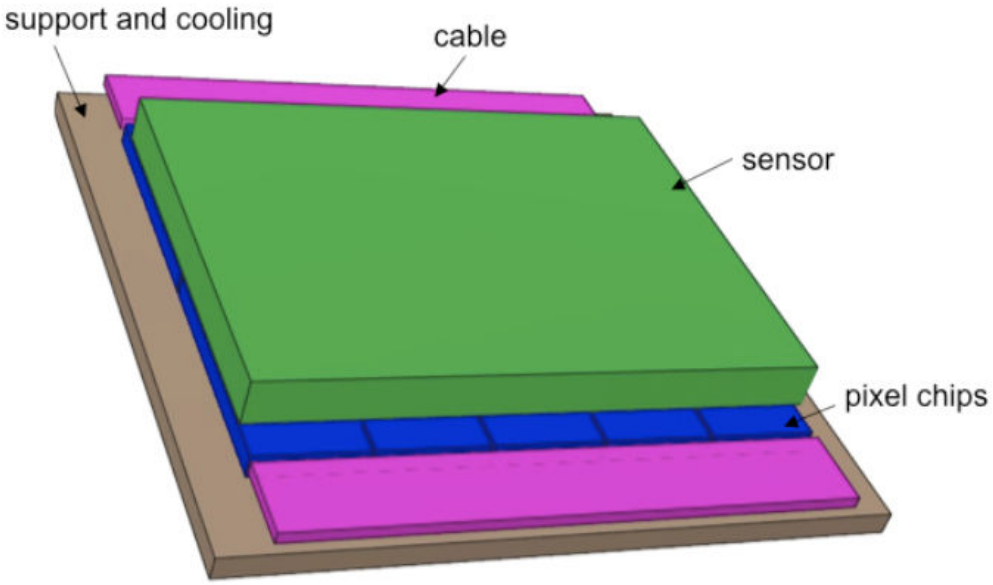
- X/X_0 ~0.5% per station
- $\sigma(p_K)/p_K$ ~0.2%
- $\sigma(\theta_K)$ ~16 μrad
- pixel size 300 μm × 300 μm
- **σ(t) ~150 ps (rms)** on single track

Material budget

- Gigatracker: three hybrid silicon pixel detector stations
- Material budget:
  - 200 μm sensor + 100 μm read-out chip → 0.32% X_0
  - Bump bonds (Pb-Sn) ≈ 0.01% X_0
  - mechanical support and cooling (baseline assumption: 100 μm carbon fiber) ≈ 0.1% X_0
  - [redacted] < 0.5% X_0
- Mi[redacted]zation of material in the[redacted] 27 mm² active beam are[redacted]iformity)
  - [redacted] profile adapted: two [redacted] of read-out chips
  - [redacted] connections to r-o [redacted] outside active area

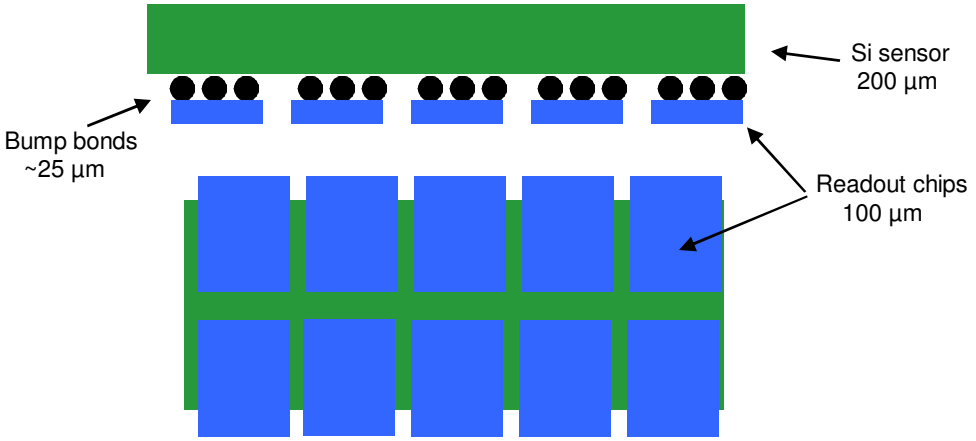


Gigatracker assembly



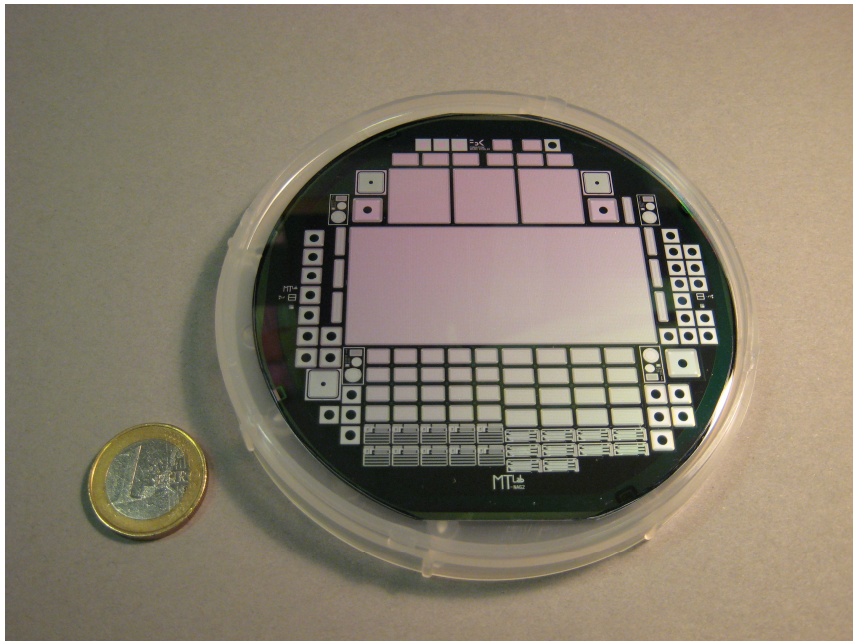
- hybrid pixel detector
- 1 sensor (60 × 27 mm^2)
- 10 read-out chips (12 × 13.5 mm^2 on sensor)
- 40 columns with 45 pixels each (1800 pixels/chip)
- 18k pixels per station

- interconnections through bump bonds
- readout wafers target thickness: < 100 μm (material budget)



Sensors

- standard p-in-n sensors
- 200 μm sensor wafers thickness
- over-depleted operation of the detector required to achieve target time resolution of 200 ps (rms) per GTK station
  - total charge collection time less than 6 ns can be achieved with over-depletion voltage of at least 200 V
- sensor processing at FBK-irst (Trento, Italy)
- a few 4" wafers already delivered
- wafers contain final-size sensor (60 mm × 27 mm) plus prototype sensors and other test structures
- flip-chip bonding of prototype sensors in spring 2010

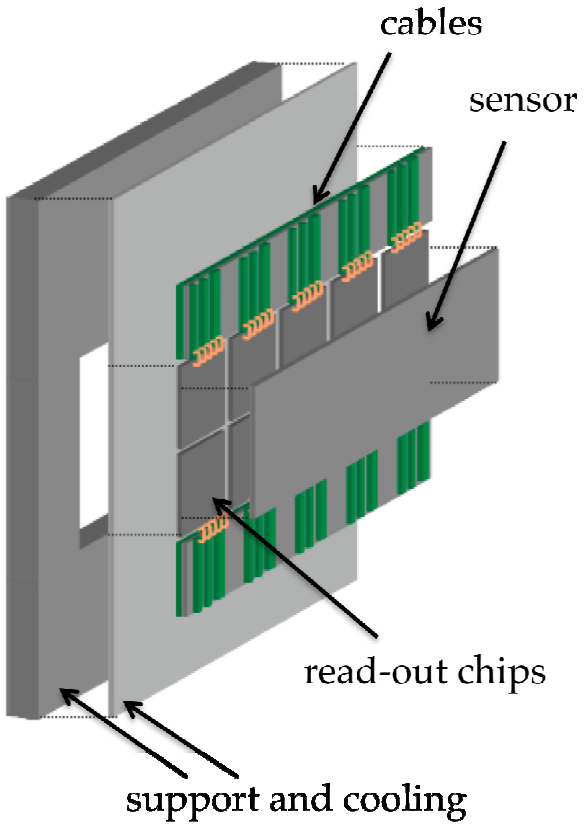


Operating environment

- GTK planes will be mounted inside vacuum to avoid additional material in the beam path
- High radiation levels: severe challenge to sensor lifetime
  - assuming 100 running days per year, the expected fluence is ~2×10^{14} (1 MeV n_{eq}/cm^2) during one year physics run
    → comparable to those expected in inner layers of the LHC trackers during 10 years of operation
- Irradiation tests performed on prototype p-in-n diodes with protons and neutrons, in addition to annealing measurements (I-V, C-V) following expected run scenario
- Radiation environment and low detector mass will require efficient cooling
  - keep radiation induced leakage current (most critical parameter) at acceptable value for stable operation

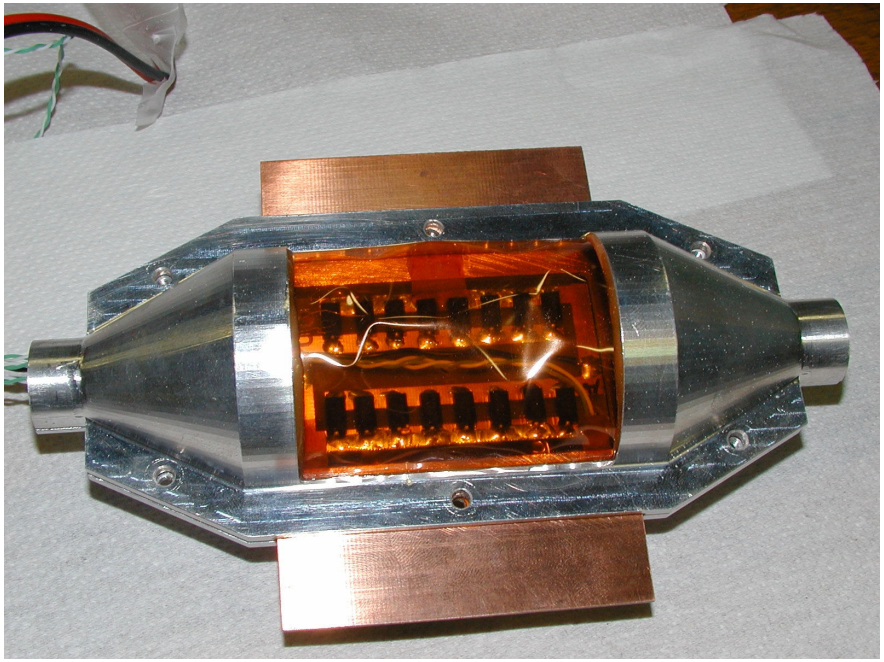
Cooling system

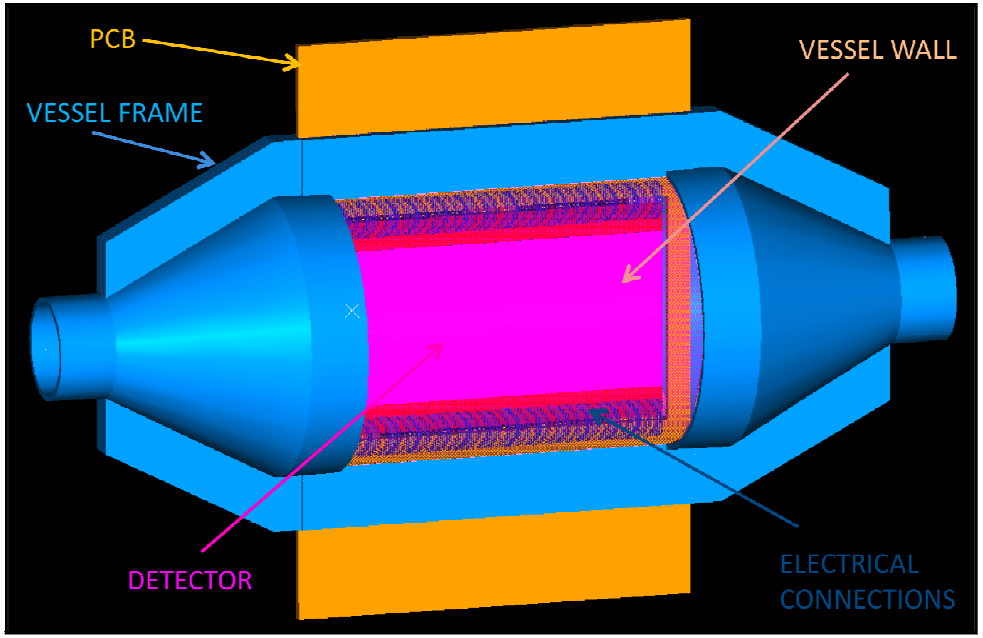
- Sensor operating temperature lower than 5 °C to limit leakage current increase induced by radiation damage
  - uniform temperature distribution across the sensor area
- Dissipated power by read-out chips is ~2 W/cm^2 (corresponds to ~32 W per Gigatracker station)
- Low material budget (**~0.15% X_0**) in the beam region
- Operation in vacuum
- Cooling options under study:
  - convective cooling in a vessel
  - micro-channel cooling



Vessel cooling

- cooling via flow of cold gaseous nitrogen (100 K)
- thin cylindrical kapton windows (50 μm thick)
- aluminum vessel frame

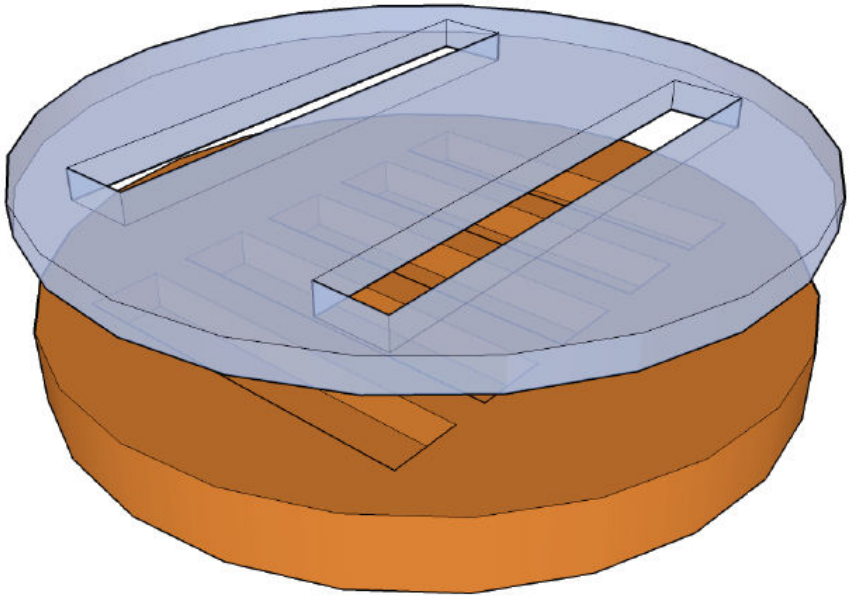


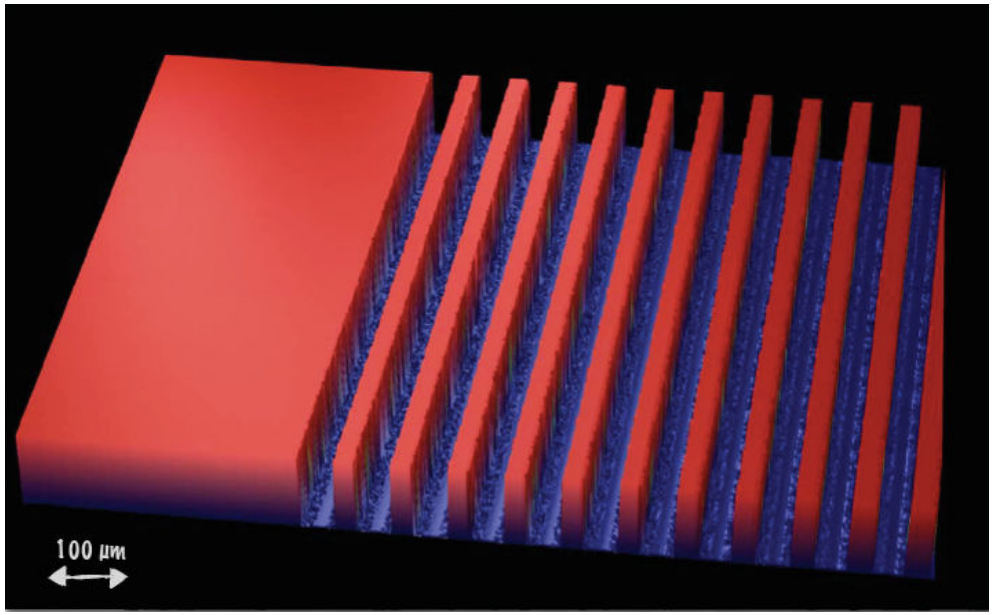


- good uniformity of temperature distribution across sensor area (thermal analysis simulation)
- full size prototype has been built and is being tested

Micro-channel cooling

- micro-channel cooling plate: 2 bonded Si wafers (150 μm total thickness)
  - channels etched into 1st
  - opening for inlet and outlet manifolds in the 2nd

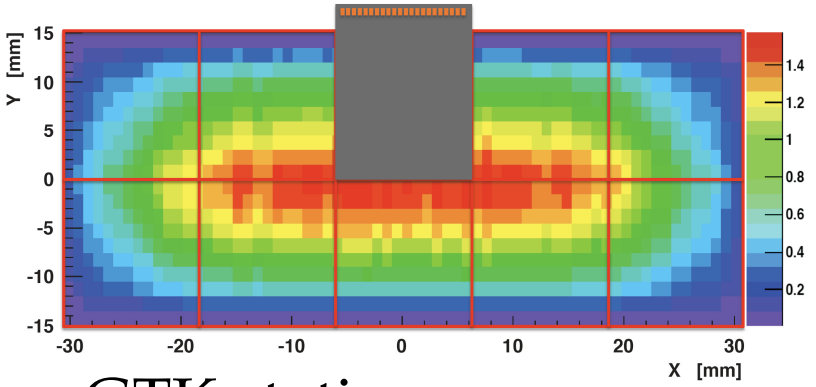




- 50 μm × 50 μm micro-channels
- rad-hard liquid coolant (C_6F_{14})
- a first prototype based on Si-Pyrex bonding has been built and a complete test stand is under construction

Read-out electronics

- 2×5 read-out chips (0.13 μm CMOS technology)
- 40 columns with 45 pixels each (300 μm × 300 μm pixel)
- Chip size: 12 mm × 18-19 mm
- Maximum particle rate per pixel: 140 kHz
- Dissipated power produced by chip ~2 W/cm^2 (32 W total)
- Dynamic range:
  5000 to 60000 electrons

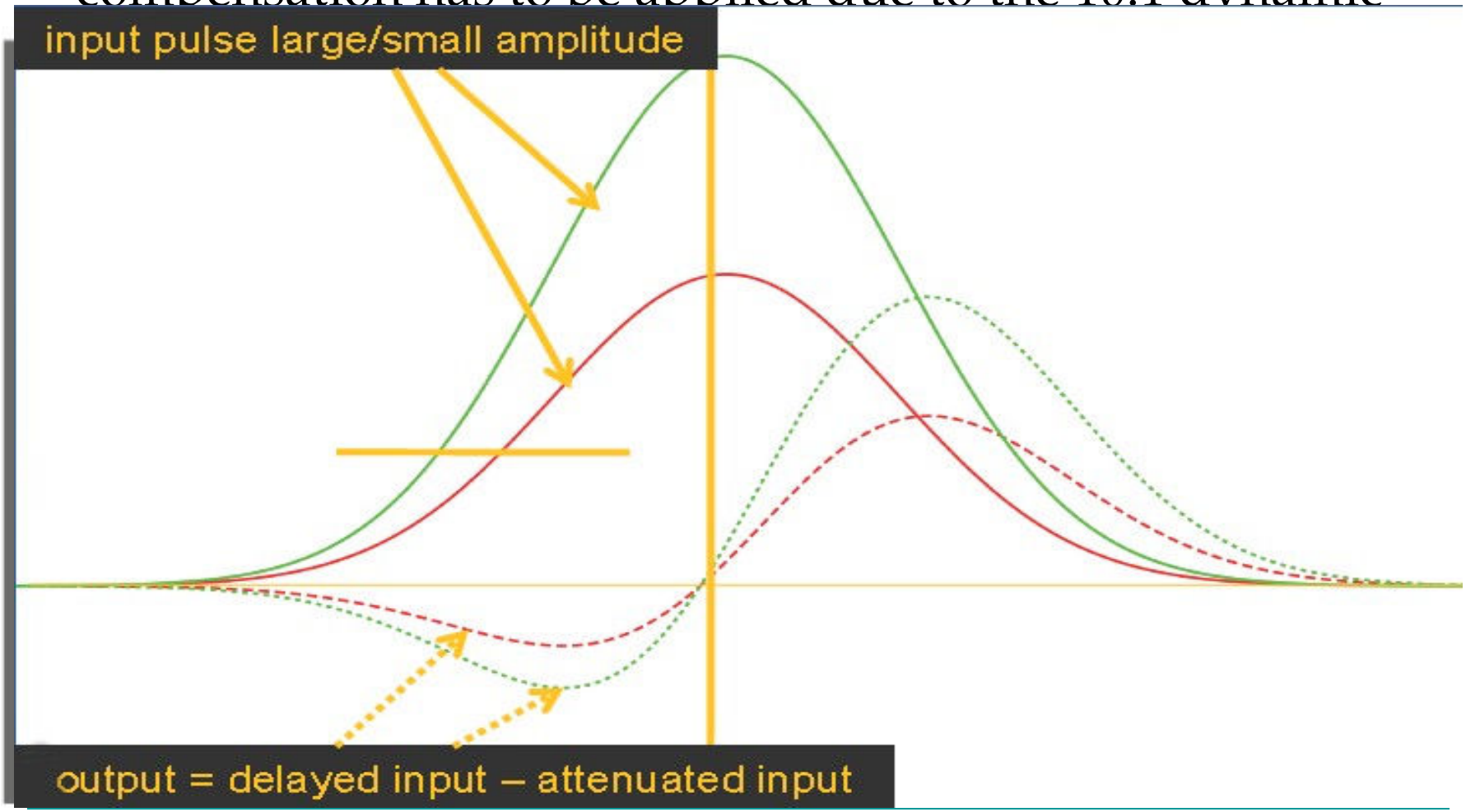


Key challenges:

- Time resolution: 200 ps (rms) per GTK station
- On-pixel fast analog pulse shaping (~4 ns peaking time)
- Maximum data rate per chip: up to 6 Gbit/s

Time-walk correction

- To achieve the required timing accuracy, time-walk compensation has to be applied due to the 10:1 dynamic



TDC options

- Coarse time measurement by counting clock pulses
- Fine measurement obtained with a Time to Digital Converter (TDC)

Two possible solutions:

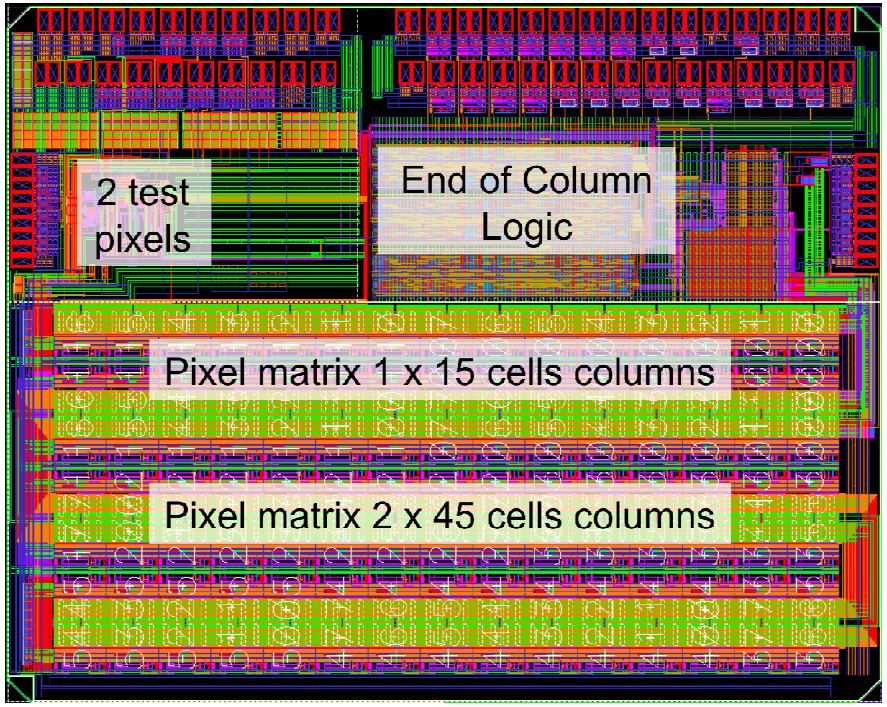
- On-pixel TDC system
  - maximize signal processing on the pixel cell (including TDC) and distribute clock to the pixel matrix (digital noise)
  - minimize complexity of end of column logic (no need to propagate the comparator signal outside the pixel)
  - must be designed to be radiation-tolerant (total dose and SEU aspects), due to the high radiation dose received in the pixel area
- End of Column (EoC) architecture
  - use high precision digital TDC in the end of column, shared by a group of pixels
  - minimize on-pixel processing for minimum noise
  - pixel comparator signals should be propagated to the chip periphery (communication of ultra-fast signal in column transmission lines)

Read-out architectures

- Two different architectures for the GTK read-out chip are under development:
  - Time-walk correction using a CFD filter + on-pixel TDC based on TAC (Time-to-Amplitude Converter) → "On-pixel TDC" option
  - Time-walk correction using ToT technique + DLL based TDC shared among a group of pixels → "End of Column (EoC)" option
- Small area prototype chips (for both architectures) have been submitted in March 2009 (MPW run) in order to investigate and compare their relative performances
- In summer 2009 the chips were delivered and tests have started in the following months

On-pixel TDC option

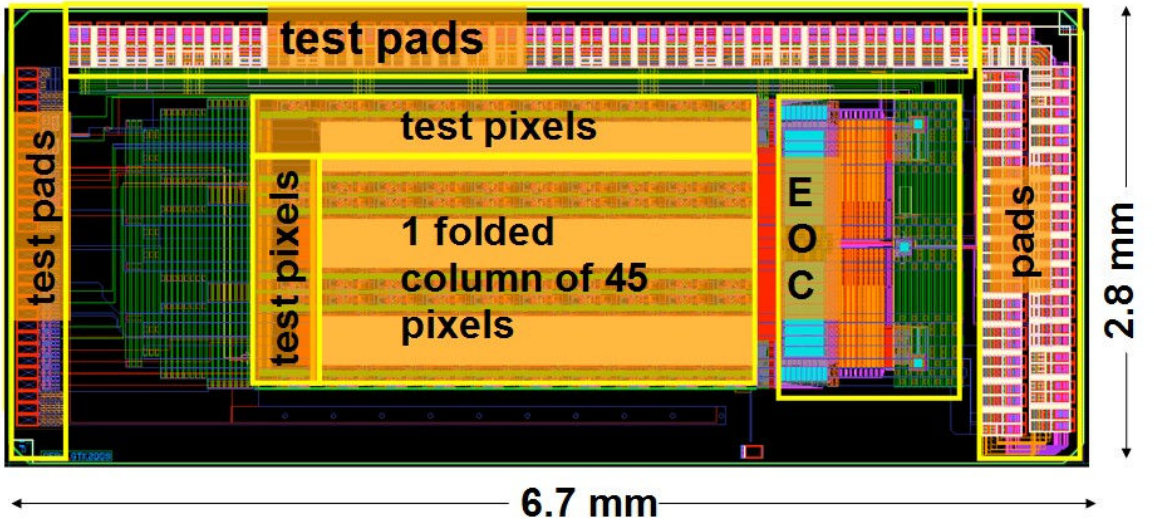
- 5 mm × 4 mm total size
- 105 + 2 pixel cells
- 160 MHz clock
- 2 folded columns (45 pixels each) and one smaller column with 15 pixels, plus two test pixels
- For each column a totally independent End-of-Column Controller is implemented



- SEU protection both in the pixel cells and the End of Column controller
- Fine time measured by starting calibrated voltage ramp at CFD rising edge and stopping at next clock rising edge
- Prototype tests are ongoing (results available soon)

EoC option

- 2.8 mm × 6.7 mm total size
- 320 MHz reference clock
- 60 pixels divided into 3 groups
- Main array: 45 pixels with 9 EoC readout blocks, each one serving the 5 pixels through the arbiter block
- Small array: 9 pixels
- Test column: 6 pixels with analog output
- Hit Arbiter: defines first arriving pixels out of 5 (asynchronous latch)
- Preliminary results from chip testing are available (next slide)



EoC prototype chip tests

- TDC qualification
  - 250 MHz DLL operation (stable)
    - 125 ps binning (LSB)
  - RMS differential non-linearity < 0.2 LSB
  - RMS integral non-linearity < 0.2 LSB
  - Bin width uniformity ~0.15 LSB
- Analog front-end measurements
  - noise 56 e^-
  - jitter <100 ps @ 3 fC (mean charge released by m.i.p.), with threshold set to 0.7 fC
- Important tests still to be done
  - full chain characterization
  - tests with sensor after flip-chip bonding

R&D program

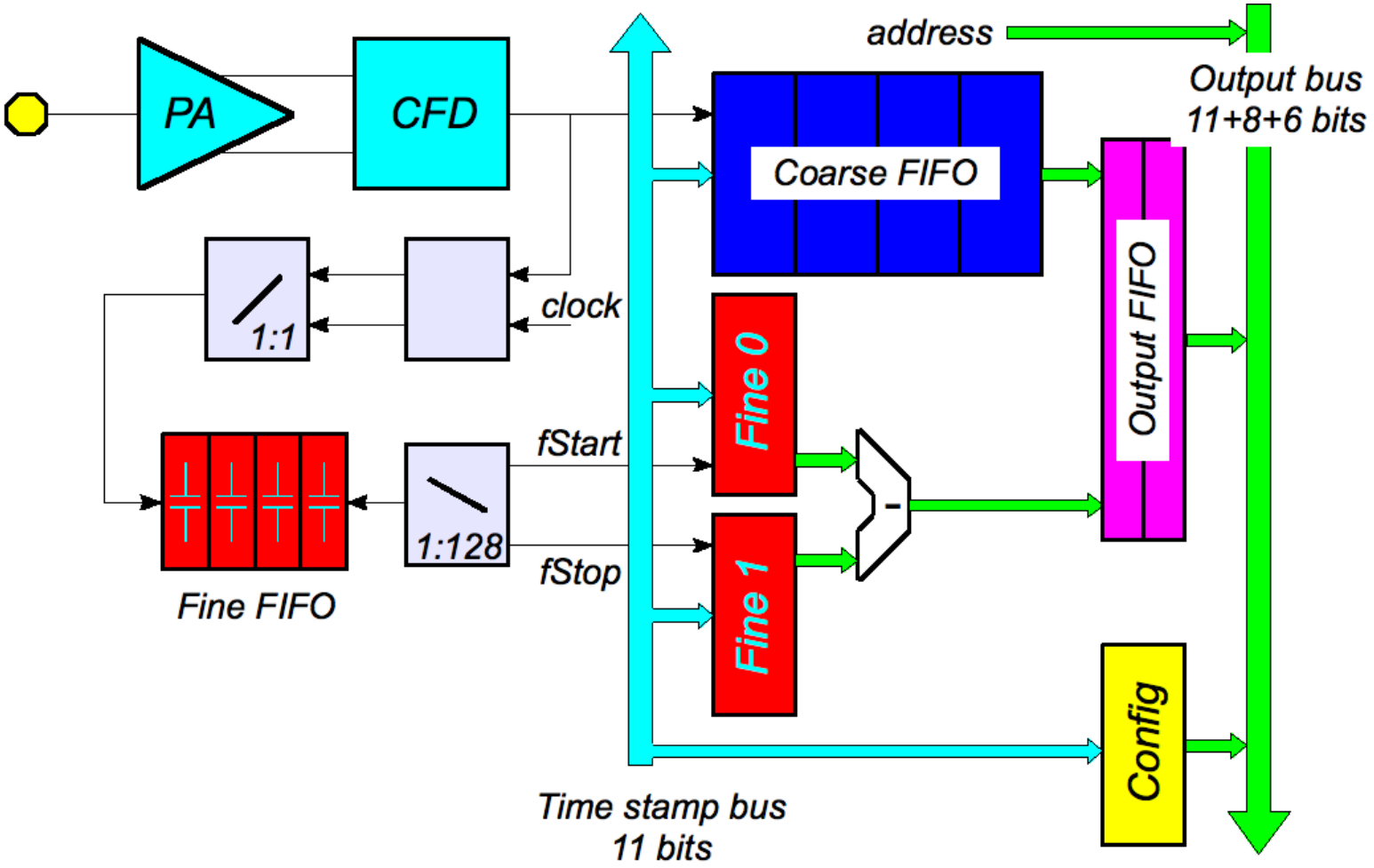
- Completion of prototype chip tests
- Flip-chip bonding to prototype sensors
- Prototype assemblies tests with laser and hadron beams
- Choice on the read-out architecture
- Design of the final read-out chip
- Validation of cooling solution
- Production of final assemblies with thinned read-out chips
- Production of complete read-out electronics and cooling systems (full integration)
- Installation in the NA62 beamline and data taking

Conclusions

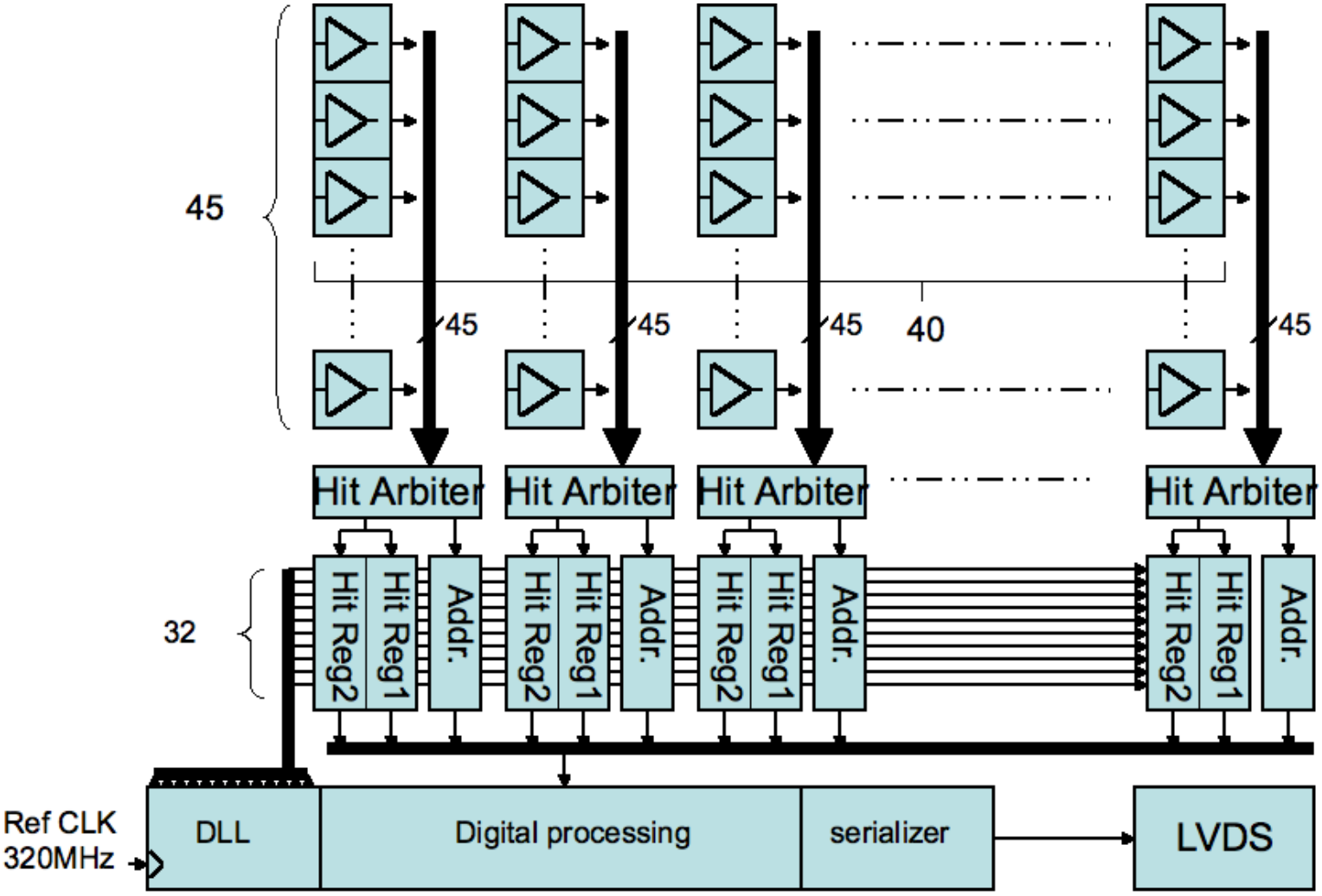
- The Gigatracker is a very challenging detector due to the time resolution requirement (150 ps rms for single track) and the high particle rate
- An efficient and low mass cooling system (~0.15% X_0) must be developed to limit radiation induced leakage current and ensure stable detector operation
- Two complementary read-out architectures have been designed and implemented in 0.13 μm CMOS technology
  - Preliminary tests on one read-out chip are very promising

SPARES

On-pixel TDC


address
Output bus
11+8+6 bits
PA
CFD
Coarse FIFO
Output FIFO
1:1
clock
Fine 0
fStart
1:128
fStop
Fine 1
Fine FIFO
Config
Time stamp bus
11 bits

EoC TDC


45
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Hit Arbiter
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32
Hit Reg2
Hit Reg1
Addr.
Hit Reg2
Hit Reg1
Addr.
Hit Reg2
Hit Reg1
Addr.
Hit Reg2
Hit Reg1
Addr.
Ref CLK
320MHz
DLL
Digital processing
serializer
LVDS