KEK Season's Greetings and Best Wishes for the New Year.

Development of SOI Pixel Detectors

Feb. 17, 2010@VCI2010
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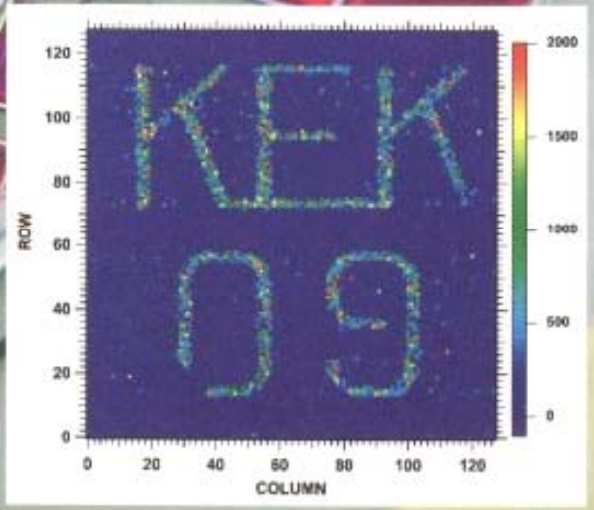
http://rd.kek.jp/project/soi/



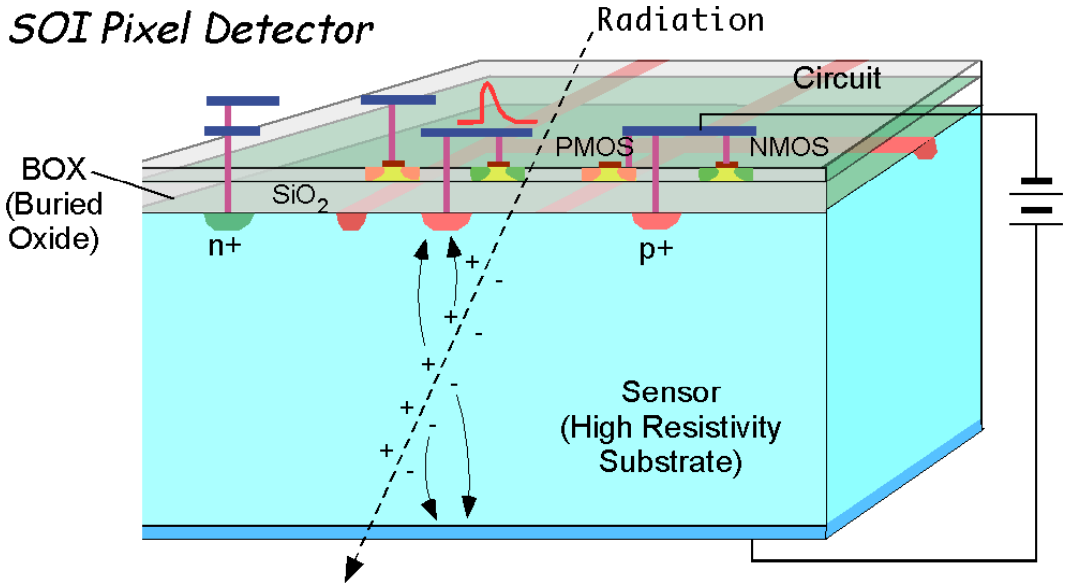
SOI wafer and an image obtained by a pixel detector

OUTLINE

1. Introduction of SOI Pixel
2. New Process Developments
   - Buried P-Well Technology
   - Vertical Integration
3. MPW run and Pixels
4. Summary

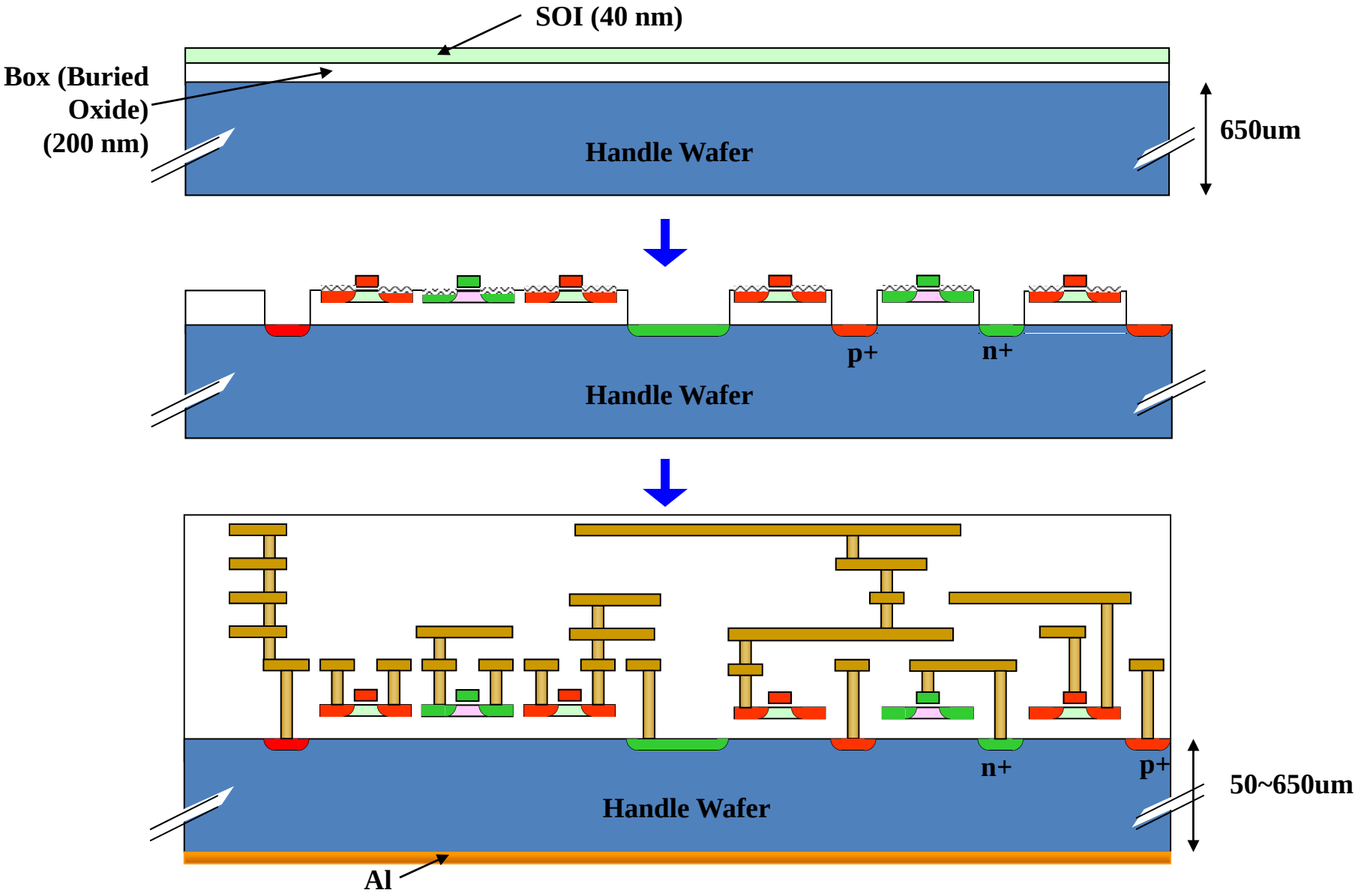
1. Introduction

Monolithic detector using Bonded wafer (SOI : Silicon-on-Insulator) of Hi-R and Low-R Si layers.



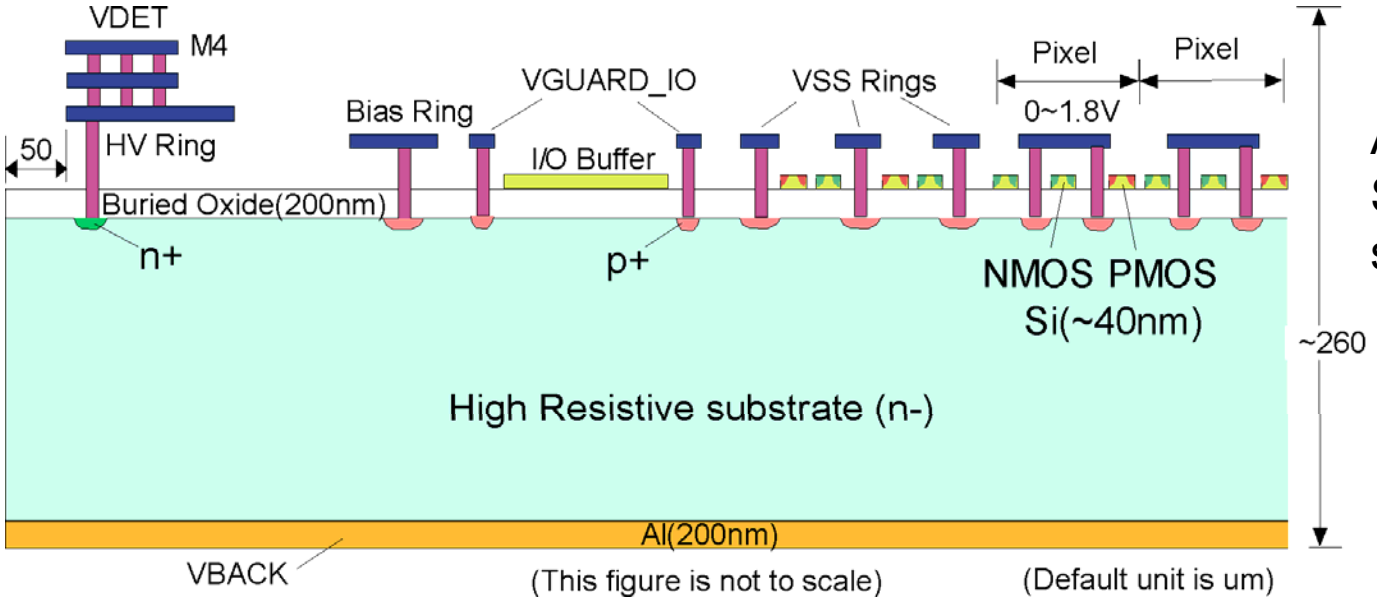
- No mechanical bump bondings
  - -> High Density, Low material budget
  - -> Low parasitic Capacitance, High Sensitivity
- Standard CMOS circuits can be built
- Thin active Si layer (~40 nm)
  - -> No Latch Up, Small SEE Cross section.
- Based on Industrial standard technology
- Seamless connection to Vertical Integration

SOI Pixel Process Flow



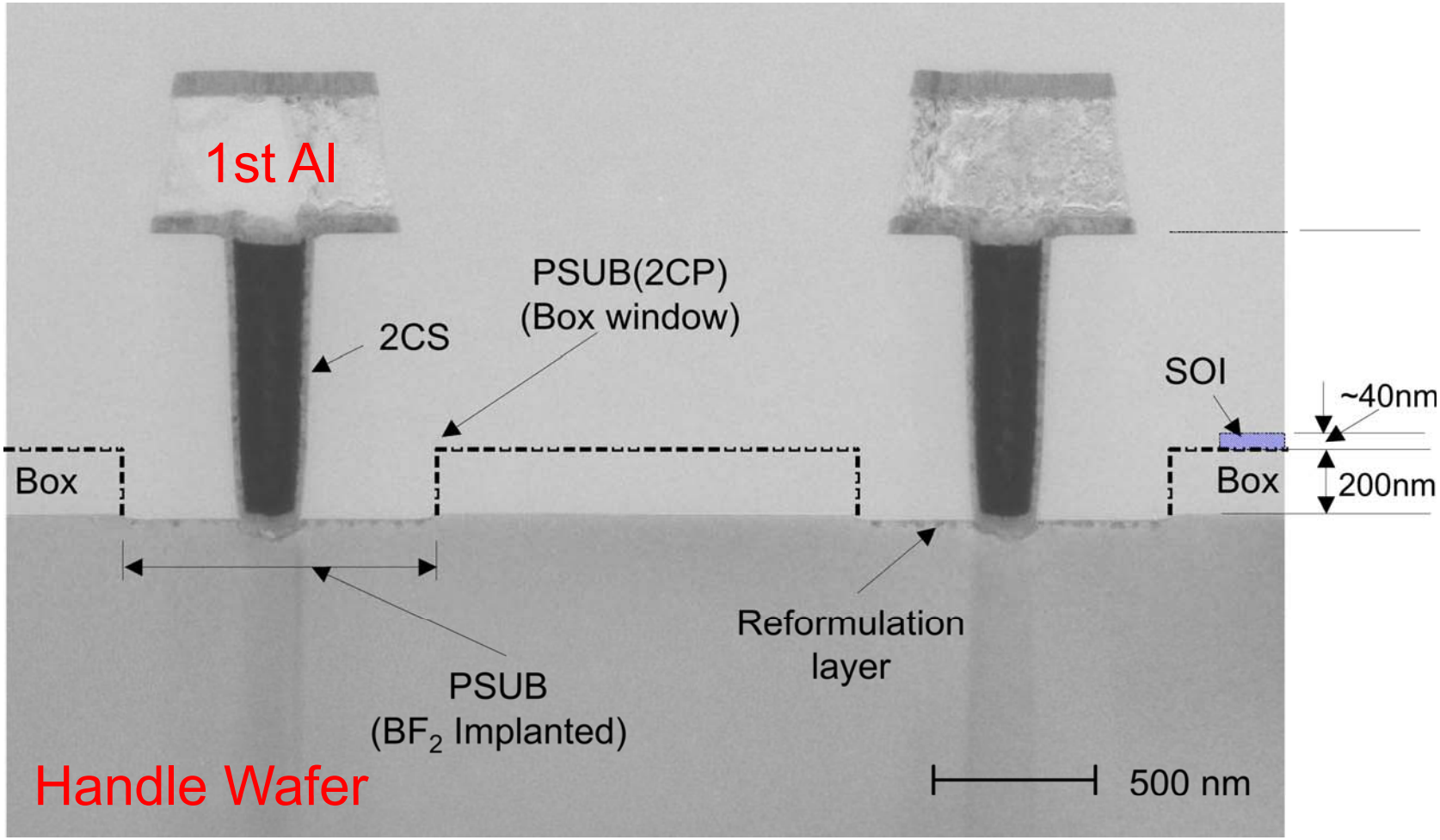
OKI 0.2 μm FD-SOI Pixel Process

Process	0.2μm Low-Leakage Fully-Depleted SOI CMOS (OKI) 1 Poly, 4 (5) Metal layers, MIM Capacitor, DMOS option Core (I/O) Voltage = 1.8 (3.3) V
SOI wafer	Diameter: 200 mmϕ, Top Si : Cz, ~18 Ω-cm, p-type, ~40 nm thick Buried Oxide: 200 nm thick Handle wafer: Cz、 700 Ω-cm (*n-type)*, 650 μm thick
Backside	Thinned to 260 μm, and sputtered with Al (200 nm).

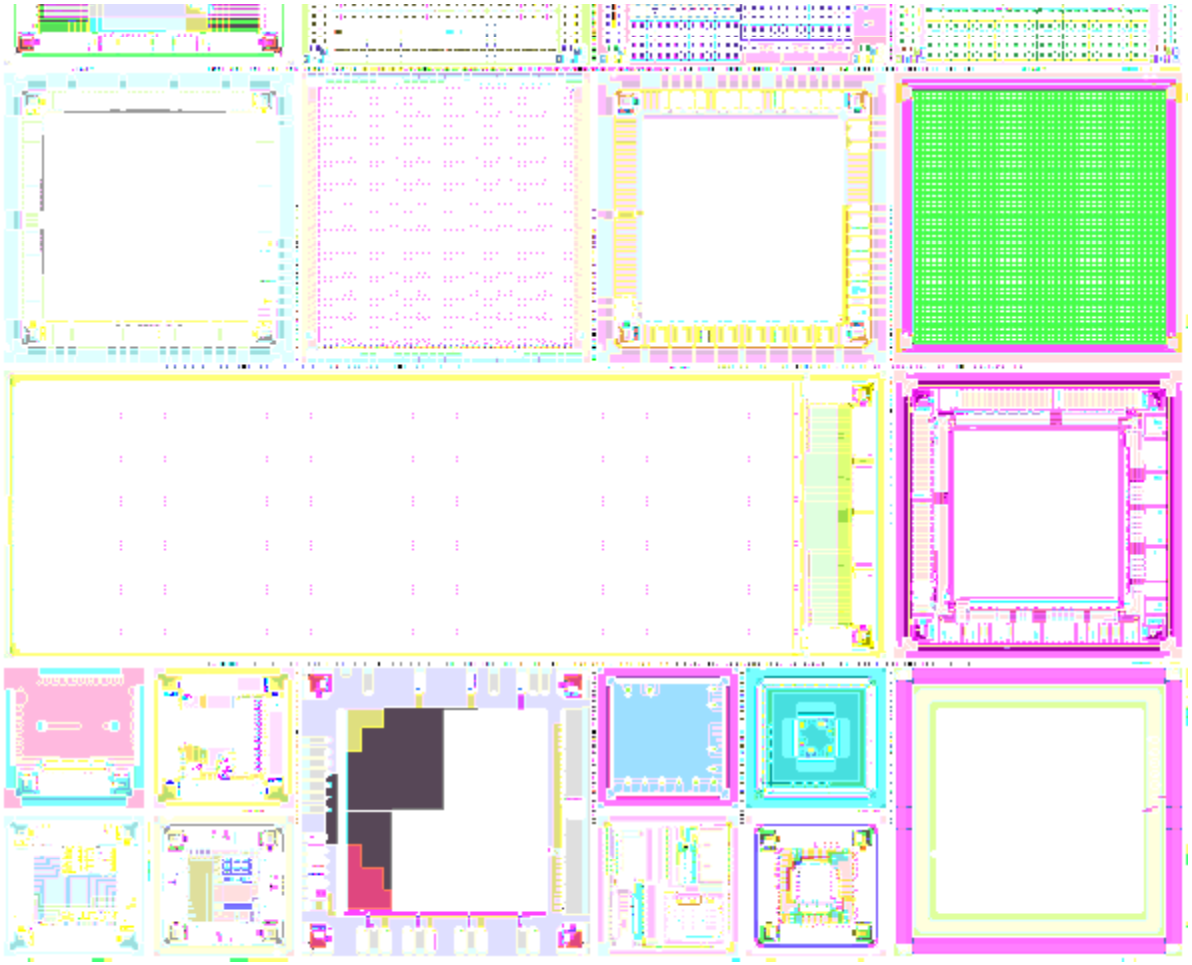


An example of a SOI Pixel cross section

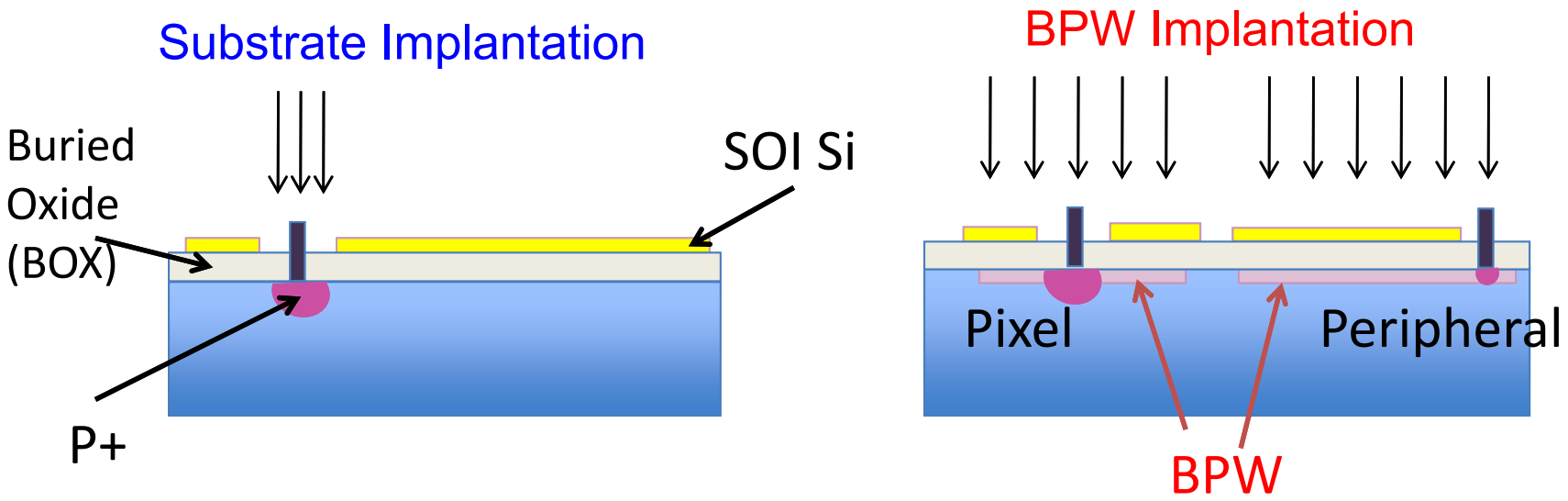
Metal contact & p+ implant



2. New Process Developments



Buried p-Well (BPW) Process



- Cut Top Si and BOX
- High Dose

- Keep Top Si not affected
- Low Dose

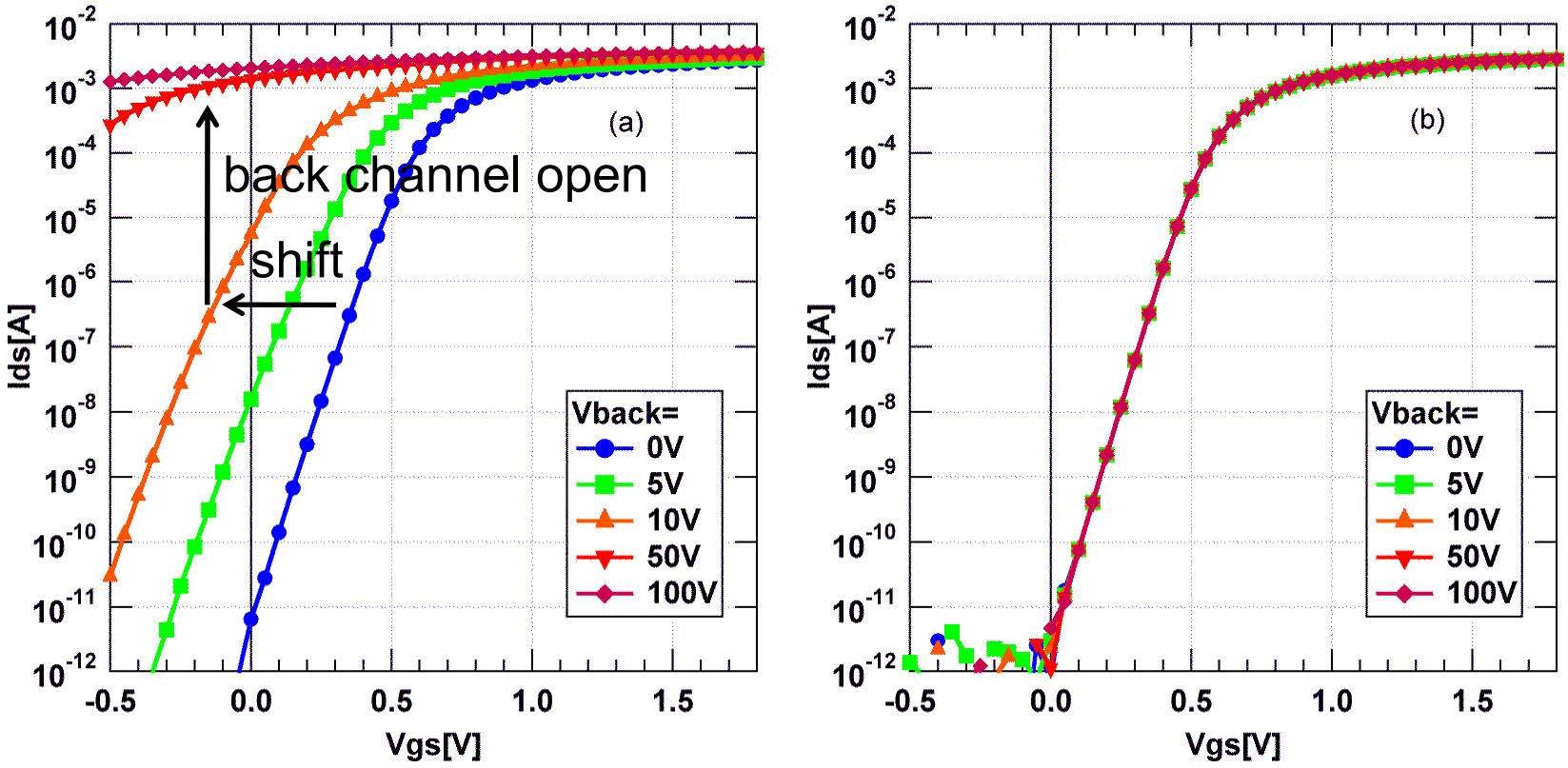
- Suppress the back gate effect.
- Shrink pixel size without loosing sensitive area.
- Increase break down voltage with low dose region.
- Less electric field in the BOX which may improve radiation hardness.

I_d-V_g and BPW

w/o BPW

with BPW=0V

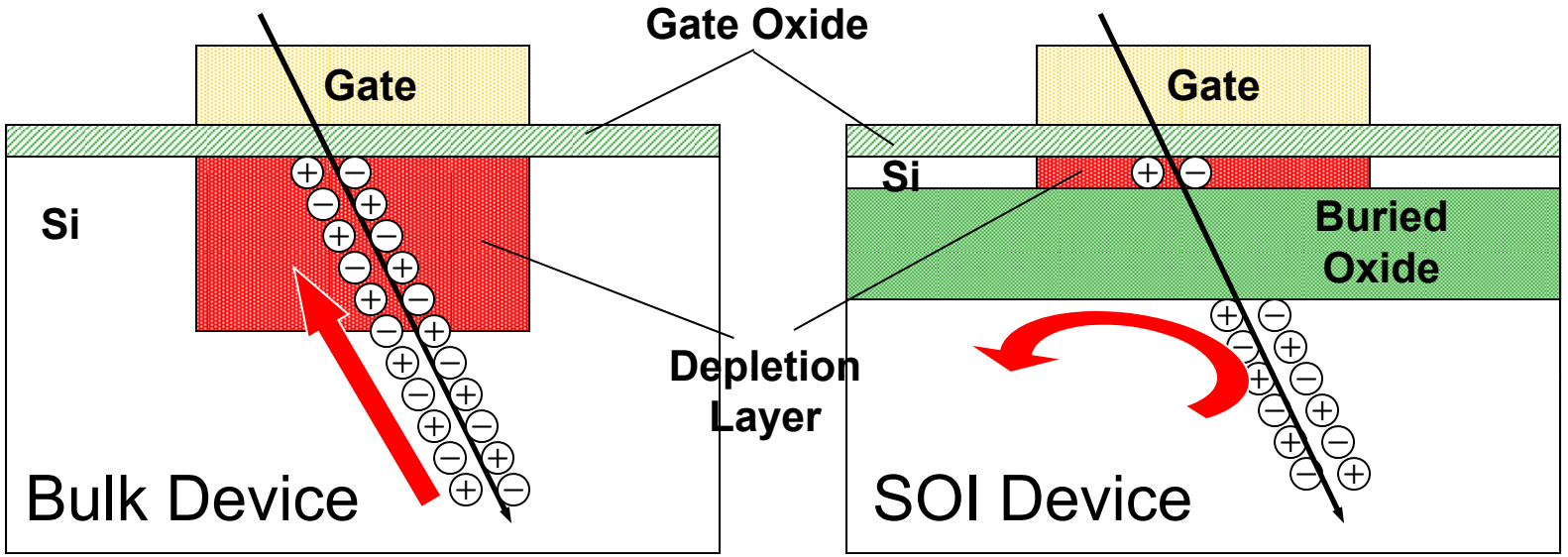
NMOS



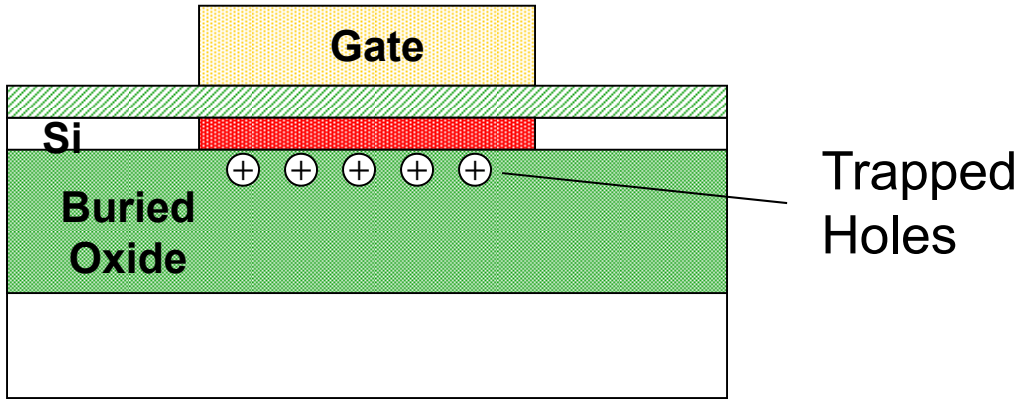
Back gate effect is suppressed by the BPW.

Radiation Tolerance and BPW

SOI is Immune to Single Event Effect



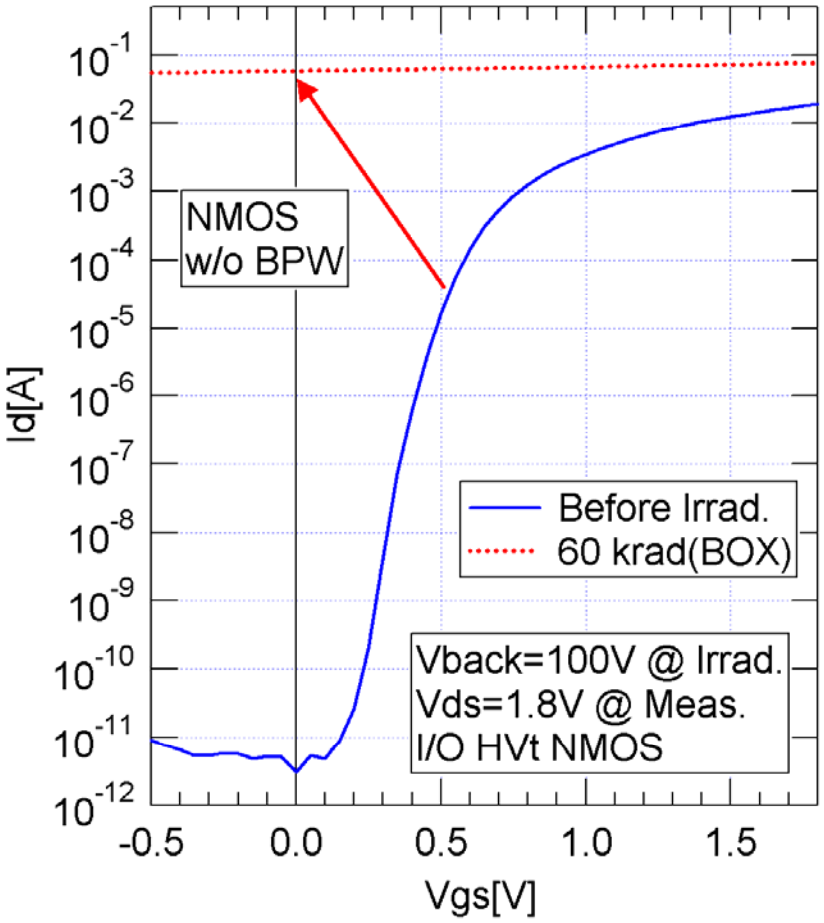
But not necessary strong to Total Ionization Dose due to thick BOX layer

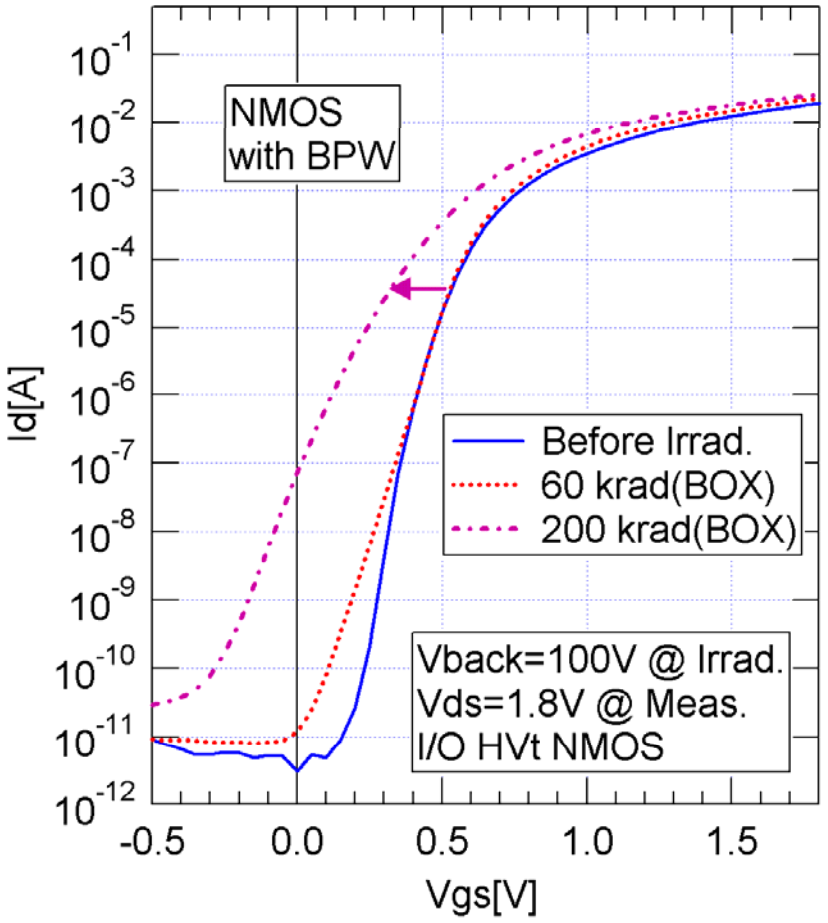


Radiation Tolerance and BPW (cont.)

By adding the BPW layer, Electric field in the BOX is reduced and possibility of charge recombination will increase.

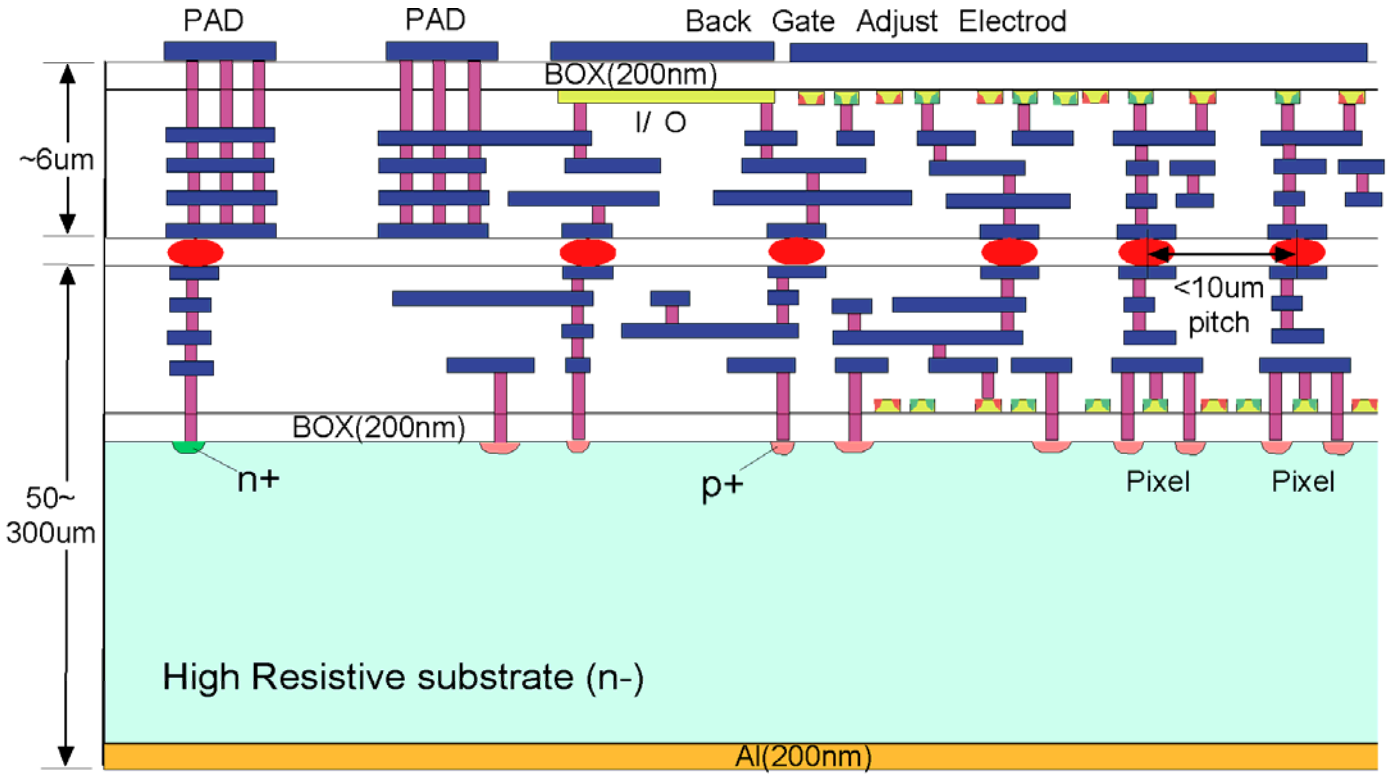
X-ray Irradiation



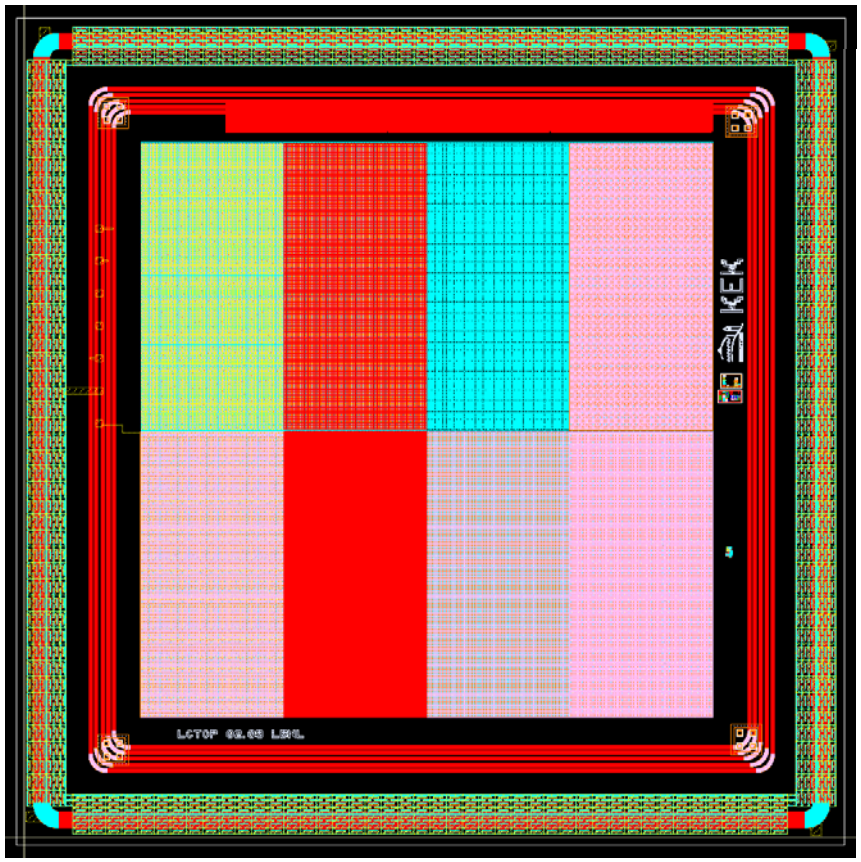


Vertical (3D) Integration

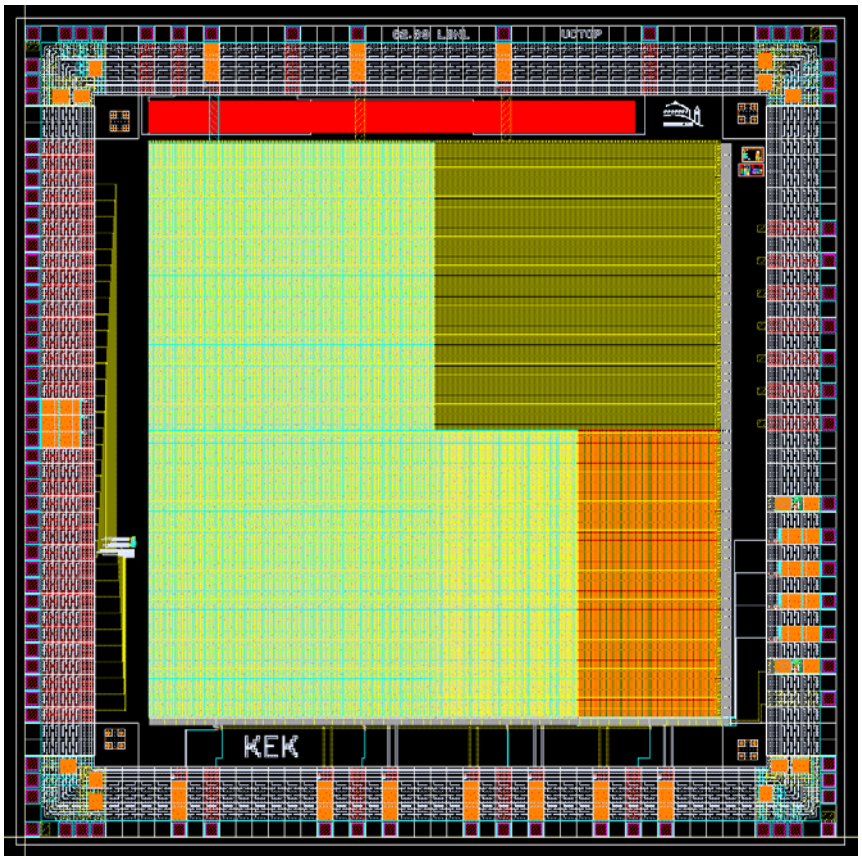
Further Integration by using μ-bump bonding (~5 um pitch) technology of ZyCube Co. Ltd.



SOI Pixel Vertical Integration



Lower Chip



Upper Chip

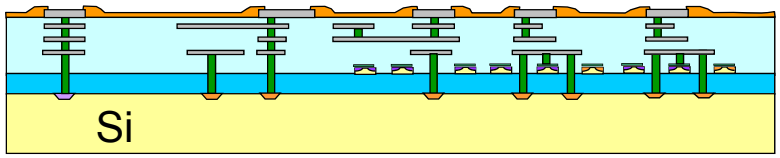
Process Flow for SOI Pixel Detector

OKI SEMICONDUCTOR

ZyCube

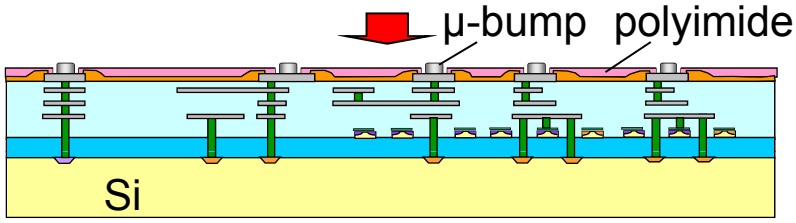
Lower Chip

- Starting LSI



FD-SOI + MIM capacitor +DMOS
1P4M process
Core (I/O) voltage= 1.8(3.3) V
8”Φ SOI Technology
Si :CZ , p-type 18ohm,tsi=40nm
BOX:tSiO2=200nm

- Form μ-bump

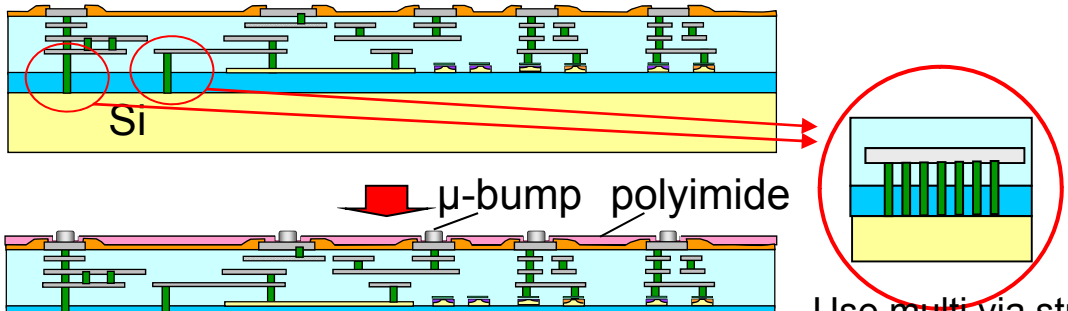


Next page (Stacking)

Upper Chip

(Layout must be done with mirror inverted)

- Starting LSI



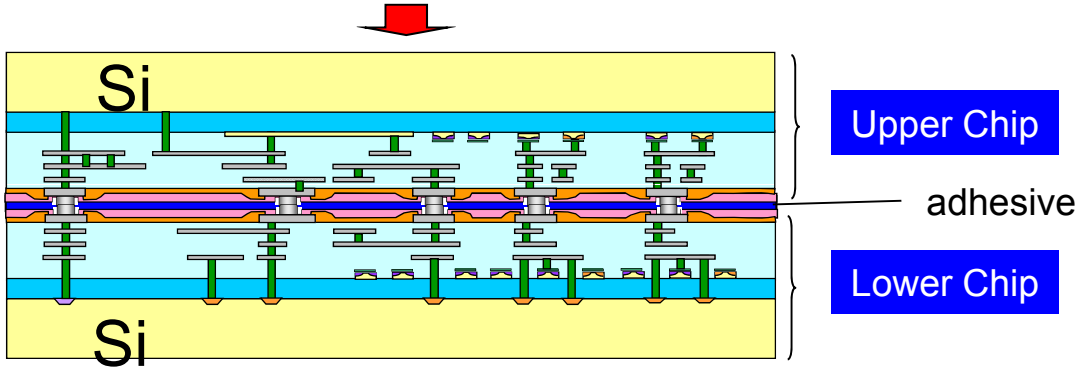
Use multi via structure for contact path between 1metam and bond pad dia./space 0.32/0.6μm
In left figure, single via is used for simplifying the cross section

- Form μ-bump

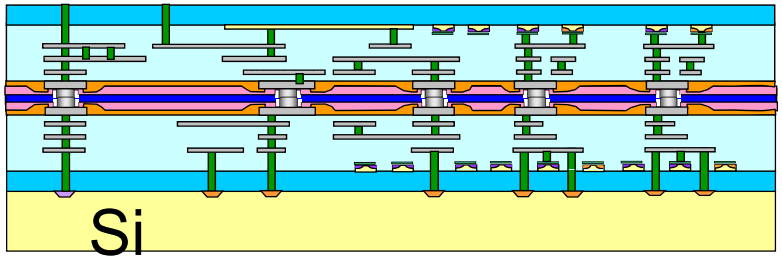
Next page (Stacking)

ZyCube

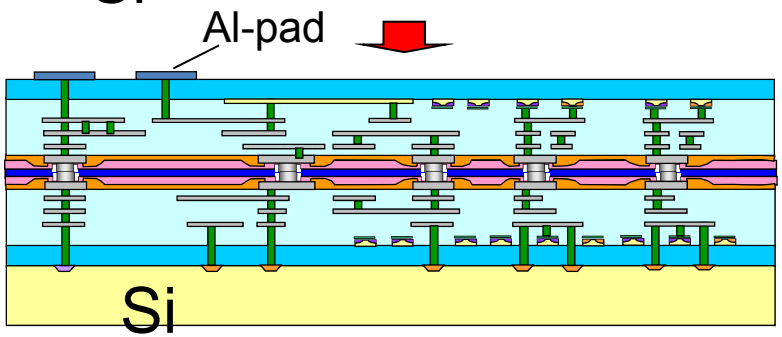
-Stack wafer (Chip) with μ-bump and adhesive



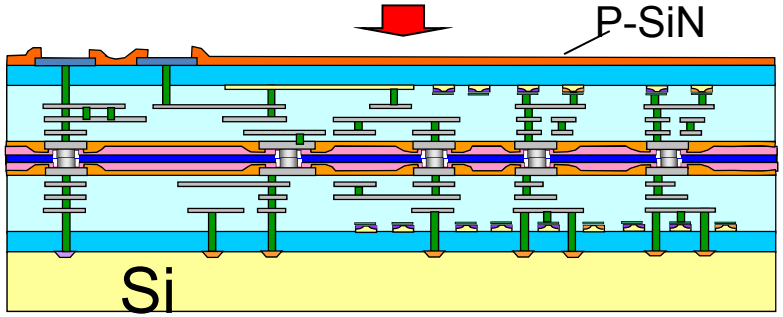
-Si etch
-SiO2 slight etch



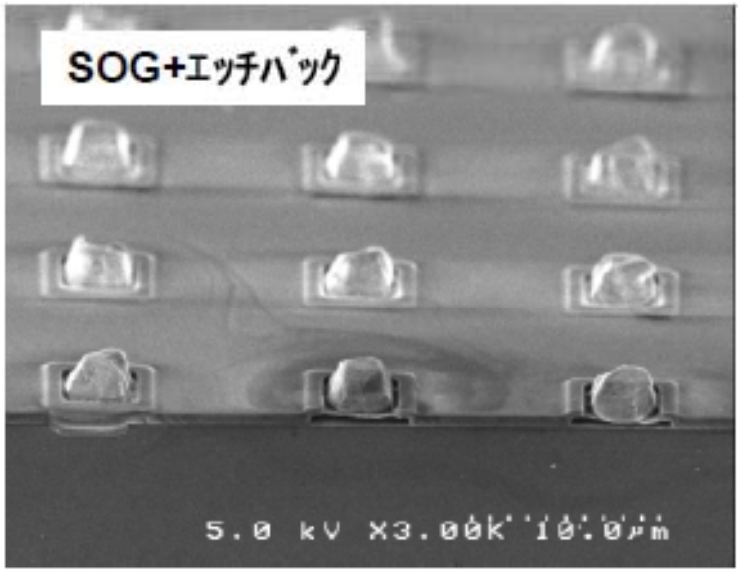
-Ti/TiN/Al sputter
-Metal Pad Litho.

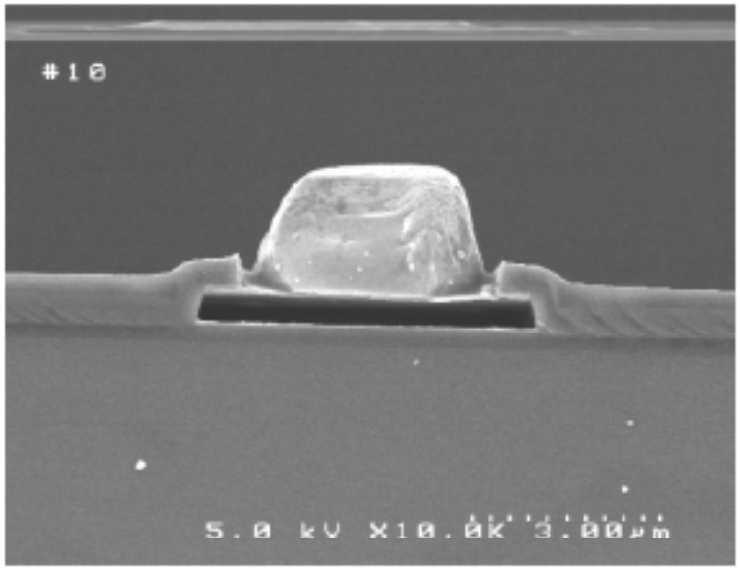


-P-SiN deposition
-Pad Litho.



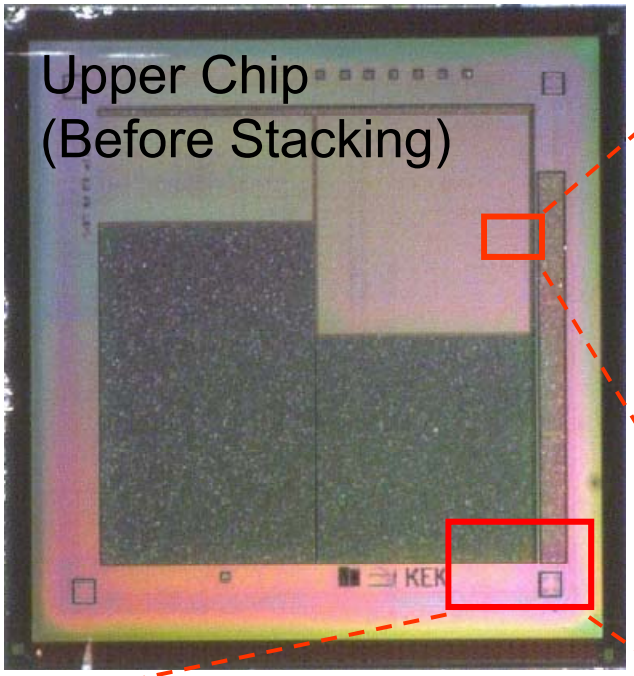
μ-bumps fabrication

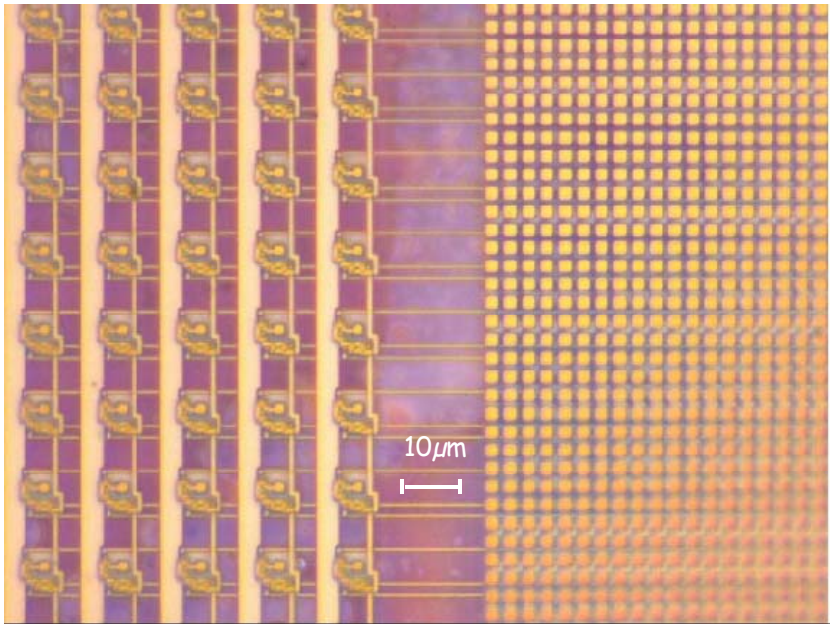




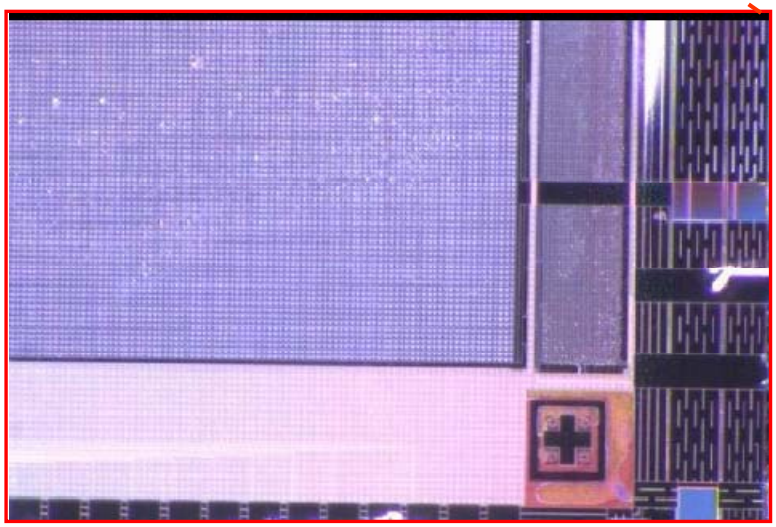
ZyCube

3D-SOI pixel Detector : Stacking



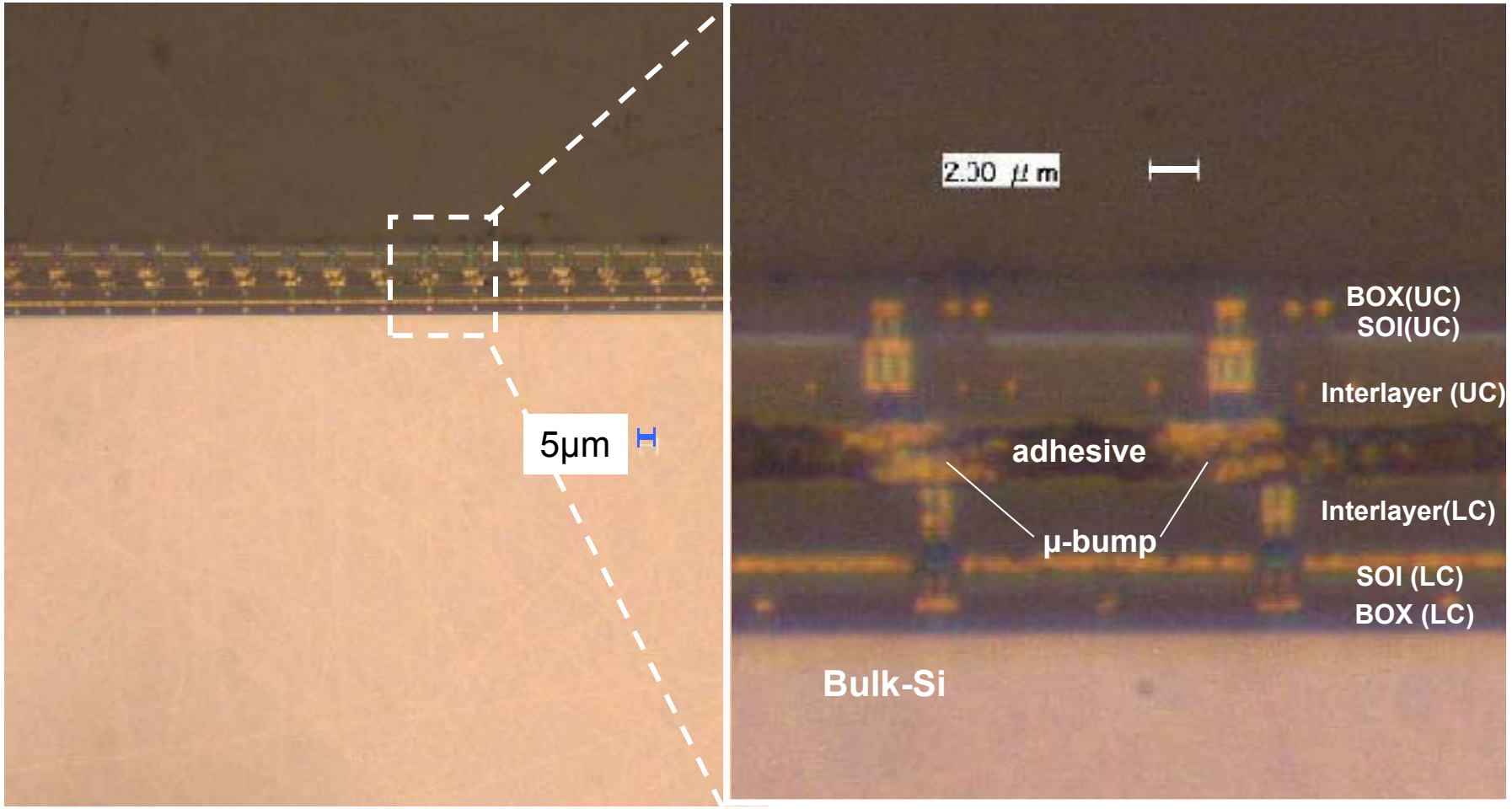


Detector Array +Peripheral Circuits
(After stacking)



Alignment Mark (After stacking)

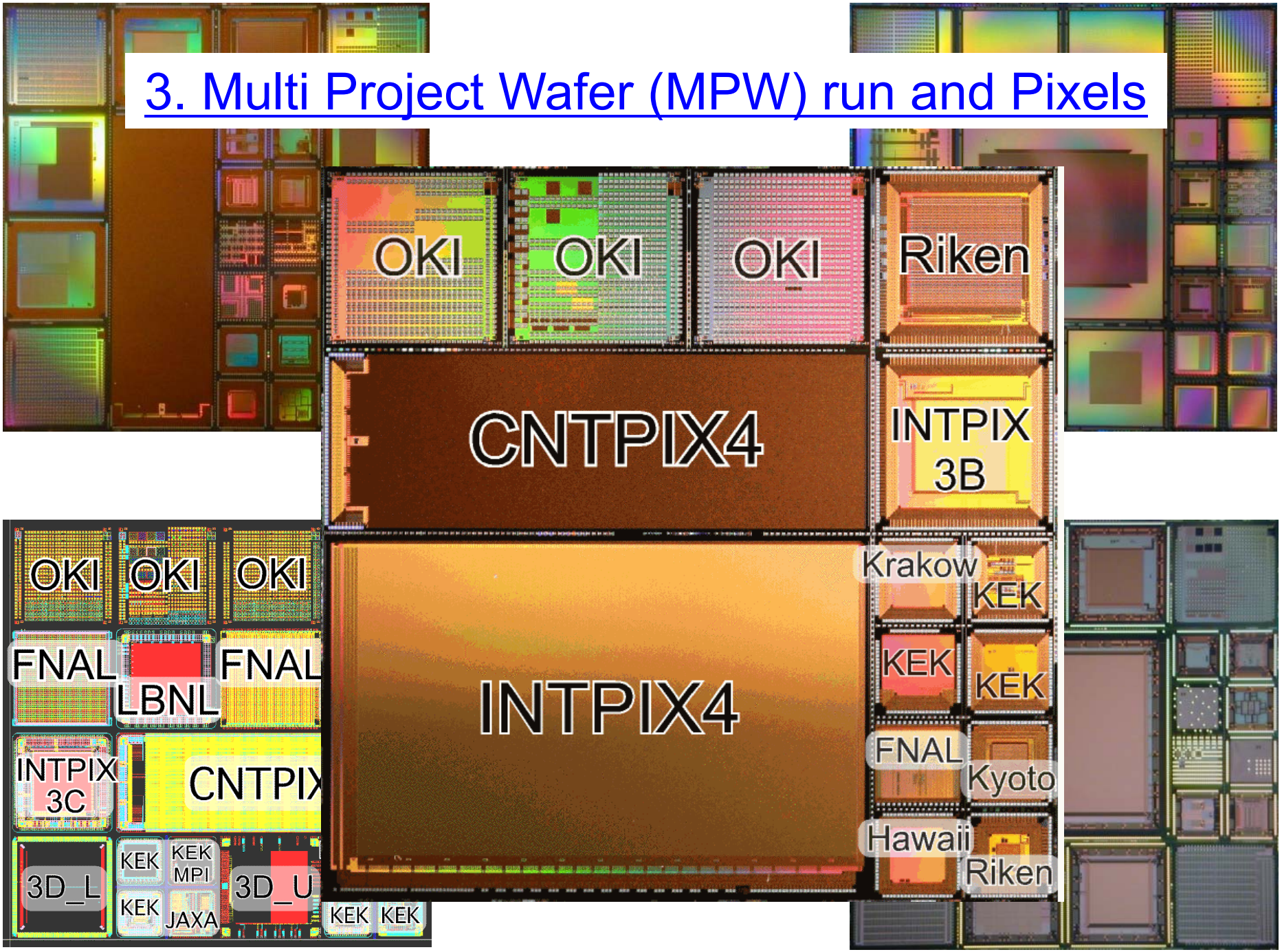
Cross sectional view of detector array (After stacking)



Unfortunately first trial takes longer time than expected due to mismatch between OKI and ZyCube process.

Work is still ongoing

3. Multi Project Wafer (MPW) run and Pixels



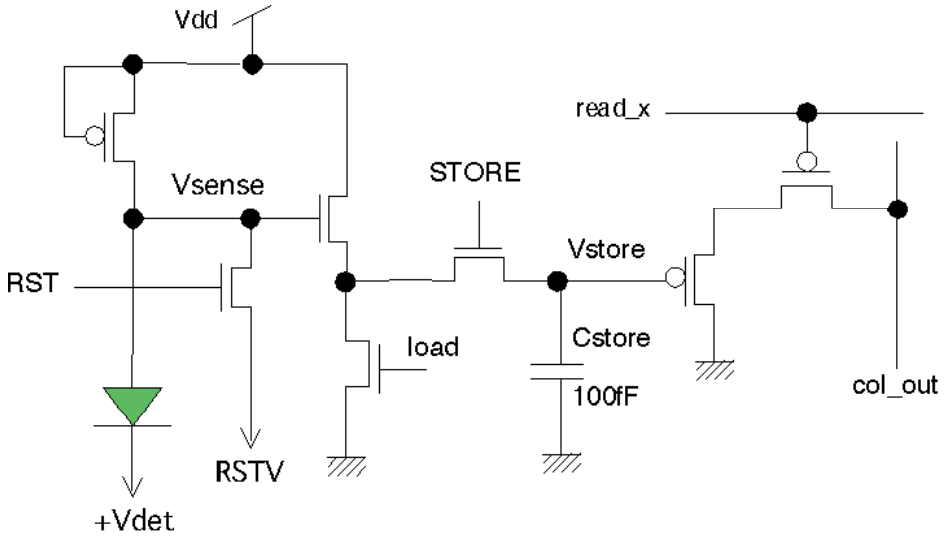
We have been operating the SOI MPW runs from 2007.
Several Lab./Univ. are joining this run.

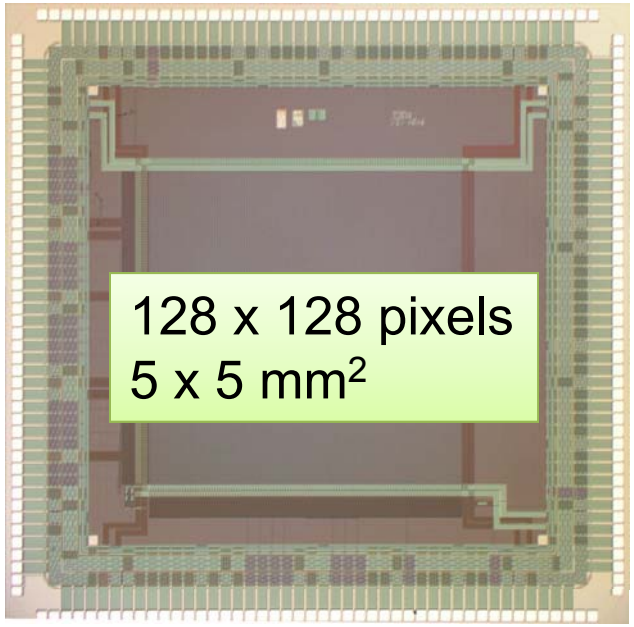
Further Process Improvements are envisaged.

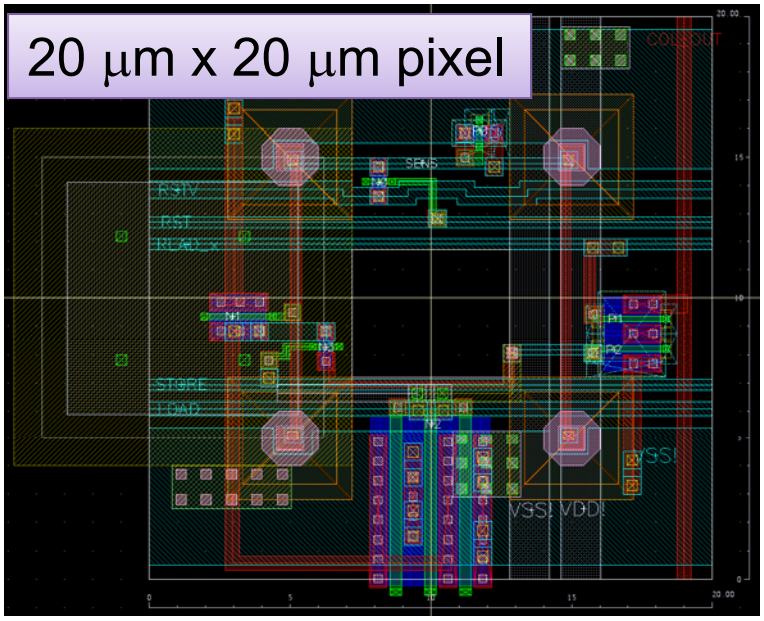
- Increase No. of Metal Layer : 4 -> 5 layers
  --> Better Power Network for Large Chip
- Increase MIM Capacitance : 1 -> 2 fF/um^2
  --> Shrink Pixel size
- Relax drawing rule : 30^o, 45^o -> Circle
  --> Higher Break Down Voltage
- ...

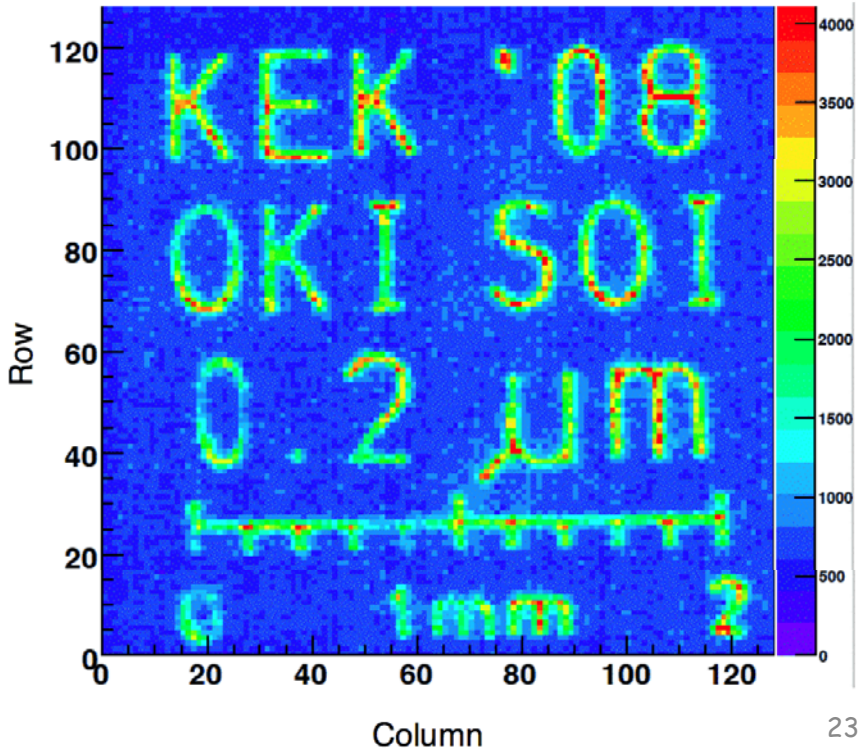
2 Submissions (July and December) are planned in FY2010.

Integration Type Pixel (INTPIX)



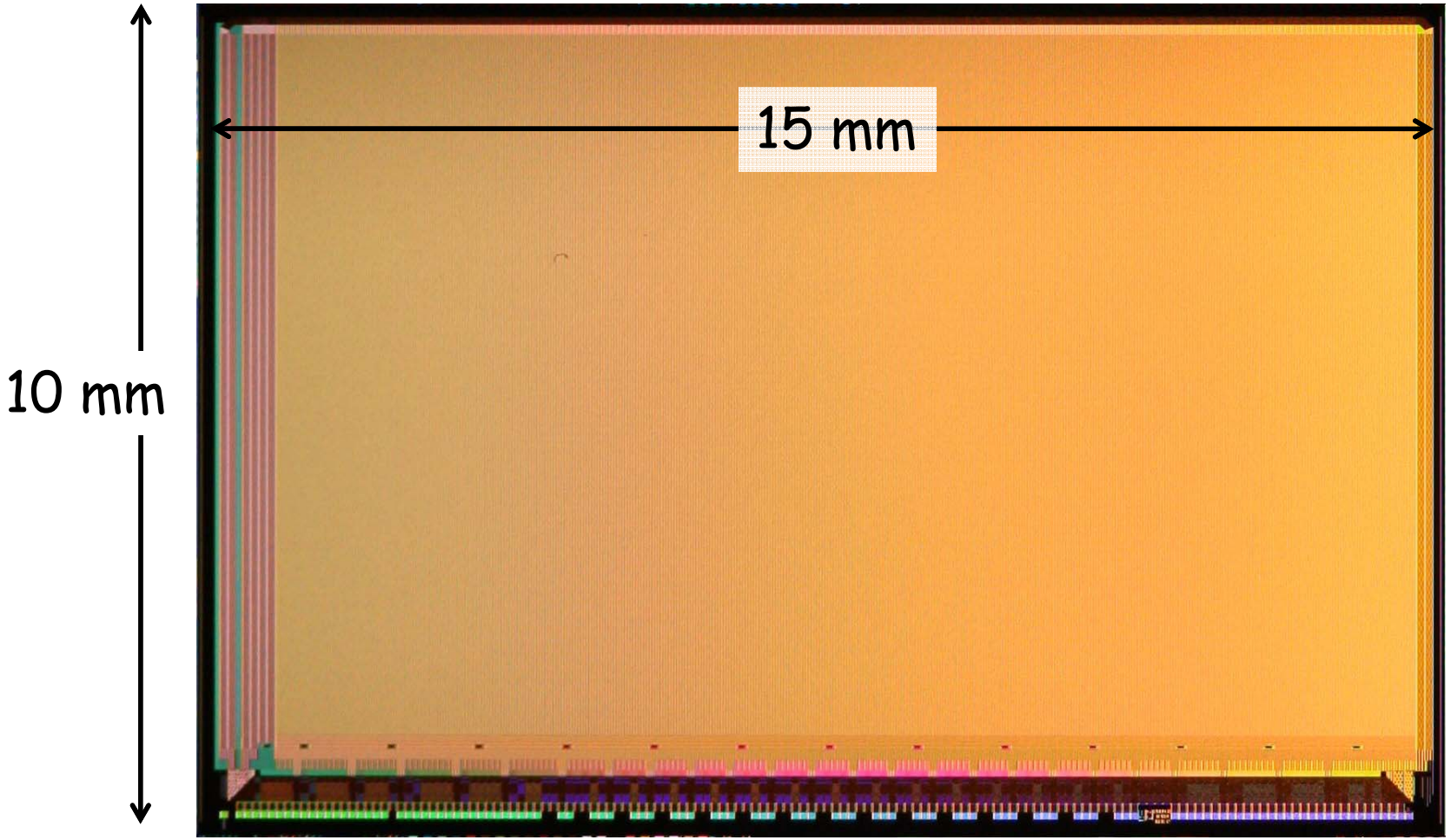






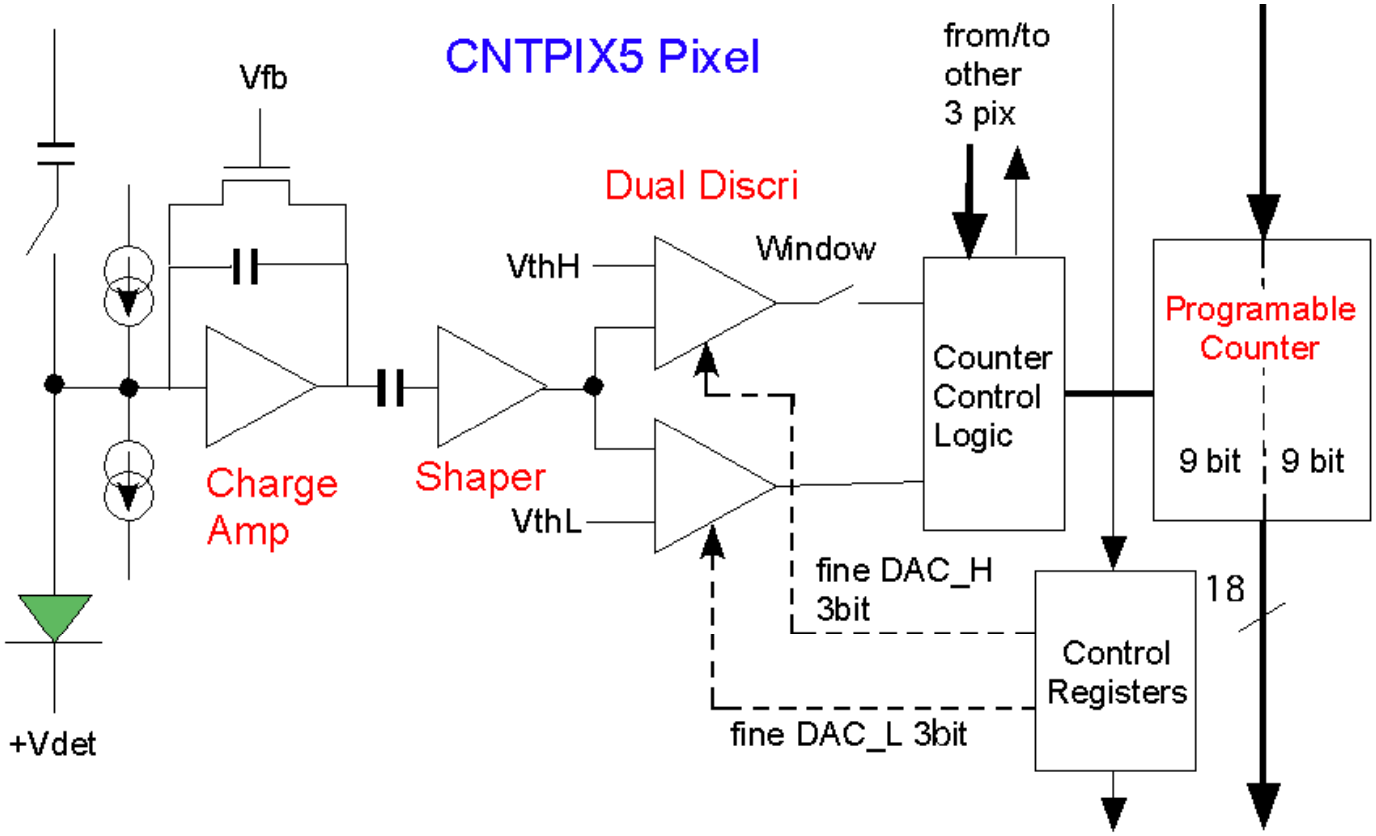
INTPIX4

Largest chip so far



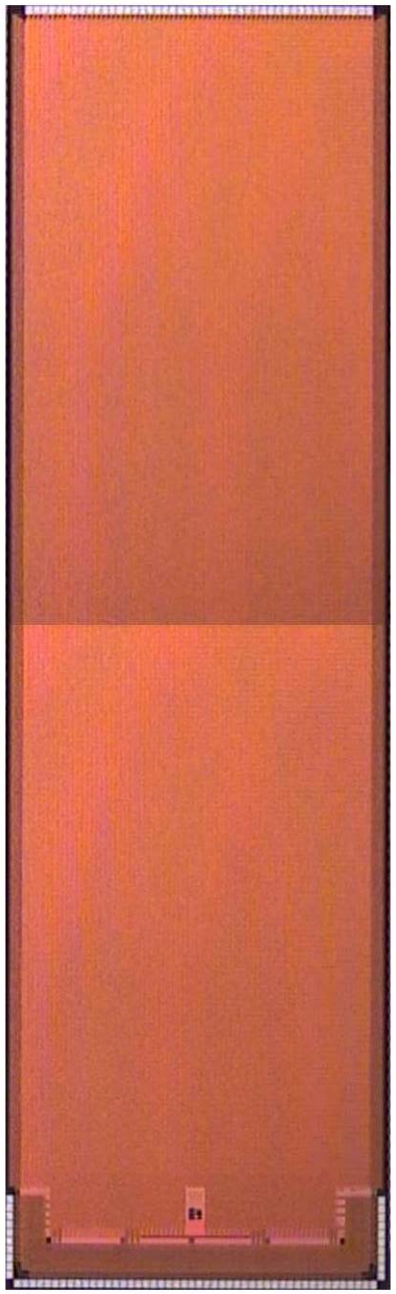
17x17 μm, 512 x 832 pixels (13 Analog Out)
CDS circuit in each pixel

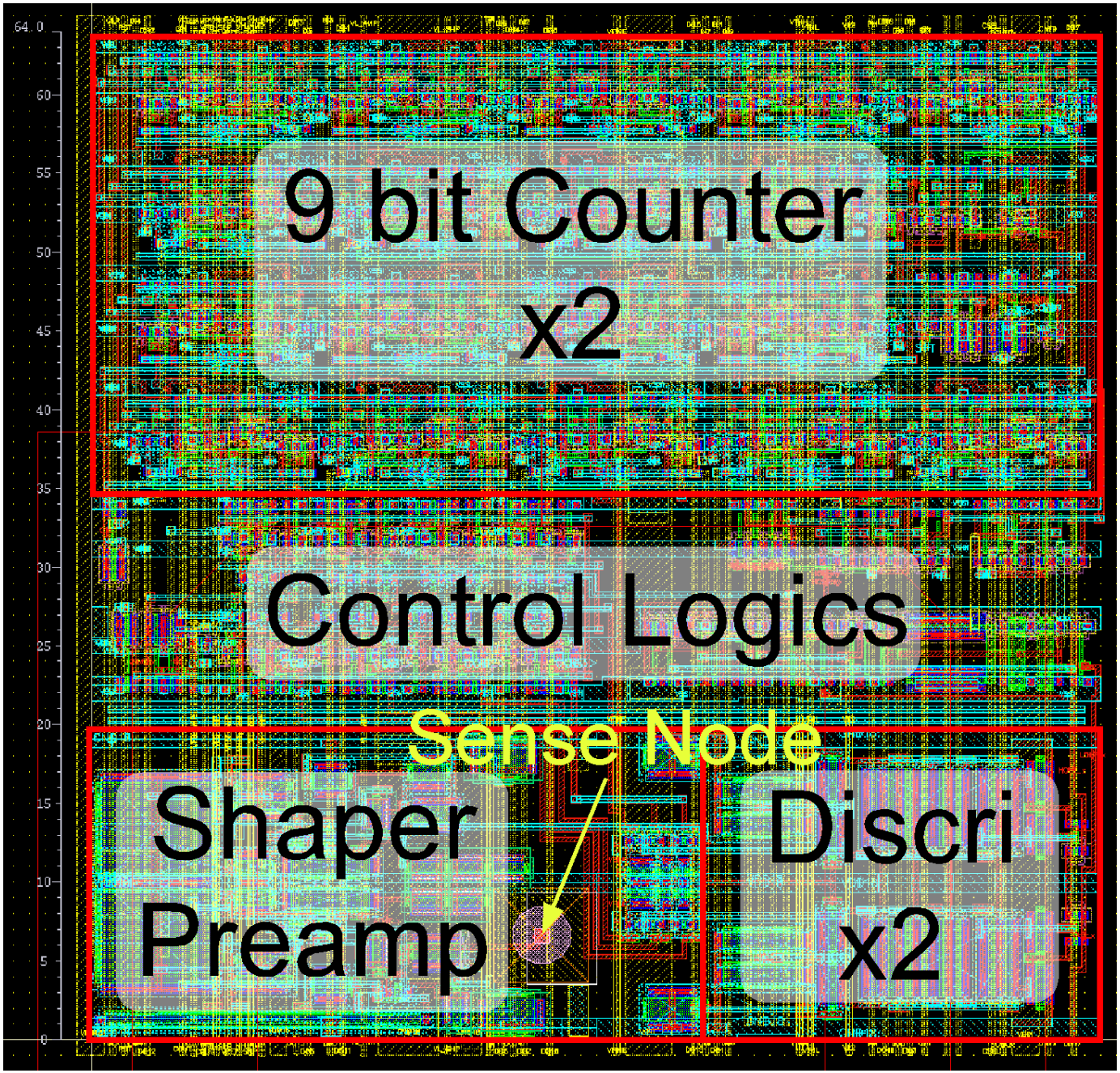
Counting Type Pixel (CNTPIX)



Energy selection and Counting in each pixel. 4 pixels can be combined.

5 x15.4 mm^2
72 x 272 pixels
64um x 64 um pixel



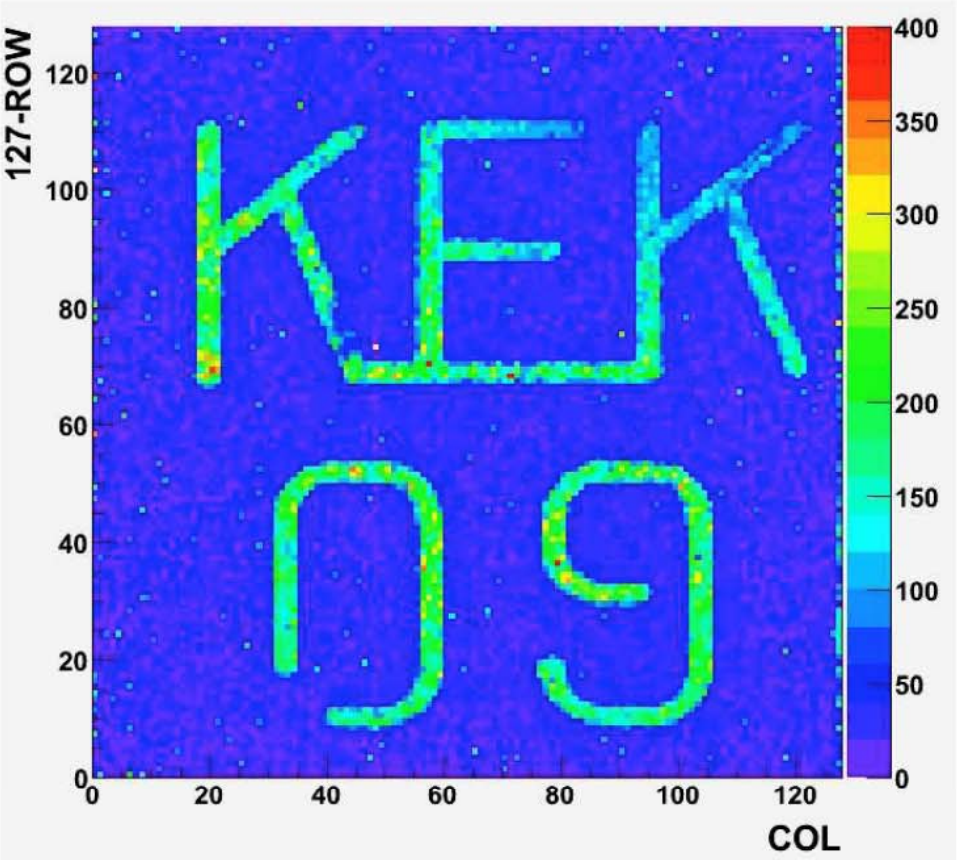


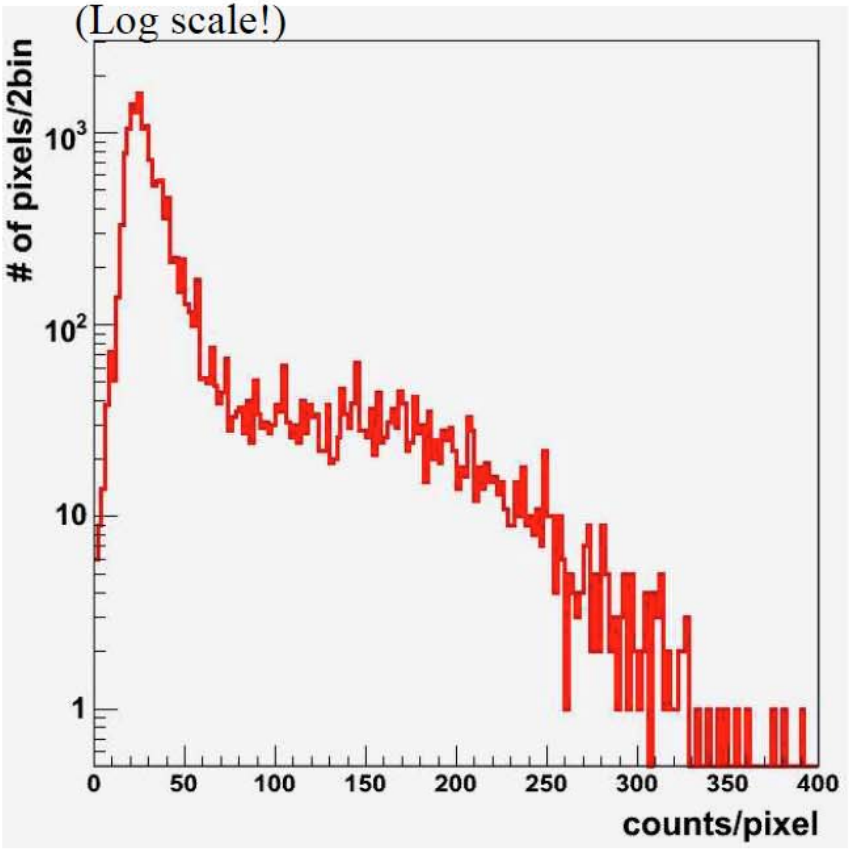
CNTPIX5
Pixel Layout

64x64 um^2

~600 Tr/pix
x 72 x 212
= 10,000,000 Trs

Brass (Cu/Zn) mask image (CNTPIX2.1)





Counter works fine!

~8 keV X-tay

Integration time 1.6ms
Vback =20V, Vref=1600mV, vthl=1400mV

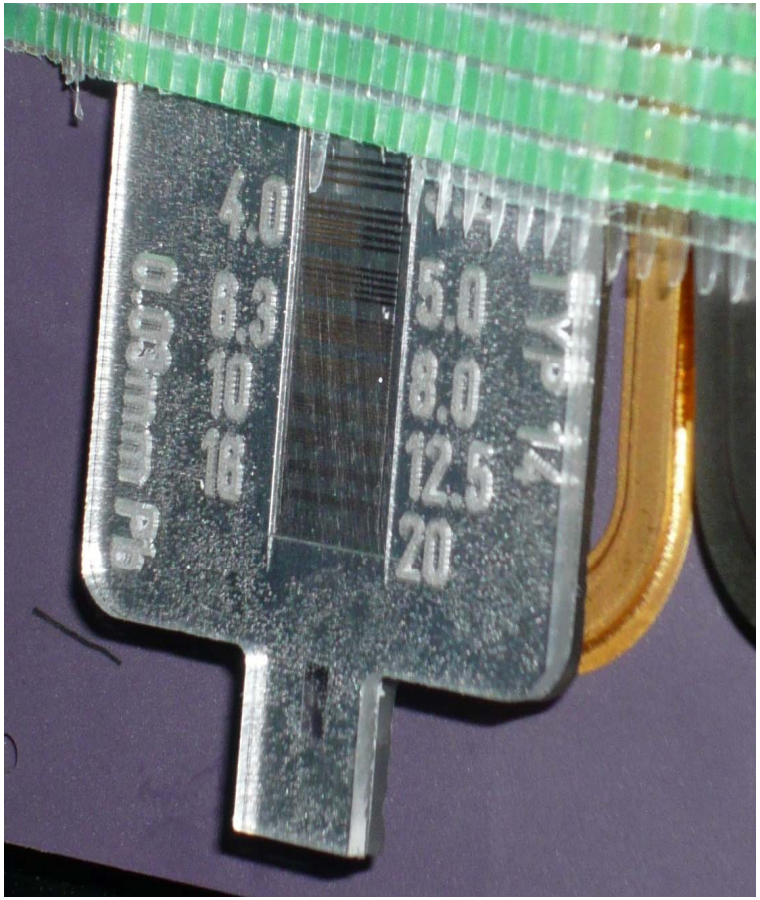
4. Summary

- SOI Pixel technology is very attractive for fabricating intelligent radiation image devices.
- The newly introduced Buried p-Well provide us ;
  - suppression of back gate effect
  - improving radiation tolerance
  - improving breakdown voltage
  - new sensor structure
- We are also developing 3D vertical integration technique by using μ-bump technology of 5 μm pitch.
- This SOI Pixel process is very unique, and no commercial process of this kind is available. So we open this process to our community by operating MPW runs.

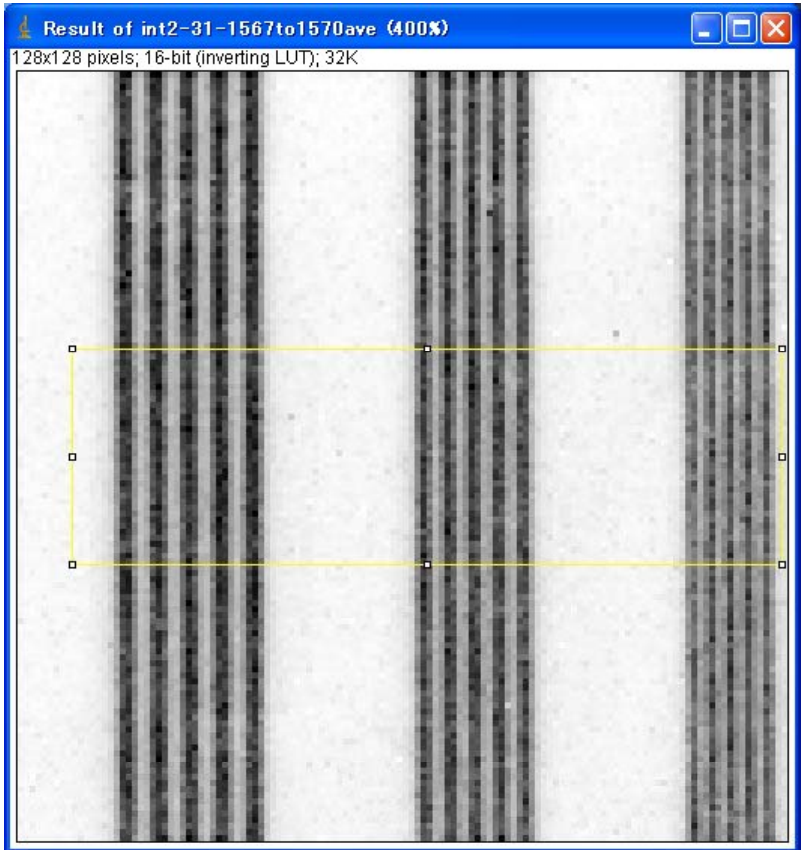
Supplements

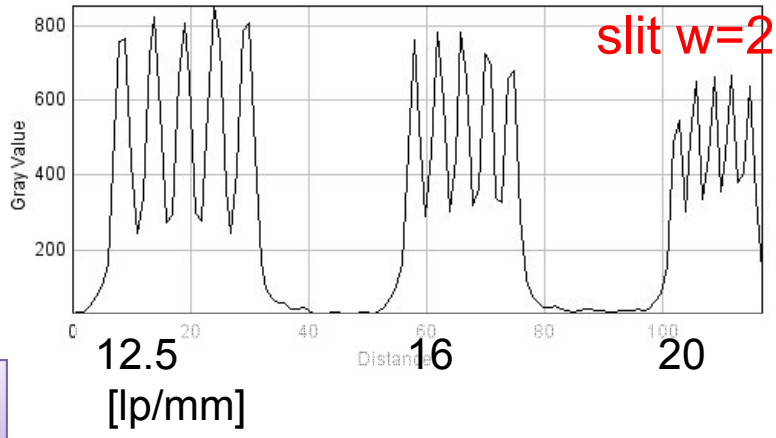
X-ray Image
Position resolution
(pixel size=20μm x 20μm)

INTPIX2



X-ray Test Chart



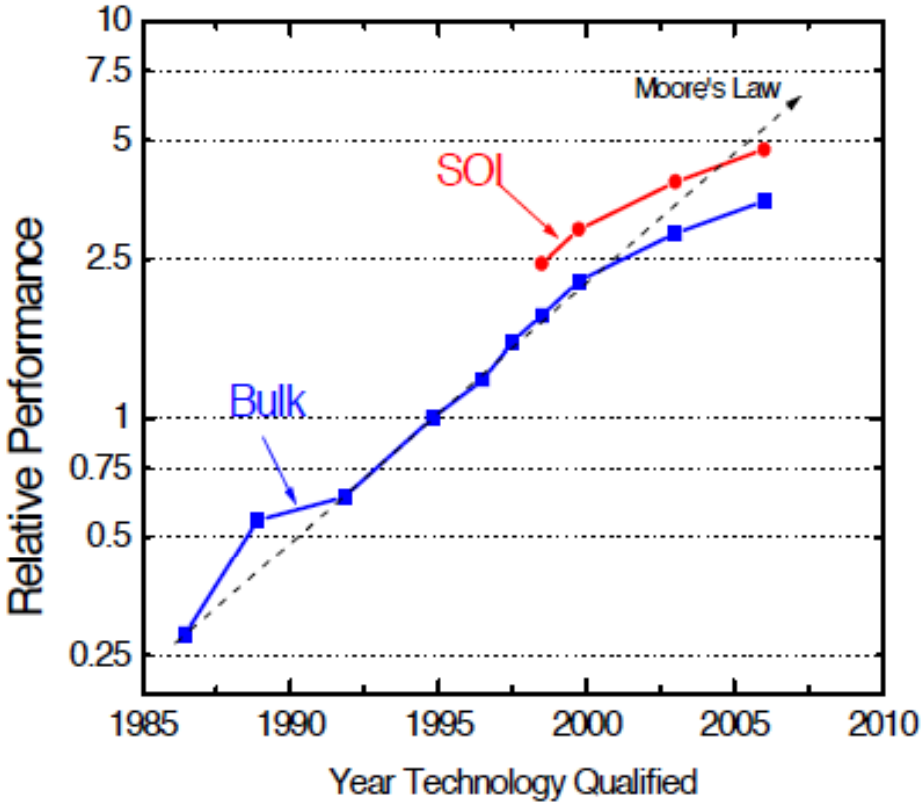


slit w=25μm

25 μm Slit is well separated.

Features of (FD-)SOI

- Full Dielectric Isolation :
  Latchup Free, Small Area,
  Good Circuit Isolation
  No Back Bias Effect
- Low Junction Capacitance :
  High Speed
- Steep Subthreshold Slope
  Low Power
- Less Impurity in Body
  Good Vth Matching,
  Less 1/f Noise

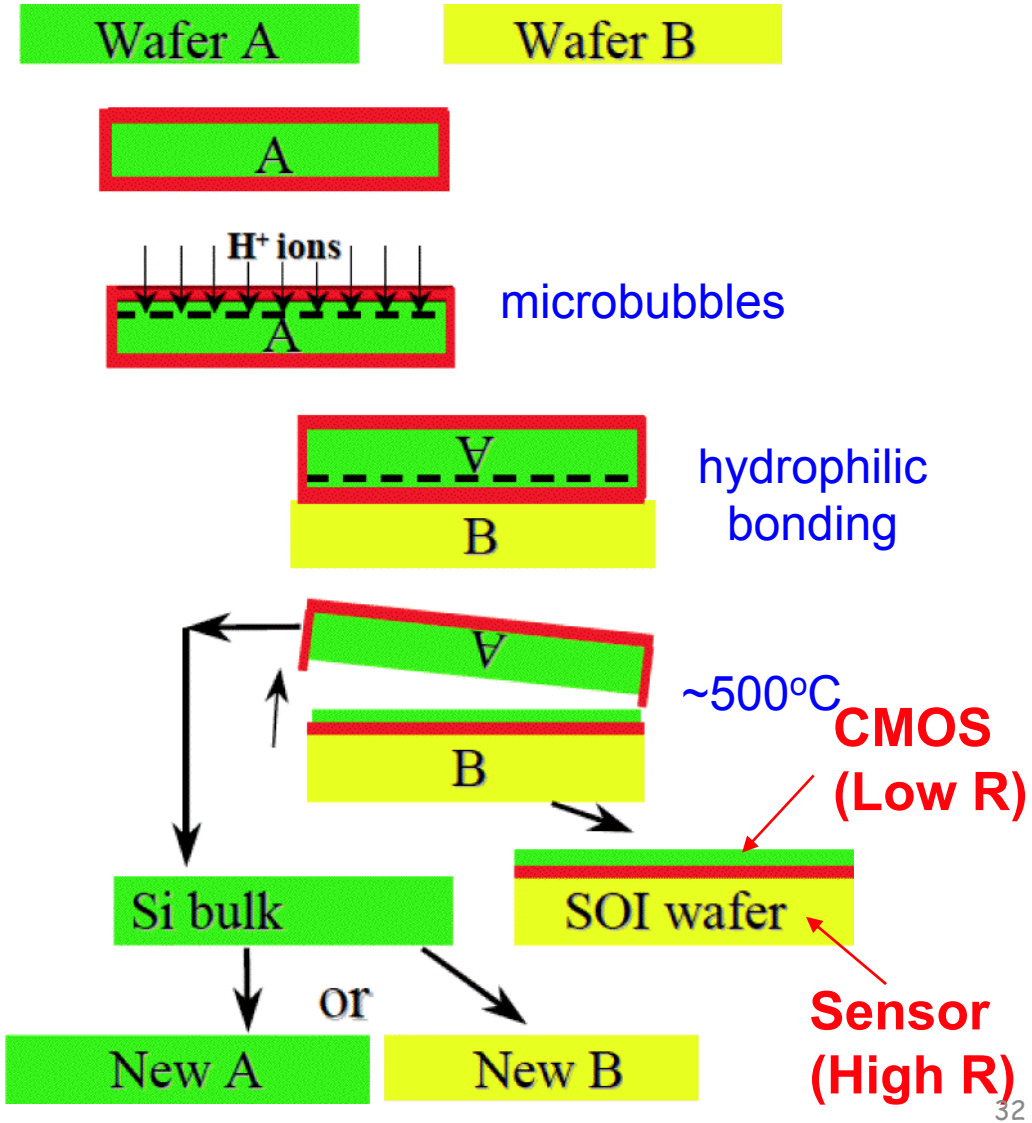


- No Well junction, Thin Film :
  Low Leak,
  Low Vth Shift (High Temp).
- Small Active Volume :
  High Soft Error Immunity

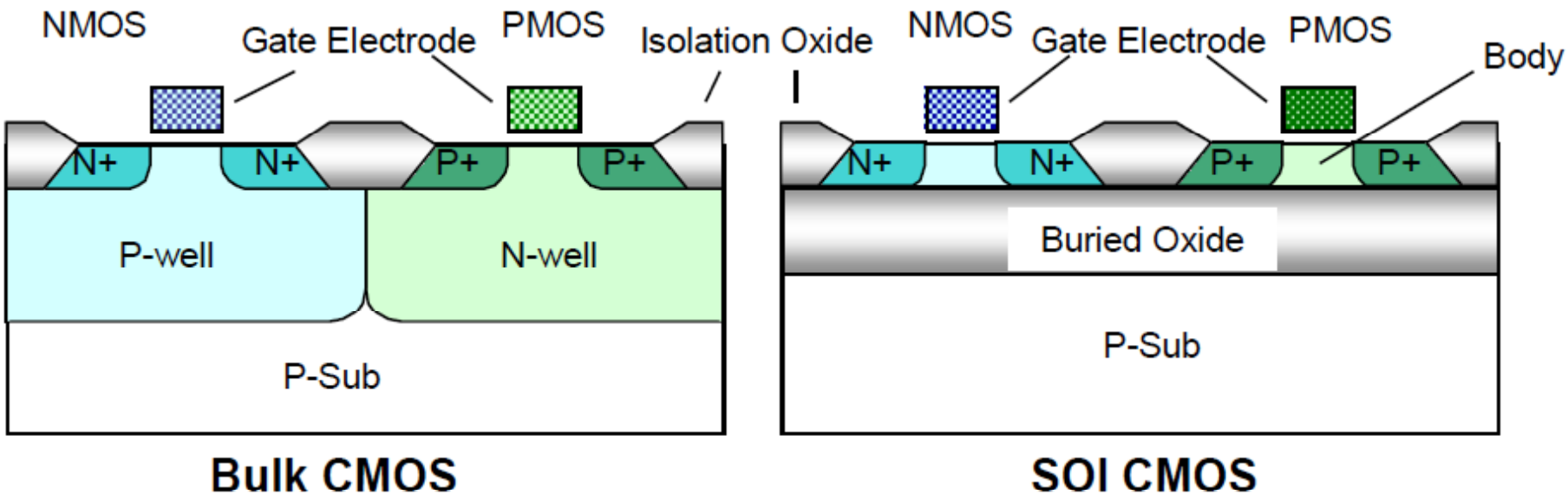
1. Introduction of SOI Technology

SOI Wafer (UNIBOND™) (1995, France LETI -> SOITEC)

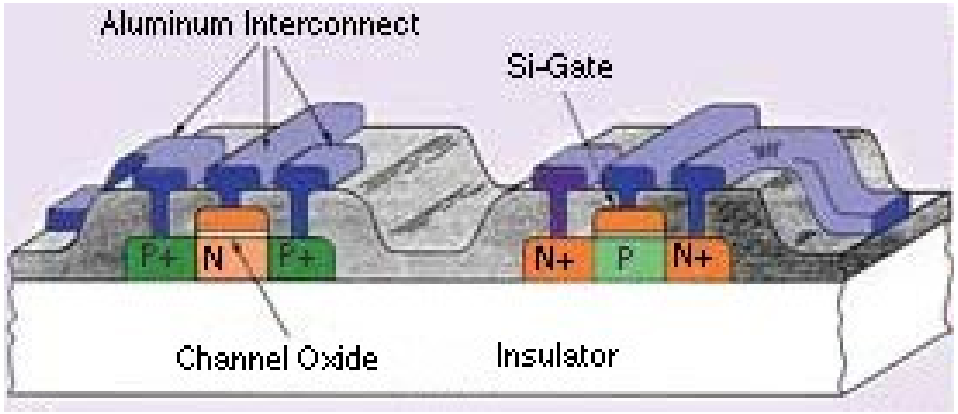
1. Initial silicon wafers A & B
2. Oxidation of wafer A to create insulating layer
3. Smart Cut ion implantation induces formation of an in-depth weakened layer
4. Cleaning & bonding wafer A to the handle substrate, wafer B
5. Smart Cut - cleavage at the mean ion penetration depth splits off wafer A
6. Wafer B undergoes annealing, CMP and touch polish => SOI wafer complete
8. Split-off wafer A is recycled, becoming the new wafer A or B



Bulk CMOS vs. SOI CMOS



In SOI, Each Device is completely isolated by Oxide.



PD-SOI vs. FD-SOI

PD-SOI (Partially Depleted)

◆Thick SOI thickness（T_{SOI}）
～100-200nm

◆Depletion layer < T_{SOI}

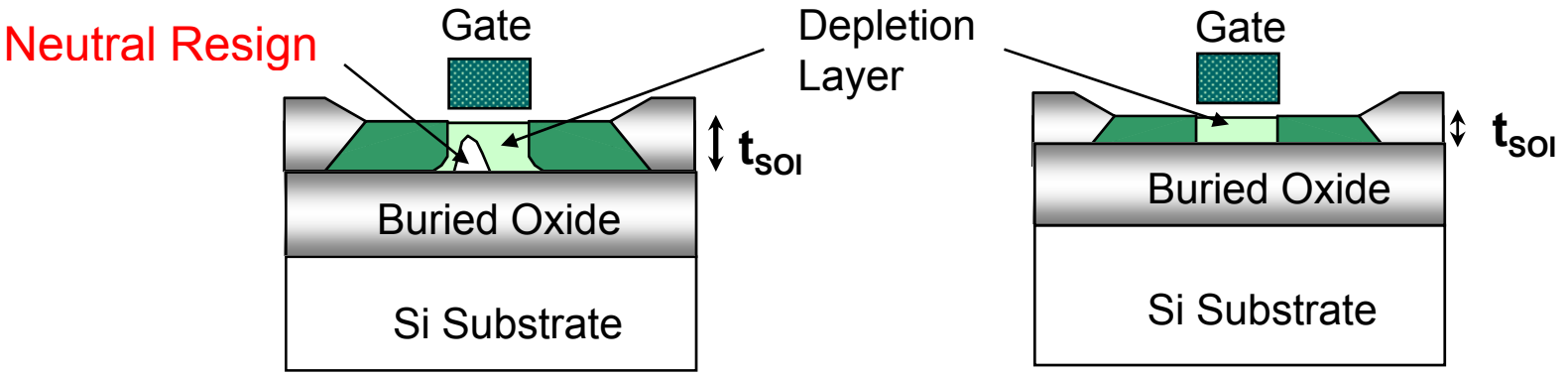
◇Large floating body effect
◇High drive Current by kink effect
→ High speed application

FD-SOI (Fully Depleted）

◆Thin SOI thickness （T_{SOI}）
< 50nm

◆ Depletion layer > T_{SOI}

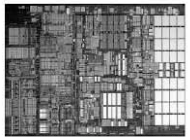
◇Less floating body effect
◇Steep subthreshold slopes
→ Low power application



FD-SOI has advantage in performance under very low voltage operation.

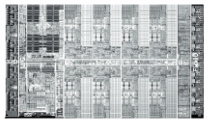
Current Status of PD-SOI and FD-SOI

◆ **PD-SOI (Partially Depleted)** (T_{SOI}=100~200 nm)



High-speed microprocessors

- **IBM: PowerPC , mainframe CPU's, Wii(Nintendo), Xbox**
- **Free scale: PowerPC**
- **AMD: Athlon processors**
- **Sony (with IBM and Toshiba) : Cell, PS3**



◆**FD-SOI (Fully Depleted)** (T_{SOI} < 50 nm)

Low-power application

- **Oki: solar cell watch, long-wave RF decoder**

http://www.casio.co.jp

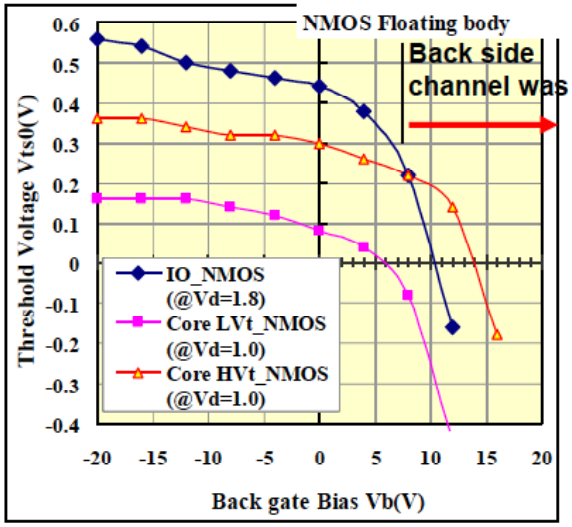
Technology Node option beyond 32nm, Next 3D Tr.

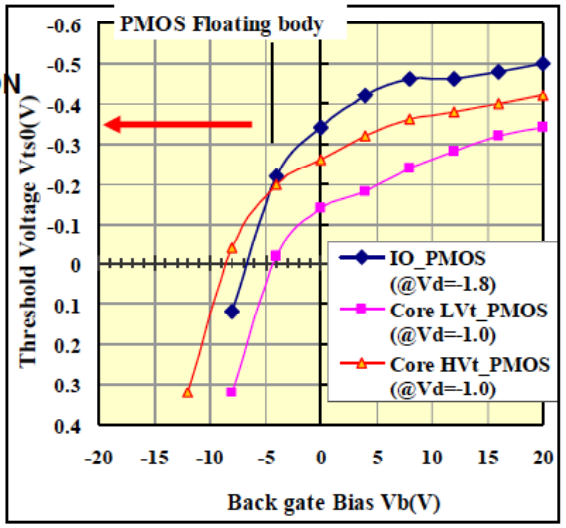
- **Intel, many major companies**

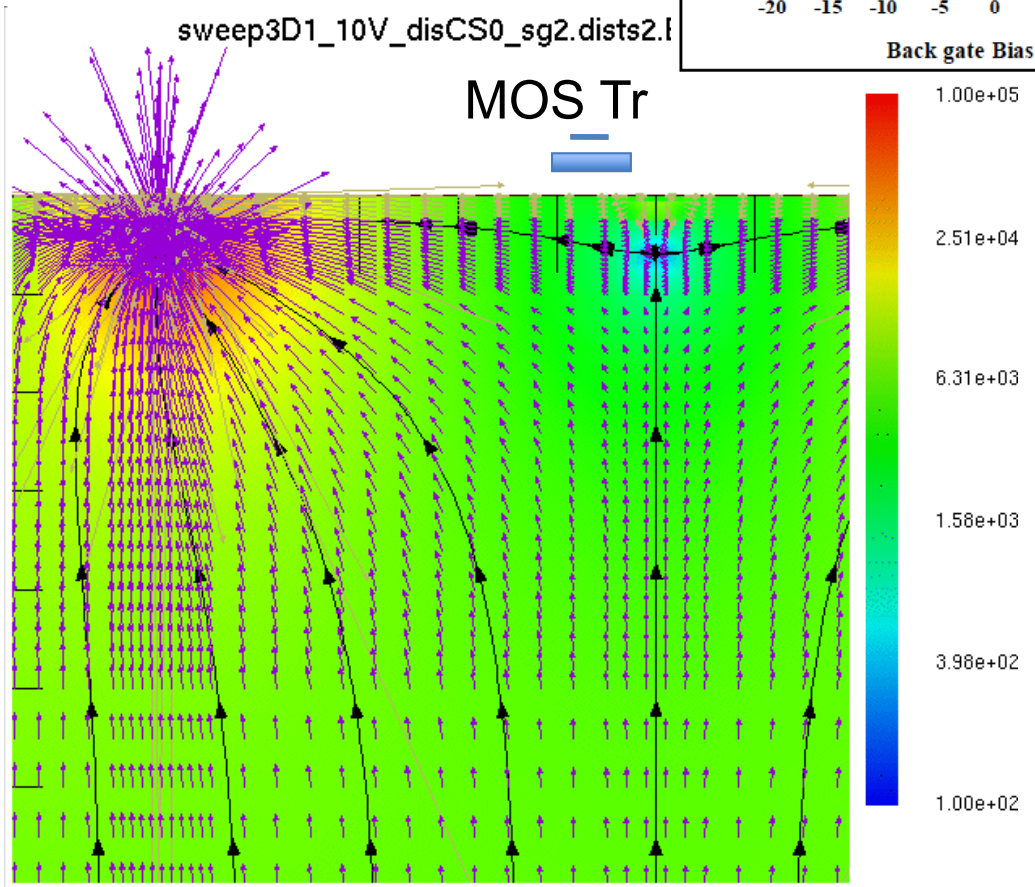
At present, only Oki has an experience of mass production of FD-SOI

Back Gate Effect

NMOS Threshold Variation PMOS transistor







Substrate Voltage act as Back Gate, and change transistor threshold.

FY09-1 KEK/OKI SOI CMOS 0.20um MPW run(MX1350)

Last update Oct. 21, 2009

Ths Submission was successfully done!

SOI MPW run web page
http://rd.kek.jp/project/soi/

GDS data submission dead line :

Dead line Aug. 24(Mon.), 2009, 17:00 Japan Time

Note on FY0

- It is not nec
- OKI request layer after r
- Dummy me matel layer
- No. of meta
- No Inductor
- BOX thickne
- Buried P-W
- Optional 3D

Documents

KEK-OKI SOI Pixel Process Design Kit

- Aug. 20, 2009 : KEK PDK Rel 04.01 : Release Note (Japanese, English), soi020_kek_OKI_REL0401.tar.gz NEW! NEW!
- Aug. 12, 2009 : DRC Rule file for Rel. 04.00 (Official version will be available on 20th Aug. This is temporary version (020soi_calibre_drc_for_KEK_r03_1arai2.rule) written by Y.Arai) obsolete!
- Aug. 11, 2009 : KEK PDK Rel 04.00 : Release Note (Japanese), soi020_kek_OKI_REL0400.tar.gz obsolete!
- Feb. 16, 2009 : Revised DRC Rule file (020soi_calibre_drc_for_KEK_r03_1.rule) obsolete!
- Feb. 11, 2009 : KEK PDK Rel 03.00 : Release Note (Japanese), soi020_kek_OKI_REL0300.tar.gz obsolete!

SPICE

- June 30, 2009 : How to specify Body-Tie, Source-Tie, and Body-Floating Tr parameters in SPICE (pdf)
- June 30, 2009 : Core Low Vt Body Floating Tr SPICE model is updated (.inc file, .skew file, pdf)
- June 23, 2009 : Diode model (Layout, I-V curve, Low Temperature model, High Temperature model)
- Oct. 3, 2007 : QSD-11523
  * QSD-11523 document (revised Nov. 28, 2008) (Japanese Excel , English pdf)
  * Appendix (Excel, Excel, English pdf)
  * SPICE models (zip) (or use files in soi020_kek_OKI/SIM_PARAM for Cadence Opus Environment)