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Sparsified Fast Readout for a 256-Pixel 3D Device

A prototype of a 256-pixel 3D ASIC, proposed by the Italian VIPIX Collaboration and implementing a fast readout architecture with sparsification capabilities, was recently submitted. The chosen technology is CMOS Chartered 130 nm. In particular, the readout logic exploits one of the two layers of a 3D device. The readout logic can face an input hit rate of the order of 100MHz/cm2, it can interface with a matrix of 256 pixels and allows sweeping the matrix within 1us. The architecture has been deeply investigated in terms of efficiency and sparsification capabilities and a parameterised VHDL code has been designed to match even larger matrices of pixels. A fast readout might also match a data-driven tracking system. The paper presents the readout efficiency versus a variety of parameters as the clock rate, the pixel hit-rate and the time-stamp resolution. The overall project leads to design a high-density thin vertex detector with an on-chip sparsified digital readout system, for particle tracking, aimed at matching the requirements of future high-energy physics experiments.

Summary (Additional text describing your work. Can be pasted here or give an URL to a PDF document):

www.bo.infn.it/vipix/downloads/summary.pdf

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