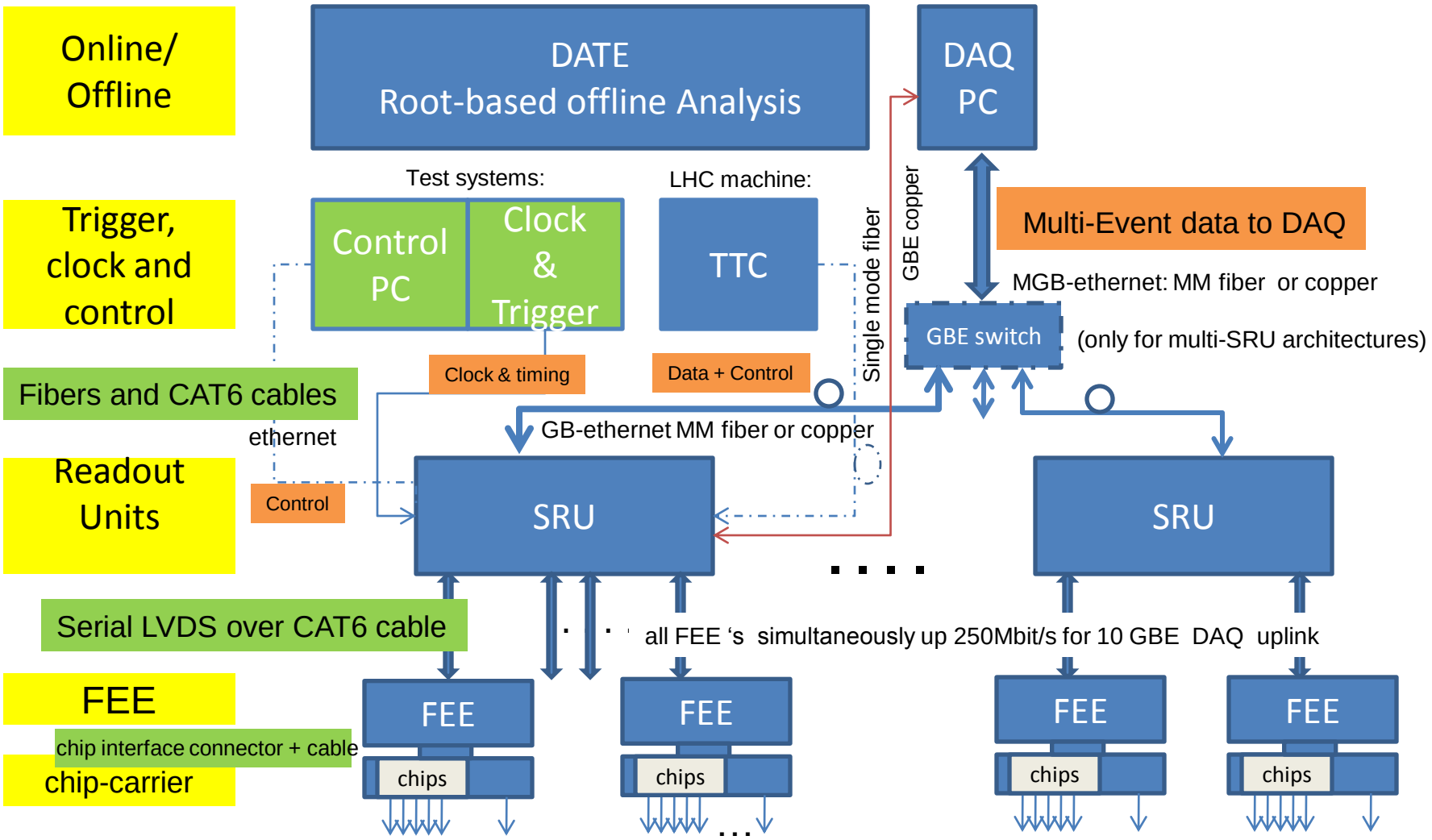
Scalable Readout System status

proposal: see WG5 meeting CERN
April 2009

Scalable concept in a nutshell



People, Users, Companies

- **CERN resources**
- Dr. H. Muller, CERN PH: scalable RO proposal , coordination and documentation
- Dr. H. Hillemanns, CERN DG/KTT Technology Transfer officer: legal and WEB
- Dr. P. van de Vyvre, CERN PH, ALICE DAQ: Gigabit ethernet port for DATE
- Dr. V.S. Martoiu (CERN fellow RD51 as from Sept 09) FEE- Chip Interfaces

External engineering and production resources

- Rui Pimenta, Satellite services, NL: Cadence design SRU (completed)
- Infosys, London UK (Allegro Layout)
- Firstec Geneva (production)

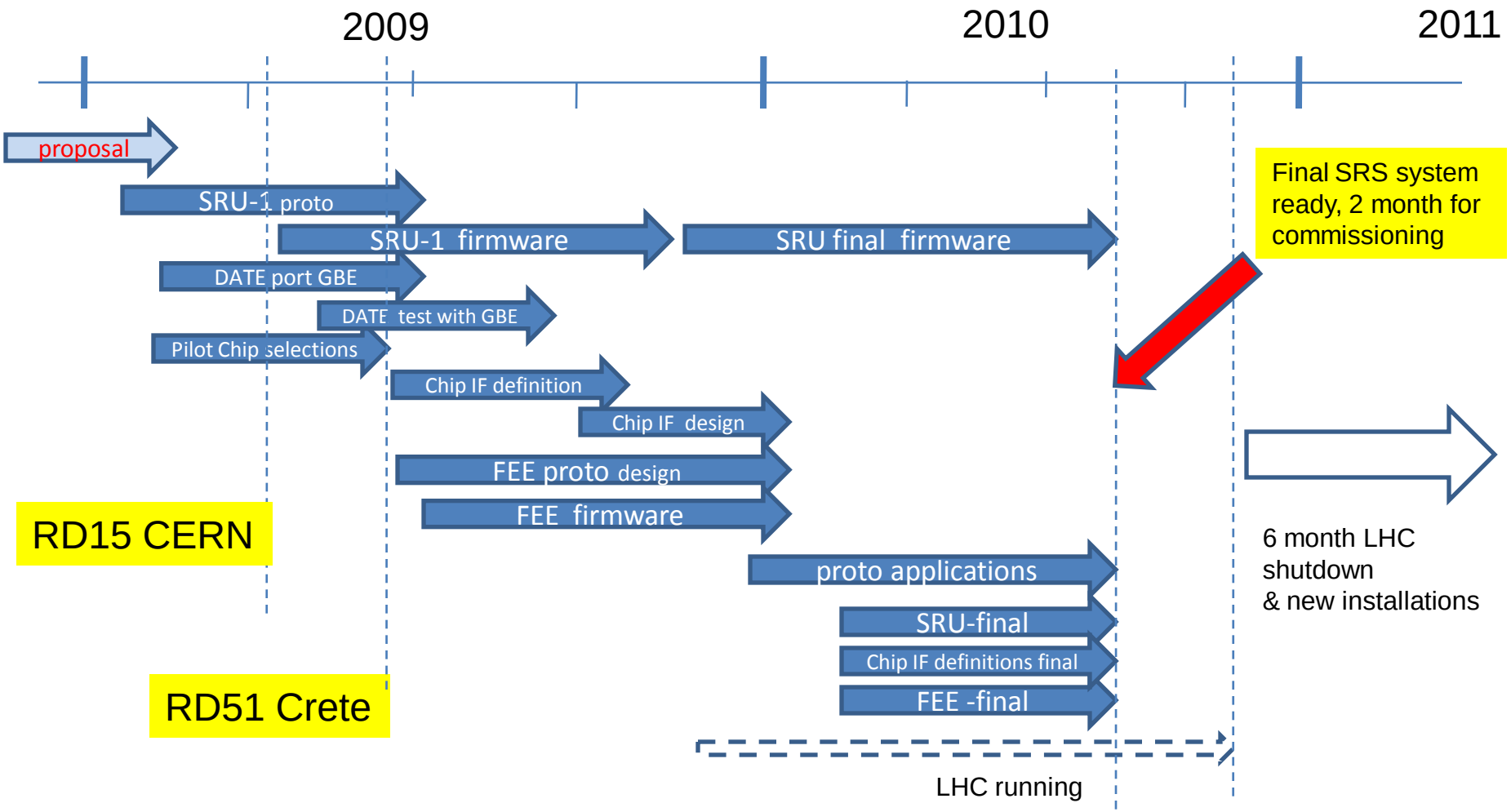
<u>Confirmed USERs</u>

- Dr. Jose Toledo , Univ. o. Valencia: NEXT (dual Beta decay) FEE electronics and packaging
  + Alfonso Tarazona , Univ. o Valencia, NEXT project: Gigabit Ethernet hardware implementation
- Prof. Daicui Zhou for CCNU Wuhan team: upgrade projects for ALICE LHC: serial cable, Board Controllers, DATE compatible Data formats and protocols
- Dr. J. Wotschak, CERN PH, for ATLAS MMega project: upgrade of Altro-based system
- Other teams under discussion

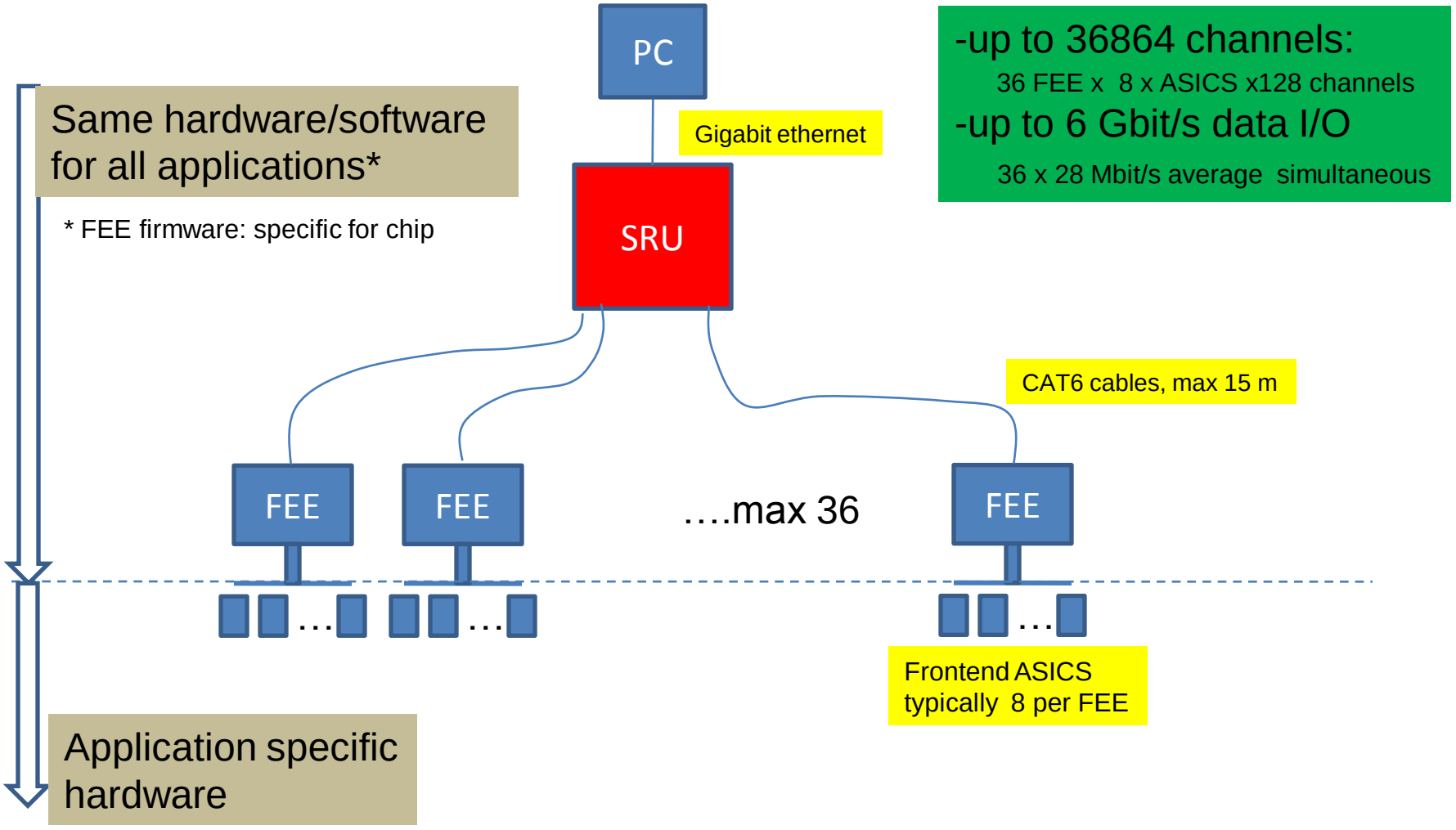
<u>Observers , potential users</u>

- Dr. Alex Walsch, GE Global Research, Garching Munich: industrial research application

Project Timing SRS



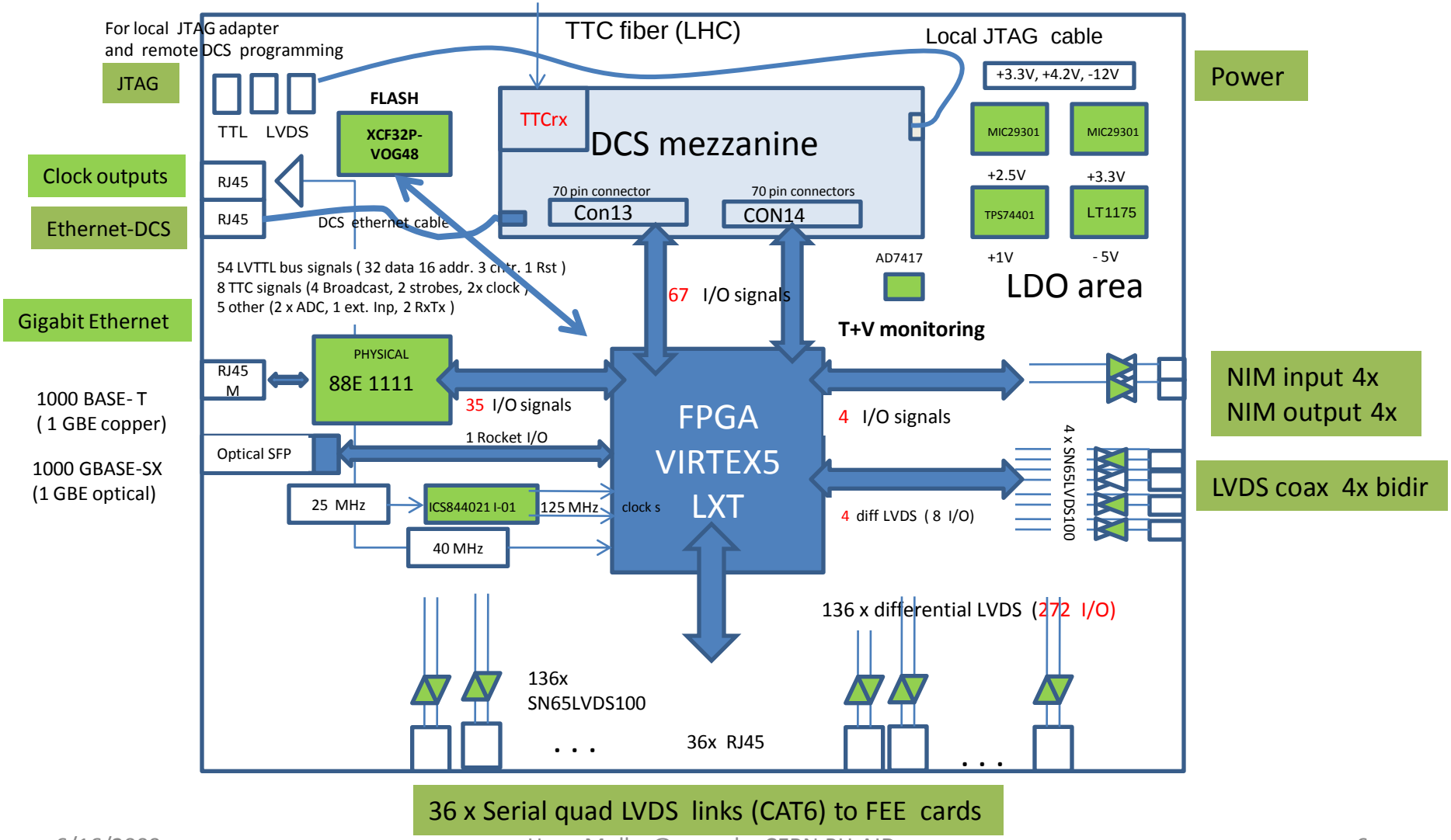
First target: 1 Gbit/s to DAQ single SRU system



First SRU

1 Gbit/s ethernet copper/optical

based on Virtex-5 LXT FPGA



Status

- SRU (V1.0) Cadence design finalizing now
- Board layout in July 09 in UK
- test protos (Nr. tbd) in September in Geneva
- Serial cable and BC to start in July in Wuhan
- FEE proto design at UPV starting in July (?)
- GBE implementation started at UPV
- Chip interface design starting at CERN in Sept.

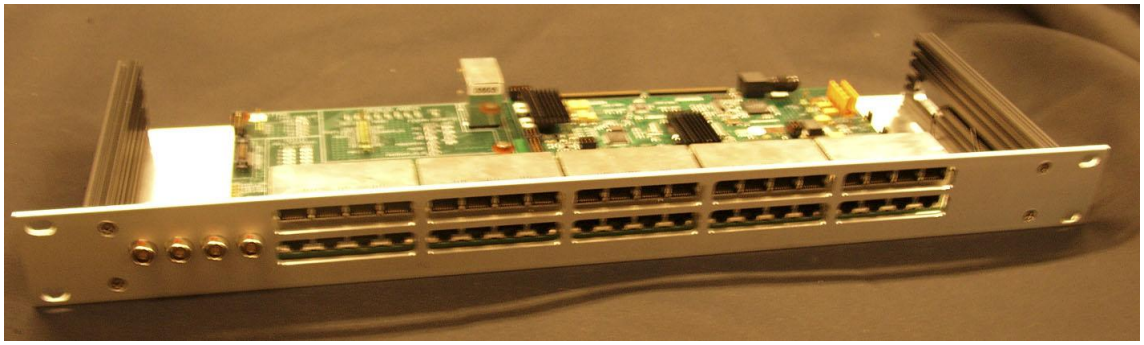
Plans and calls

- Target for 1 GBE proto system (with 1 dedicated FEE /chip) by end 09
- More applications focusing on other FEE chips: welcome for active participation
- Template FEE design and Firmware for APV25, VFAT, Timepix, … needed
- Need to decide soon on formfactors, power, cooling and connectors

Backup

SRU board: rack mounting in 19”

Photo of a similar card with RJ45 network plugs on the front panel

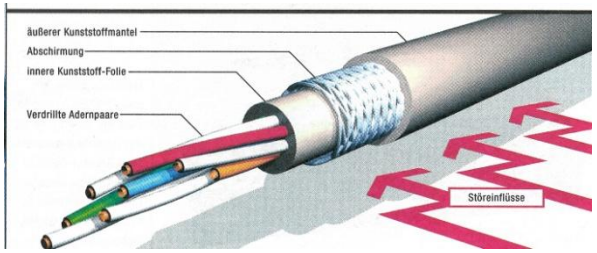


With similar layout, the SRU board will fit in 1U of a 19” chassis, power from backside

RJ45 cables to FEE’s

Trigger and clock coaxial cables

SRU<->FEE: serial LVDS



4 x twisted pairs

max 15 m @ 280 Mbit/s

clock
data
select
return

CAT 6 cable

34 x

FEE

RJ45

FPGA

4

chip Interface bus

SRU

RJ45

Reversible LVDS drivers/receivers

FPGA

4

10 GBE

Input data stream from
34 FEE's = 9.52 Gbit/s

Serial readout/contol modes over CAT6 cables

2 modes of operation defined by SRU clock
FEE board controller senses clock to switch mode

Readout mode: clock = 40 MHz to FEE
data = 280 Mbit/s to SRU
select = readout-trigger to FEE
return = local trigger to SRU

Control mode: clock <= 4 MHz to FEE
data = Serial data out to SRU
select = Serial data in to FEE
return = coded status to SRU

FEE card architecture