Working Group 5 Crete

Task: Common electronics

- Scalable RO system (test system => large system)
- User/application specific frontend (chip level)
- RD51 standard electronics cards
- DAQ system: DATE due to its stability and longterm support
- Applications and timescales
- Connectors, power, packaging, distances

Working Group 5 Crete

Task: Common Readout Chips

- Chip Matrix
- Preferred chip choice: APV25, Timepix, AFTER,
- S-ALTRO ?
- Technology templates
- Availability

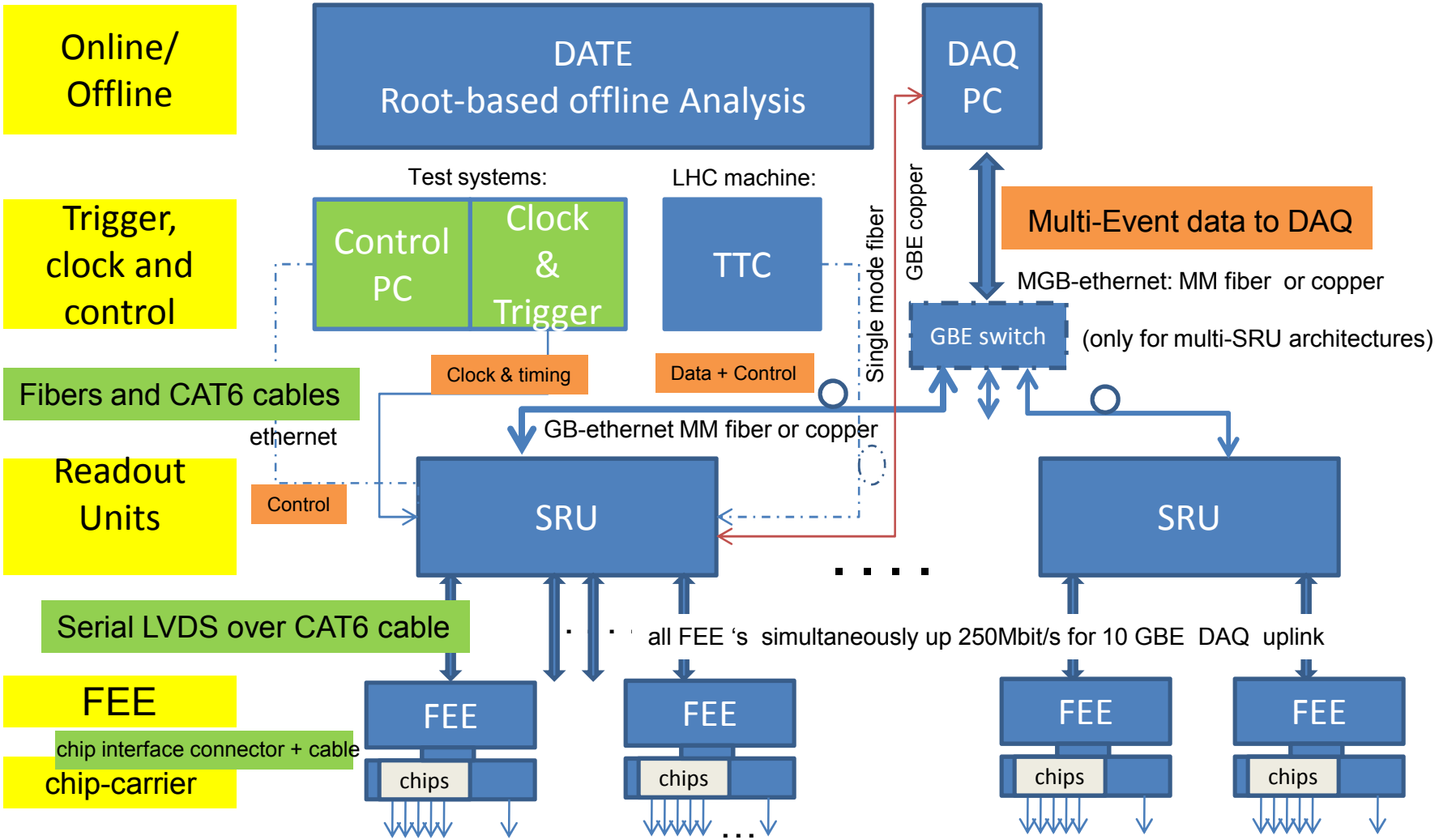
Summary WG5 meeting

rd51-wg5-contacts@cern.ch

- Welcome and presentation of new convenors (J.Kaminski, H.Muller) - Hans Taureg
- Common readout system revisited from last WG5 meeting - Jose Toledo , UPV Valencia
  - summary of the proposed solution, timescales, manpower, resources - H.Muller, CERN
- Matrix of Readout chip candidates
  APV25, VFAT, Timepix-2, AFTER, (S-ALTRO) and more - Jochen Kaminski Uni Bonn
- discussion on power, mechanics, HV control, connectors to carriers - Hans Muller CERN
- Slow Controls (DCS) - Hans Muller CERN
- Data Acquisition: DATE case example ATLAS Mmega - - Joerg Wotschack CERN
- Applications
  Electronics for NEXT Jose Toledo, UPV Valencia
  Electronics triple GEM TPC - Jochen Kaminski, Uni Bonn
  Electronics upgrade for ALICE Calorimeters - CCNU Wuhan team (presented by H.Muller)
- Action Items and goals for next meeting

Attendance WG5 5-8 persons

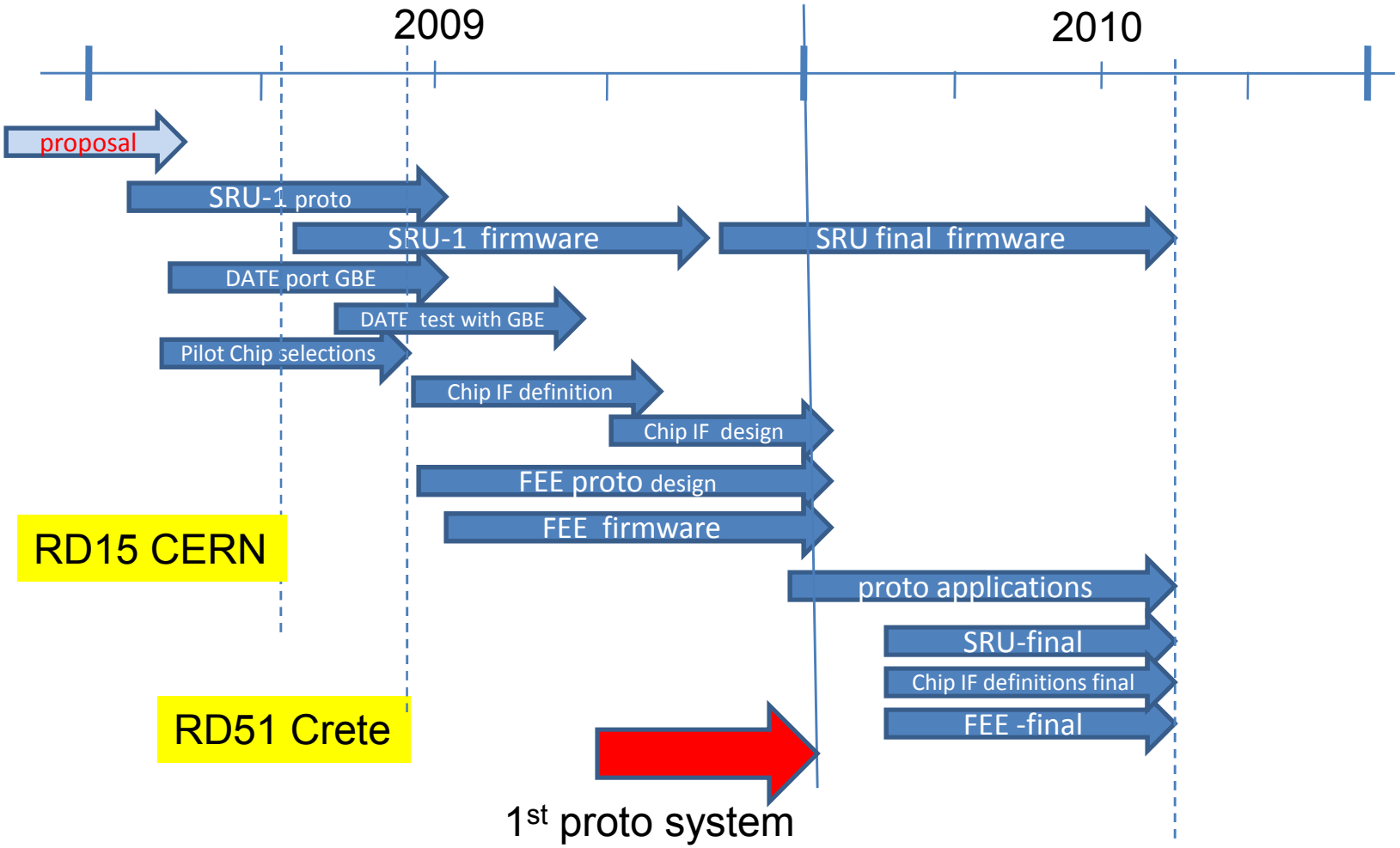
Scalable concept in a nutshell



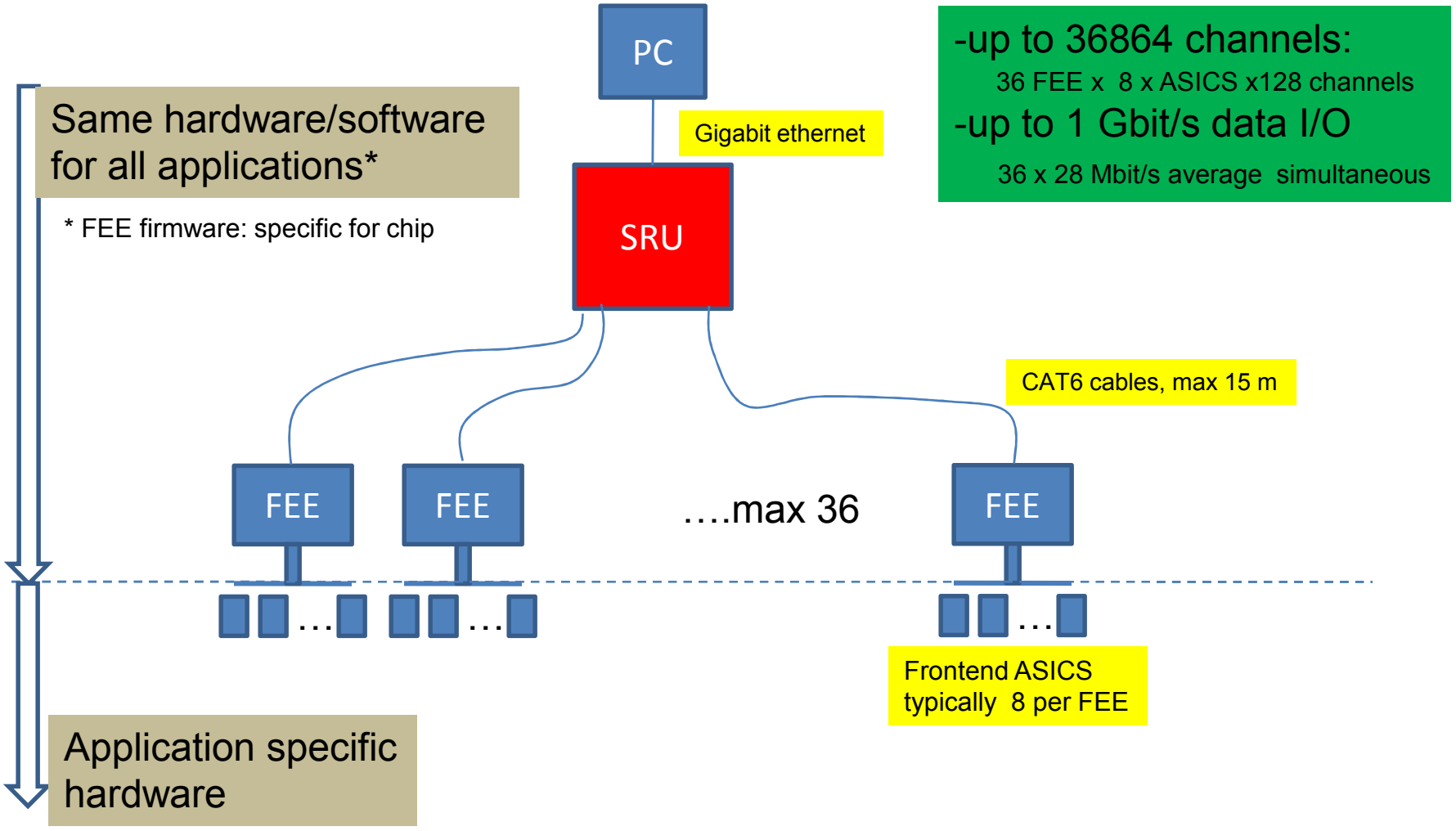
Confirmed USERs / Applications

- NEXT (dual Beta decay): dedicated FEE electronics/ Gigabit Ethernet hardware implementation
- CCNU Wuhan team: upgrade projects for ALICE LHC: serial protocol, Board Controller Firmware
- ATLAS MMega project: upgrade of Altro-based system
- LC –TPC for Timepix-based readout
- Other applications under discussion

Project Timing



First target: 1 Gbit/s to DAQ single SRU system

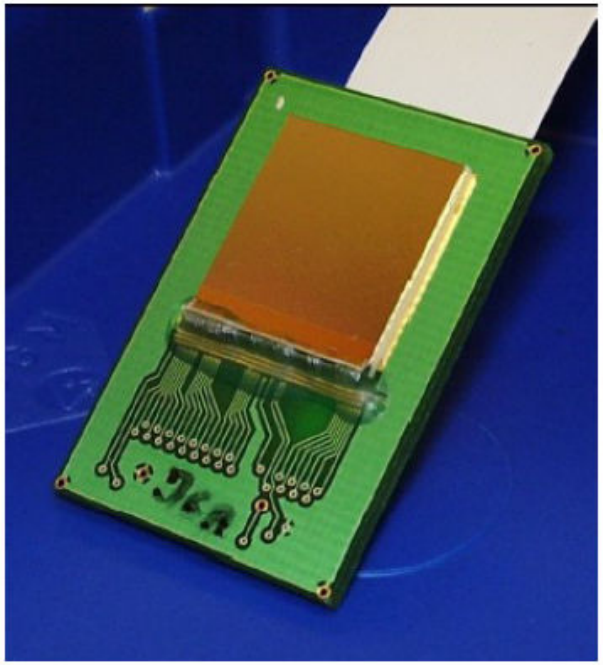


CHIP matrix

Overview of Candidate Chips

Name	# channels	preshaper	ADC bit	noise	Fast-OR	power	
APV25	128	50ns	analog	1200e⁻ at 20pF	no		
AFTER	72	100ns-2µs	analog	800e⁻ rms		8mW/c.	T2K
Timepix	65536	110ns	14	100e⁻ rms	no	16µW/c.	
VFat	128	22ns	1	650+50e/pF			
Carioca	8		1	2000e + 50e/pF		45mW/c.	
Beetle	128	23ns	128*1	500e + 50e/pF		5.5mW/c.	
Dirac	64		8			10µW/c.	ILC
KPix							
DCAL	64	65-125ns	1				ILC-Calice
SPIROC	36	50-175ns	12			15µW/c.	Si-PM
SVX3/4	128	80ns	8	500e + 60e/pF		2mW/c.	
Gossipo-3/4	32	4ns	1	800e + 60e/pF	yes	24mW/c.	
SALTRO	64	30-300ns	10		no	32-60mW/c.	
Timepix-2	65536						

Timepix



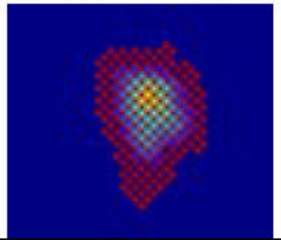
256 * 256 pixel

pixel size: 55 * 55 μm²

chip dimensions: 1.4 * 1.4 cm²

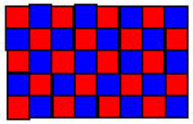
Each pixel can be set to one of these modes:

- hit counting
- TOT = time over threshold
  gives integrated charge
- time between hit and shutter end
- hit/no-hit



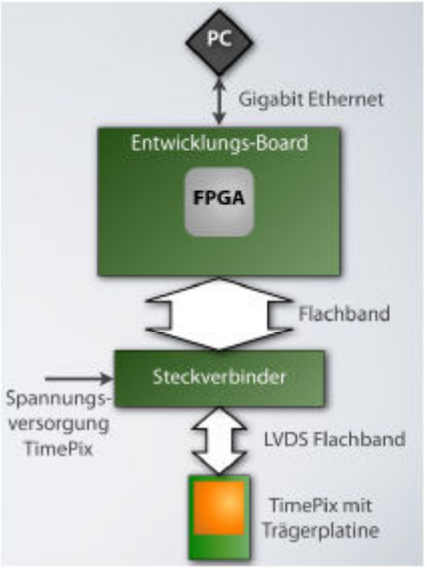
current running condition:

checker-board pattern of TOT and Time

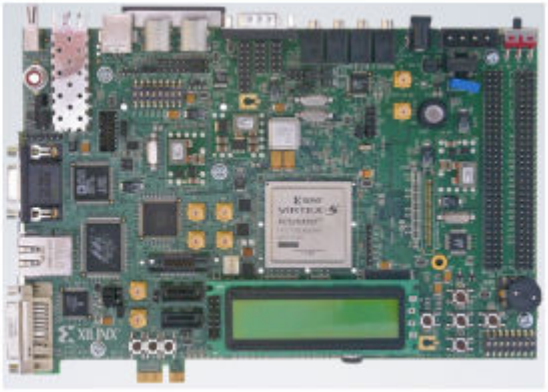


New FPGA-based Readoutsystem by University of Mainz

Mainz is designing and building a new FPGA-based readout for Timepix chips.

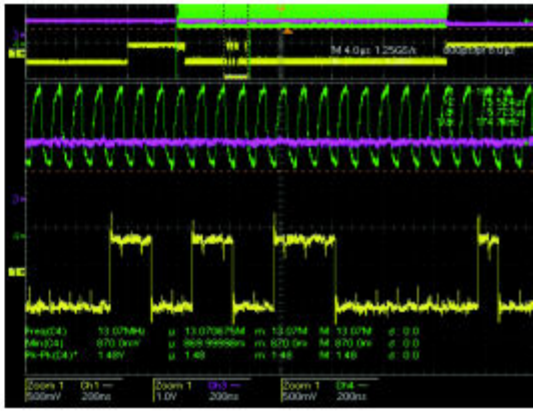


- Readout with maximum speed (100MHz)
- Connection to PC with Gigabit Ethernet
- FPGA:
  - De-/serialization of data streams
  - Conversion CMOS – LVDS
  - Firmware in VHDL



XYLINX–development board

- Software and firmware are in good shape but some missing functionality until now
- Serialization and ethernet communication are correct
- Not at full speed yet (needs matching of clock to delayed data stream in Timepix)
- Chip can be read out, test with detector at Bonn soon



Electronics for NEXT: a neutrino experiment with a Xenon gas TPC

A solution based on RD-51 electronics

J. Toledo on behalf of the NEXT collaboration

Goal: **build and operate a TPC filled with 100 kg HPGXe enriched with ^{136}Xe to measure its $\beta\beta0\nu$ decay.**

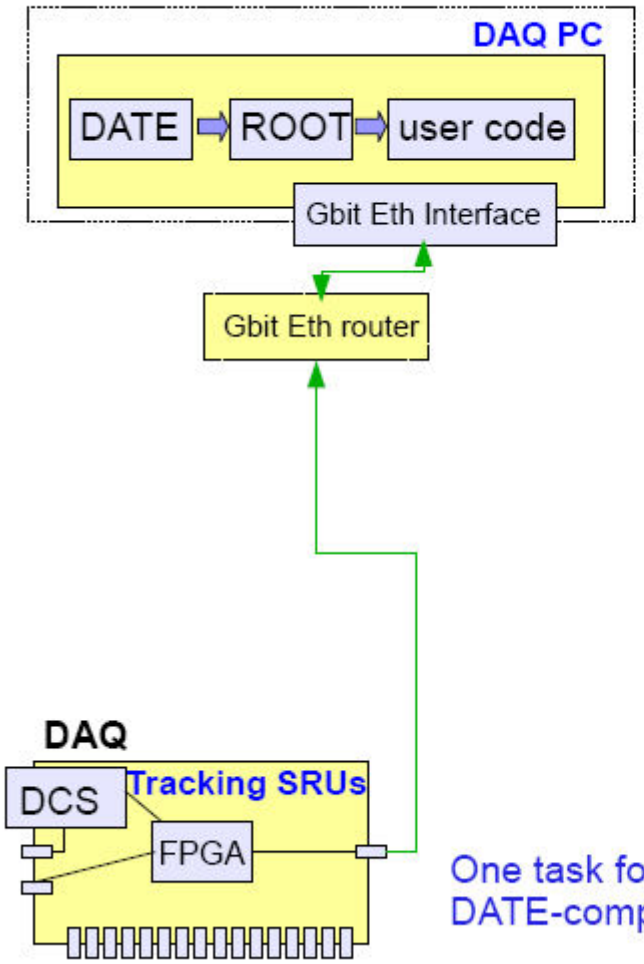
Time schedule

- ✓ $1^{1/2}$ years from now for the NEXT-1 prototype operation
- ✓ $2^{1/2}$ years from now for the 1:10 prototype NEXT-10 to prove feasibility
- ✓ $4^{1/2}$ years from now for NEXT-100 with full operation in the LSC

We plan to use RD-51 electronics already in NEXT-1

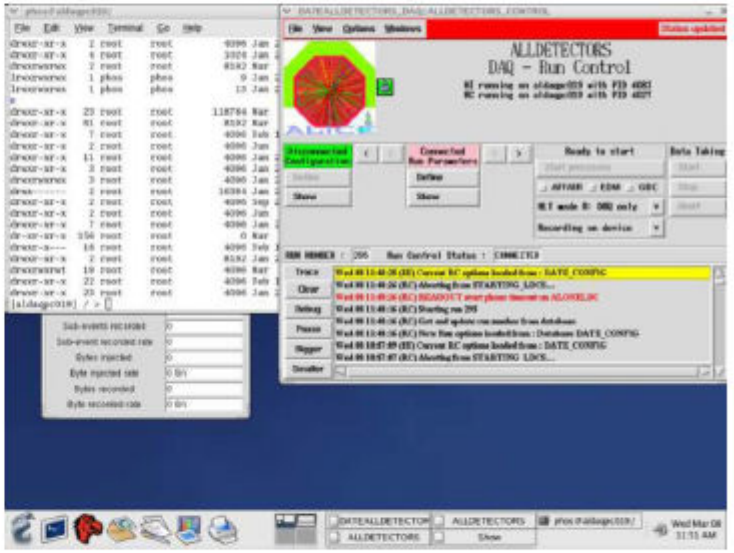
NEXT:

Online system



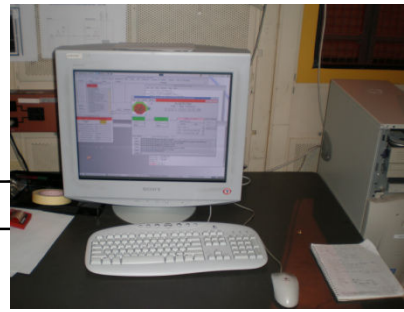
DAQ PC running ALICE DATE (Data Acquisition and Test Environment)

DATE produces ROOT compatible files
Soon: DATE support for Gigabit Ethernet (Q4'09)



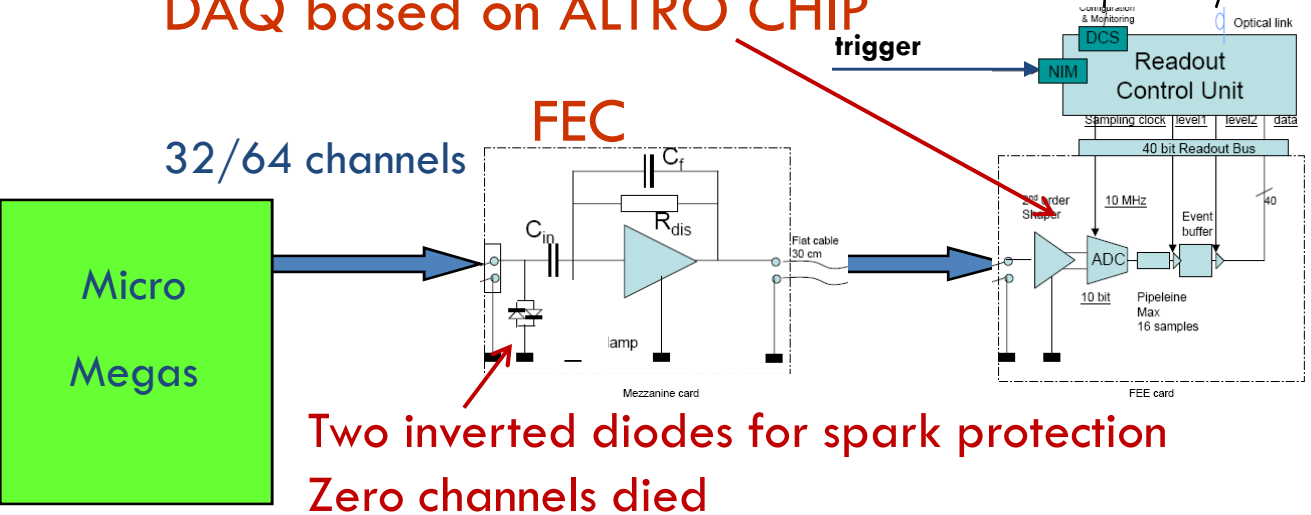
One task for NEXT in RD-51:
DATE-compatible Gbit Ethernet frames generation from FPGA

Mmega Setup (Atlas)



DAQ PC (ALICE DATE)

DAQ based on ALTRO CHIP



Two inverted diodes for spark protection

Zero channels died

32 channels

200 ns integration time

64 charge samples/ch

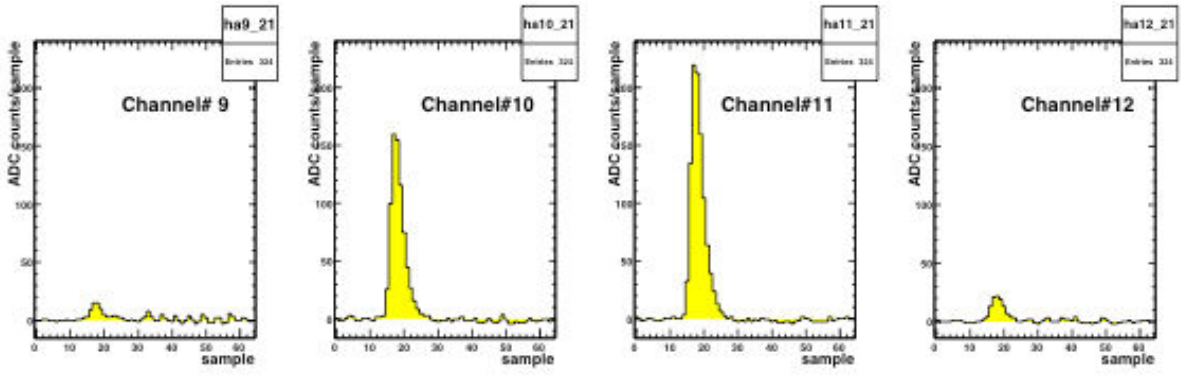
100 ns/sample

15 pre-samples

1 ADC count ~ 1000 e^-

Typical ADC spectra

- Noise subtraction (from 12 pre-samples)
- Custer position from center of gravity



Mmega Experience with DATE

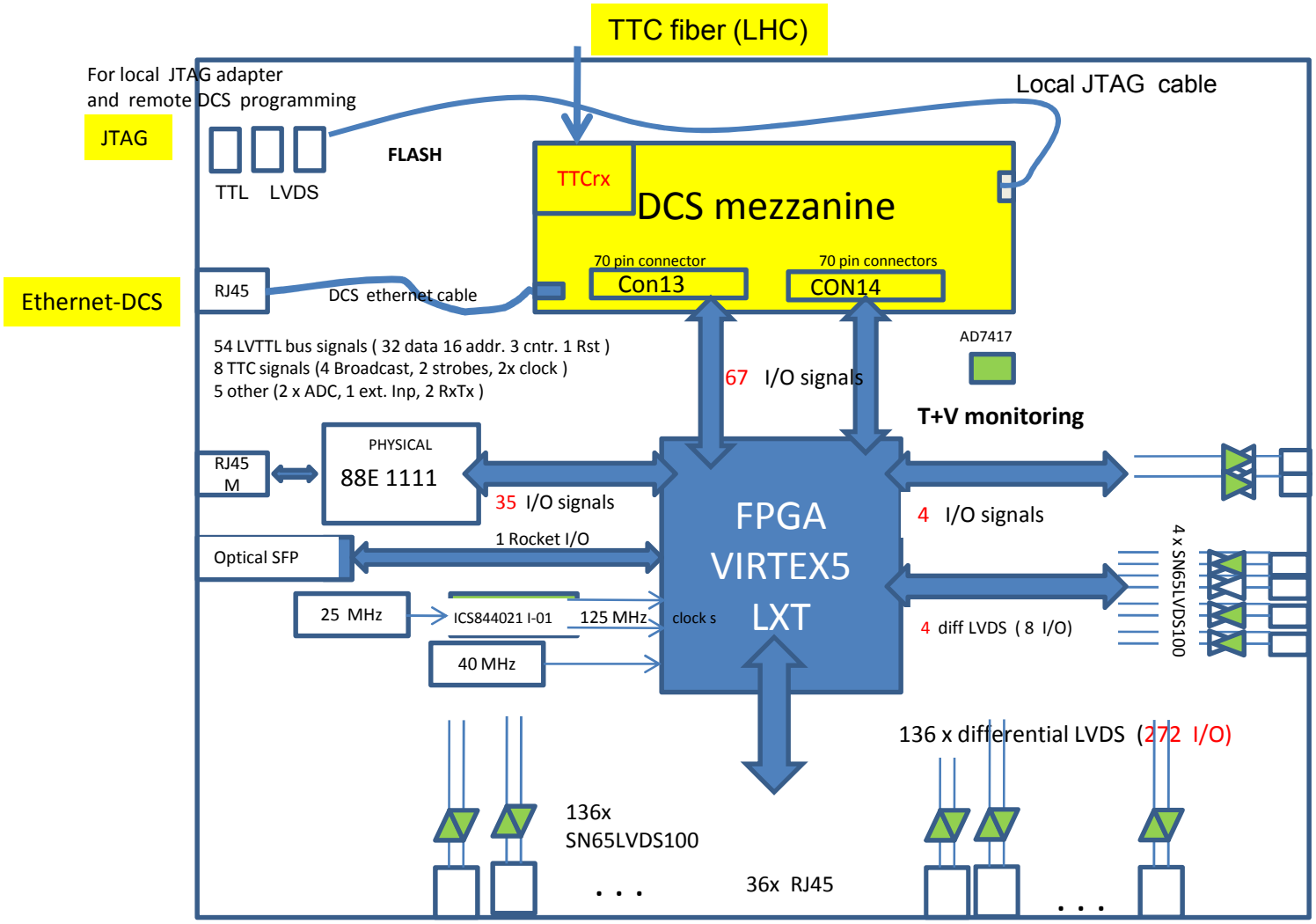
- Run Control system (DATE): very nice

  Easy to handle and extremely stable
- Readout controller (RCU)

  Fragile: must be protected against trigger signals while initializing, and during processing

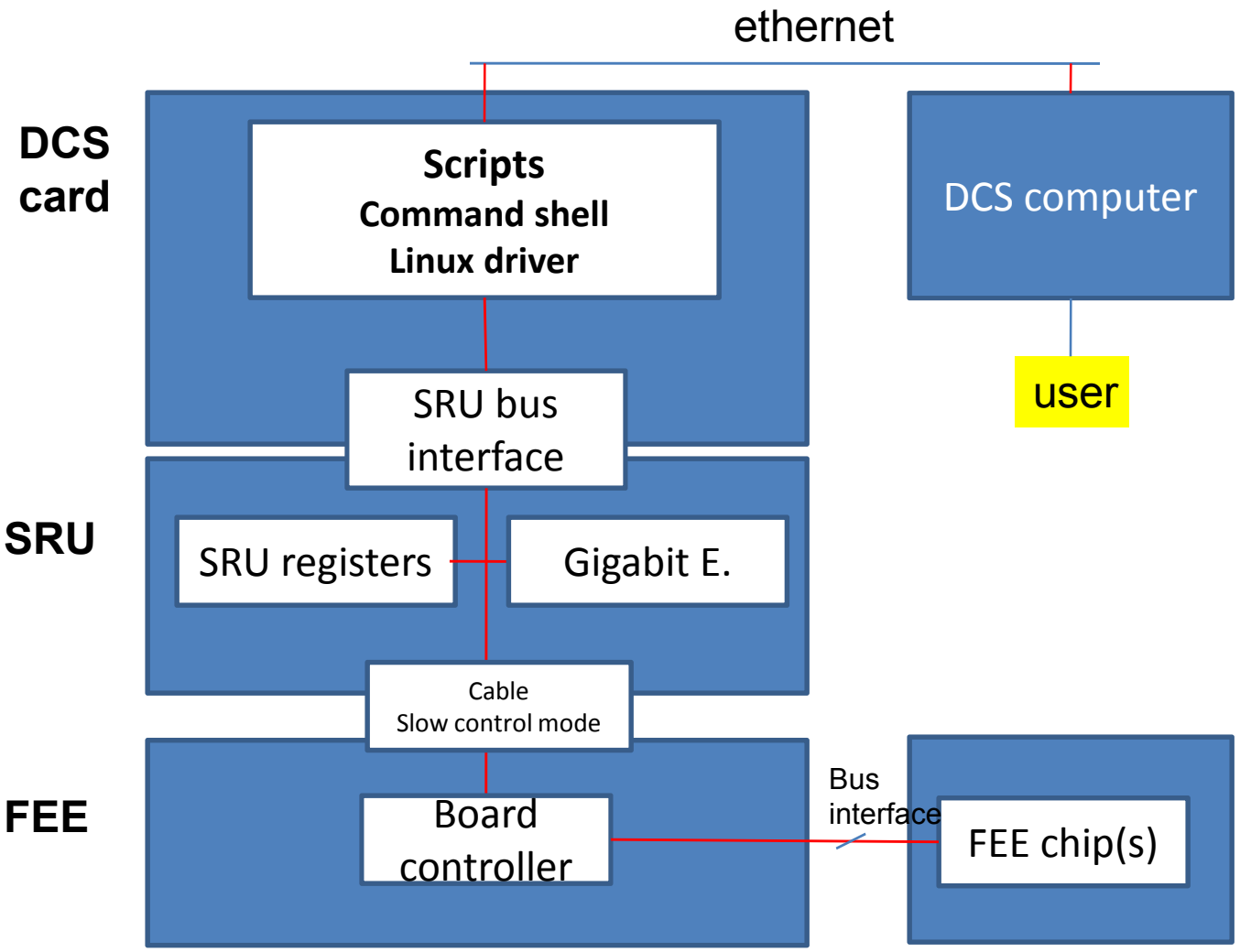
  Initialization through ethernet connection, not integrated in the RunControl (a bit clumsy)

DCS mezzanine on SRU



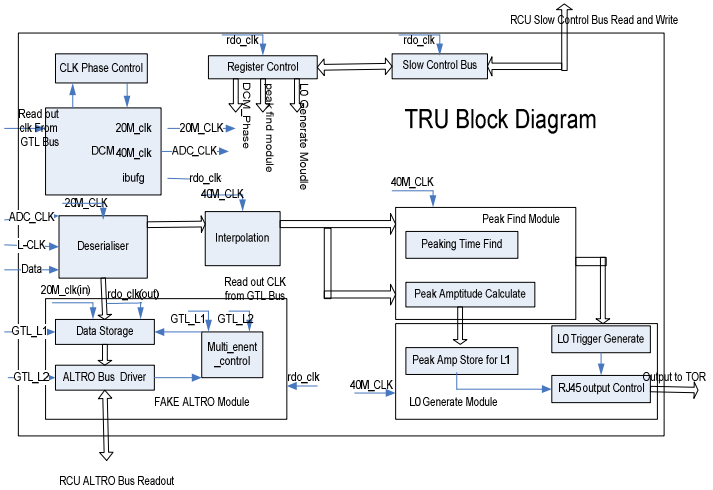
36 x Serial quad LVDS links (CAT6) to FEE cards

Slow controls Overview



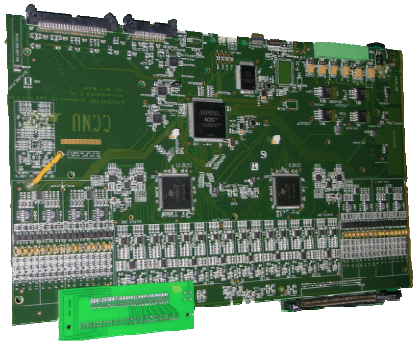
Huazhong Normal University (Wuhan) activities within RD51 scalable readout project

FEE card produced in Huazhong Normal University for ALICE/PHOS project

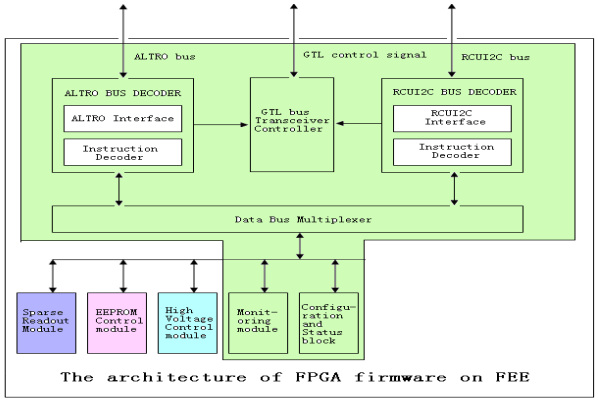


Firmware of PHOS/TRU trigger ca

Readout Electronics Test Setup

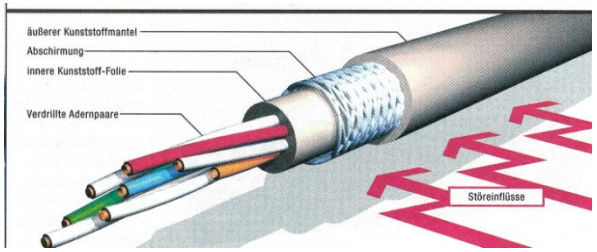


Altro-based FEE card for APD readout



Board Controller Firmware of FEE &
Participation in ALICE RCU

Wuhan tasks: BC firmware and serial protocol



4 x twisted pairs

max 15 m @ 280 Mbit/s

clock
data
select
return

CAT 6 cable

34 x

FEE

RJ45

FPGA

4

chip Interface bus

Board Controller Firmware

SRU

RJ45

Reversible LVDS drivers/receivers

FPGA

4

10 GBE

Input data stream from
36 FEE's ~ 10 Gbit/s

Summary

- Common readout system well on track
- Preferred chip choices done
- Proto RO system by end 2009
- Full systems mid/end 2010
- Driven by applications (NEXT etc)
- New teams joined and new manpower
- More participation welcome